# N-Channel 30-V (D-S) 175°C MOSFET

## CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

## DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## SUBCIRCUIT MODEL SCHEMATIC
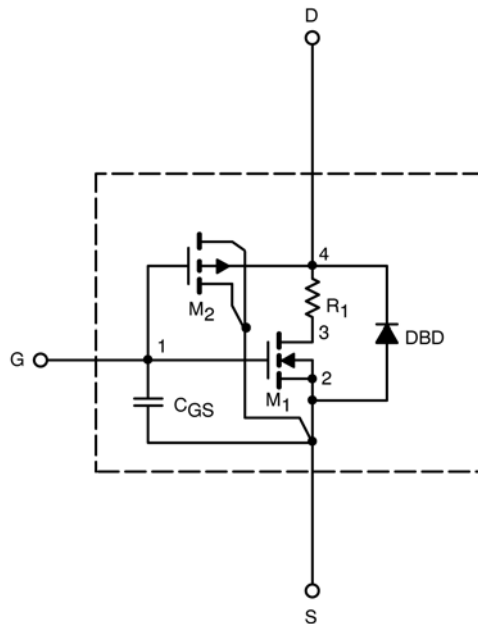


This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

# SPICE Device Model SUM110N03-04P
## Vishay Siliconix

| Parameter | Symbol | Test Conditions | Simulated Data | Measured Data | Unit |
|---|---|---|---|---|---|
| **SPECIFICATIONS (T$_J$ = 25°C UNLESS OTHERWISE NOTED)** | | | | | |
| **Static** | | | | | |
| Gate Threshold Voltage | V$_{GS(th)}$ | V$_{DS}$ = V$_{GS}$, I$_D$ = 250 μA | 1.8 | | V |
| On-State Drain Current[a] | I$_{D(on)}$ | V$_{DS}$ = 5 V, V$_{GS}$ = 10 V | 1375 | | A |
| Drain-Source On-State Resistance[a] | r$_{DS(on)}$ | V$_{GS}$ = 10 V, I$_D$ = 20 A | 0.0033 | 0.0033 | Ω |
| | | V$_{GS}$ = 10 V, I$_D$ = 20 A, T$_J$ = 125°C | 0.0049 | | |
| | | V$_{GS}$ = 10 V, I$_D$ = 20 A, T$_J$ = 175°C | 0.0058 | | |
| | | V$_{GS}$ = 4.5 V, I$_D$ = 20 A | 0.0052 | 0.0052 | |
| Forward Transconductance[a] | g$_{fs}$ | V$_{DS}$ = 15 V, I$_D$ = 20 A | 70 | | S |
| Forward Voltage[a] | V$_{SD}$ | I$_S$ = 100 A, V$_{GS}$ = 0 V | 0.92 | 1.2 | V |
| **Dynamic**[b] | | | | | |
| Input Capacitance | C$_{iss}$ | V$_{GS}$ = 0 V, V$_{DS}$ = 25 V, f = 1 MHz | 5194 | 5100 | Pf |
| Output Capacitance | C$_{oss}$ | | 780 | 860 | |
| Reverse Transfer Capacitance | C$_{rss}$ | | 292 | 430 | |
| Total Gate Charge[c] | Q$_g$ | V$_{DS}$ = 15 V, V$_{GS}$ = 4.5 V, I$_D$ = 50 A | 43 | 40 | NC |
| Gate-Source Charge[c] | Q$_{gs}$ | | 18 | 18 | |
| Gate-Drain Charge[c] | Q$_{gd}$ | | 16 | 16 | |
| Turn-On Delay Time[c] | t$_{d(on)}$ | V$_{DD}$ = 15 V, R$_L$ = 0.30 Ω I$_D$ ≅ 50 A, V$_{GEN}$ = 10 V, R$_G$ = 2.5 Ω | 13 | 12 | Ns |
| Rise Time[c] | t$_r$ | | 15 | 12 | |
| Turn-Off Delay Time[c] | t$_{d(off)}$ | | 31 | 40 | |
| Fall Time[c] | t$_f$ | | 31 | 10 | |

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

COMPARISON OF MODEL WITH MEASURED DATA (T$_J$=25°C UNLESS OTHERWISE NOTED)
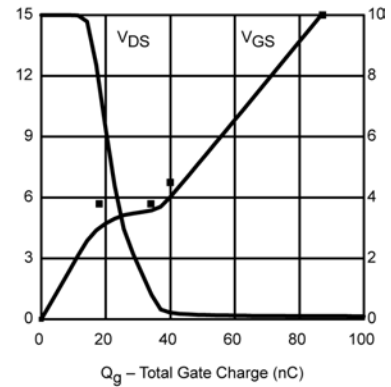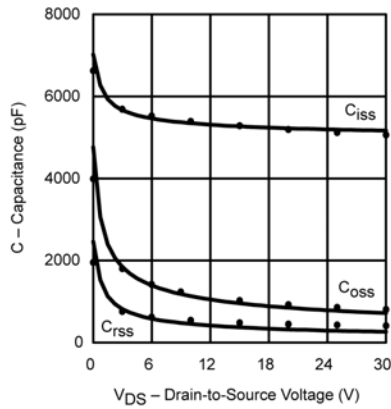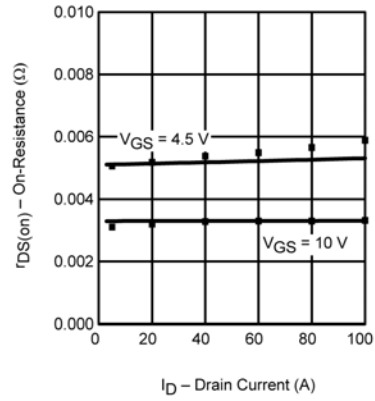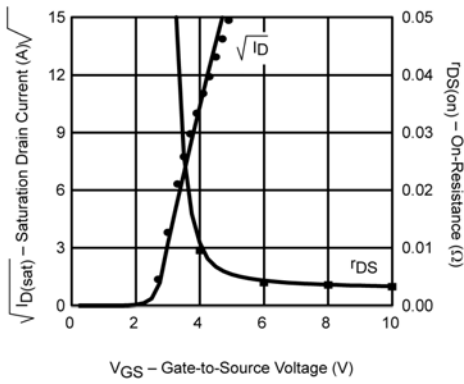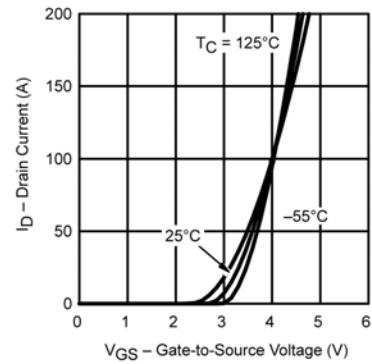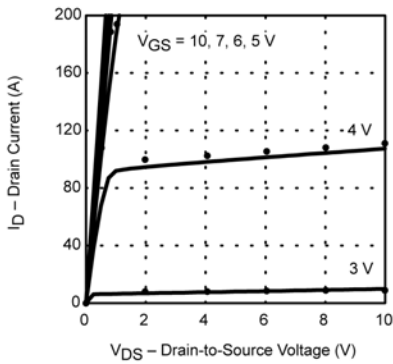
Note: Dots and squares represent measured data.