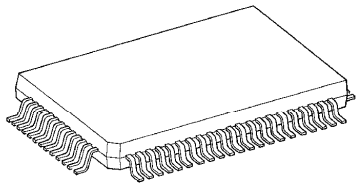
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T6A11A, JT6A11AX-AS

T6A11A, JT6A11AX-AS CMOS 1 CHIP LSI FOR LCD ELECTRONIC CALCULATOR

The T6A11A, JT6A11AX-AS is a 1 chip microcomputer for 12-digits 2-memory or 10-digits 2-memory electronic calculator.
T6A11A, JT6A11AX-AS can drive the liquid crystal display (LCD) with single power supply.
Single power supply operation, wide operating voltage range and low power consumption make it suitable for 1.5V solar battery operated calculator.
Besides T6A11A, JT6A11AX-AS can selectable with a pin-programmable to function of Power timer and Memory hold.



QFP67-P-1420-0.80

Weight : 1.20g (Typ.)

FEATURES

Operational Features :

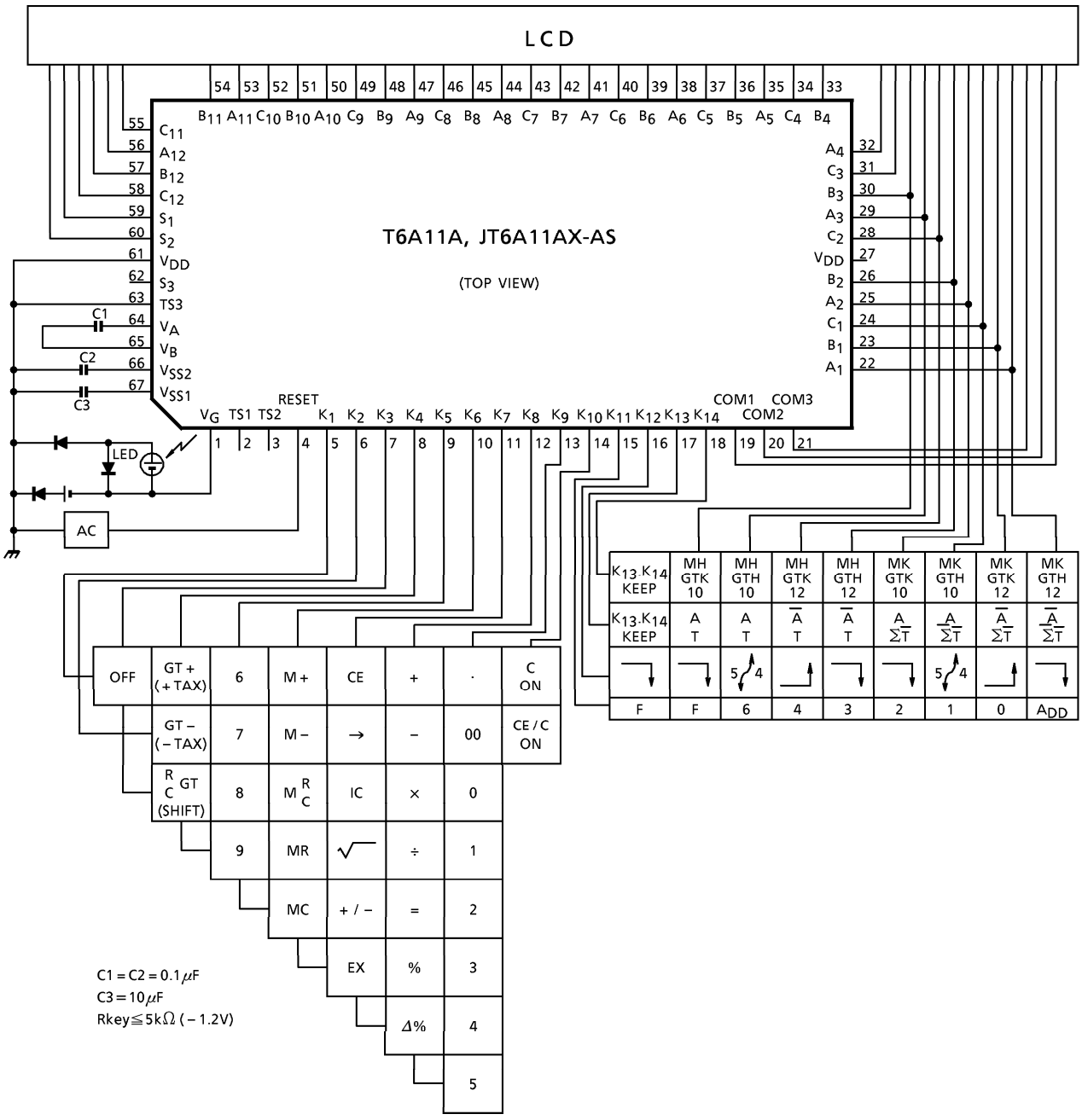
- Display : 12-digits or 10-digits (selectable with a pin-programmable) of data, 2-digits of sign, error symbol, memory load symbol.
- Algebraic mode.
- Standard 4 functions (+, −, ×, ÷).
- Memory and grand total (GT) memory calculation.
- Accumulating GT memory register with count up (down) item counter.
- Automatic percentage operation with add-on, discount.
- Automatic delta percentage, mark-up and markdown operations.
- Square root.
- Constant calculation.
- Chain calculation.
- Change sign.
- Floating point or momentary mode (selectable with a switch).
- Fixed point ("0", "1", "2", "3", "4" or "6" places) or floating point (selectable with a switch).
- Adding point mode (selectable with a switch).

- Rounding switches (rounding up, down and off).
- Leading zero suppression.
- Trailing zero suppression.
- Punctuation on display, commas for thousands.
- Memory and GT memory contents indicator, turned on with non-zero in the memory and GT memory.
- Registration overflow, indicating that too many digits are entered (the most significant digit are protected).
- Result overflow, indicating during calculation (most function key are locked as it happened).
- Memory overflow indicating to flashing of memory load mark.
- TAX calculation.

Electrical Features

- Complementary output buffer for direct driving of liquid crystal display (F.E.M LCD).
- Oscillator / clock generator internal to chip.
- Keyboard encoding internal to chip.
- Keyboard denouncing internal to chip.
- Automatic power on clear.
- Wide supply voltage range (– 1.2~ – 2.0V).
- Very low power consumption (3.3μW typ.).
- Quad in line flat package.

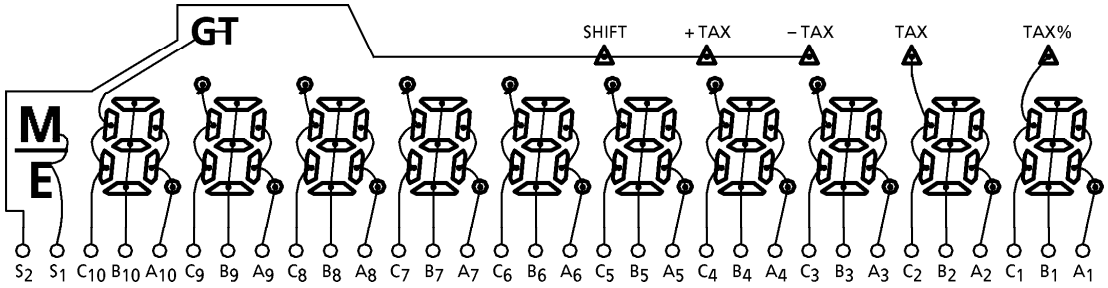
SYSTEM BLOCK DIAGRAM



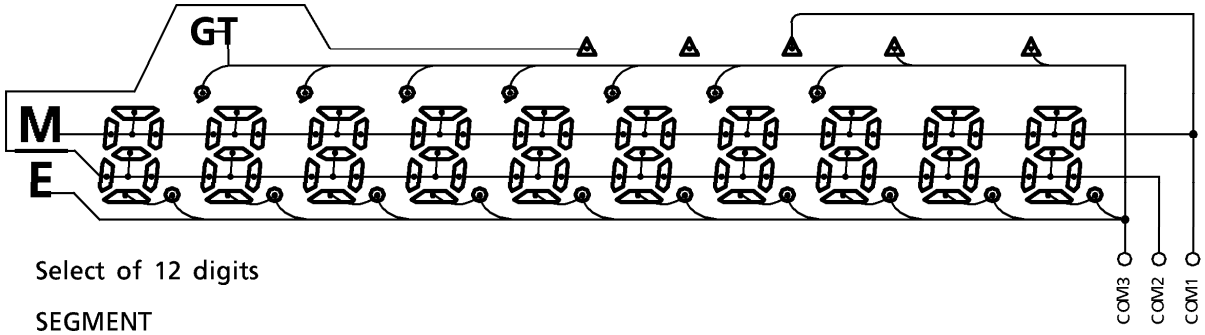
CONNECTION OF LCD

(1) Select of 10 digits

SEGMENT

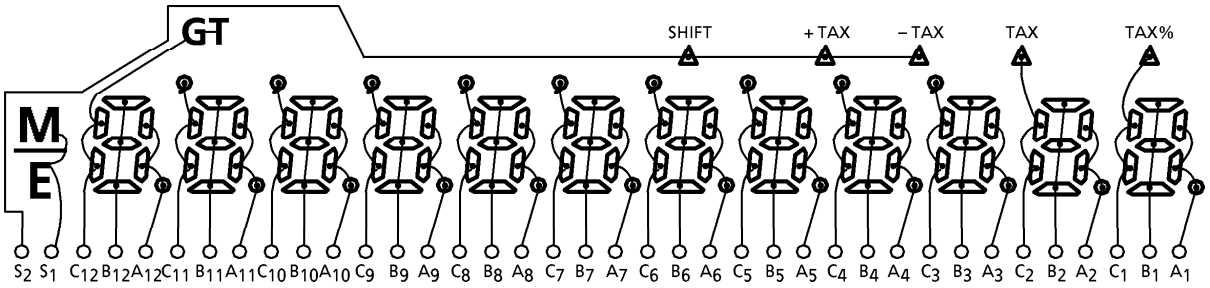


COMMON

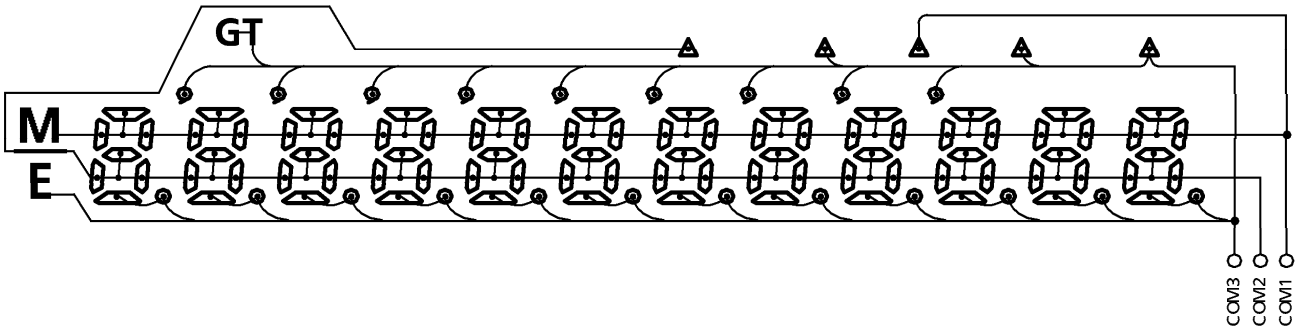


(2) Select of 12 digits

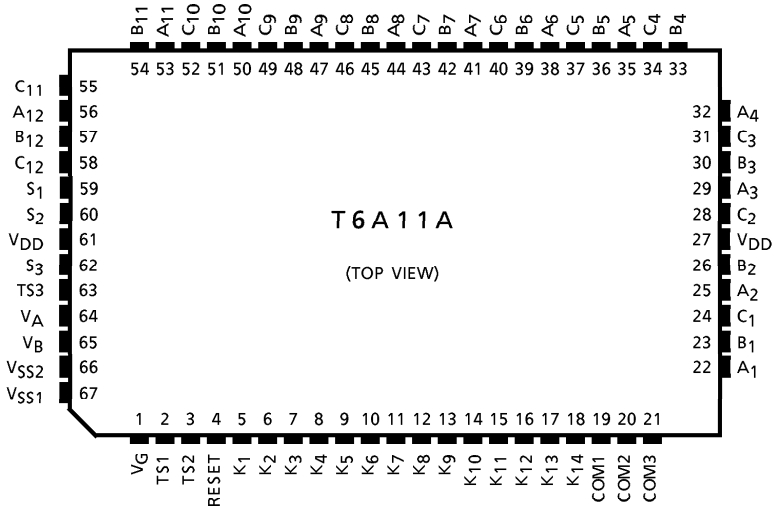
SEGMENT



COMMON

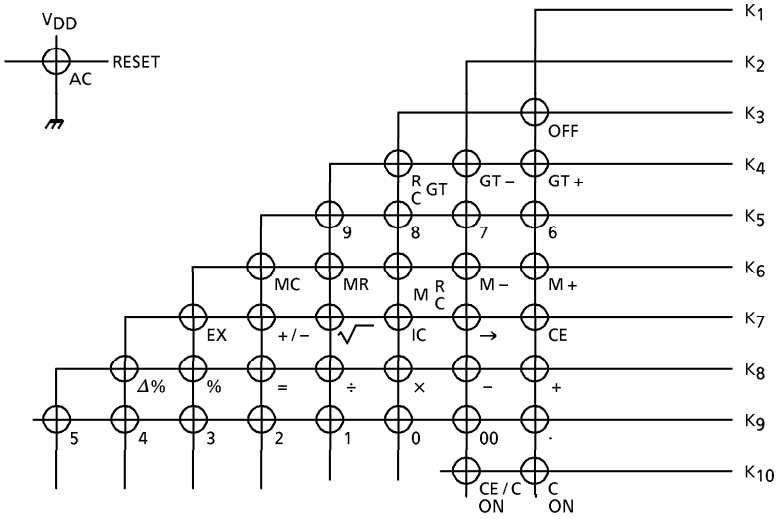


PIN LAYOUT

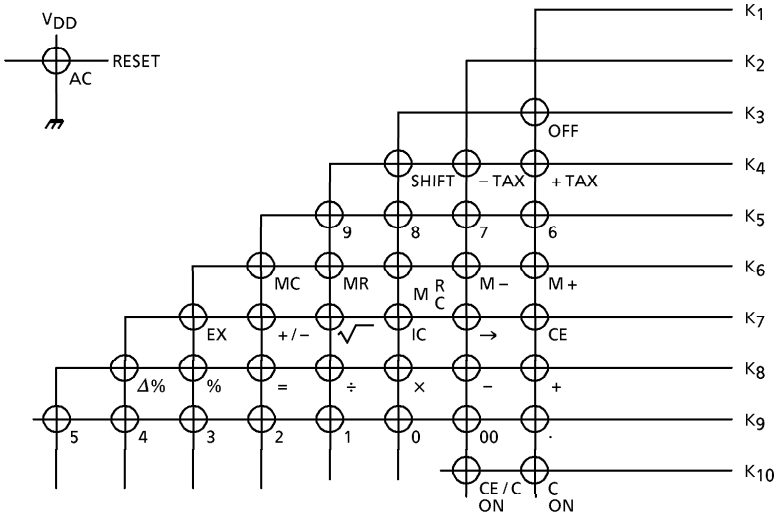

B11 A11 C10 B10 A10 C9 B9 A9 C8 B8 A8 C7 B7 A7 C6 B6 A6 C5 B5 A5 C4 B4
54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33
C11 55
A12 56
B12 57
C12 58
S1 59
S2 60
VDD 61
S3 62
TS3 63
VA 64
VB 65
VSS2 66
VSS1 67
32 A4
31 C3
30 B3
29 A3
28 C2
27 VDD
26 B2
25 A2
24 C1
23 B1
22 A1
T6A11A
(TOP VIEW)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21
VG TS1 TS2 RESET K1 K2 K3 K4 K5 K6 K7 K8 K9 K10 K11 K12 K13 K14 COM1 COM2 COM3

KEY LAYOUT

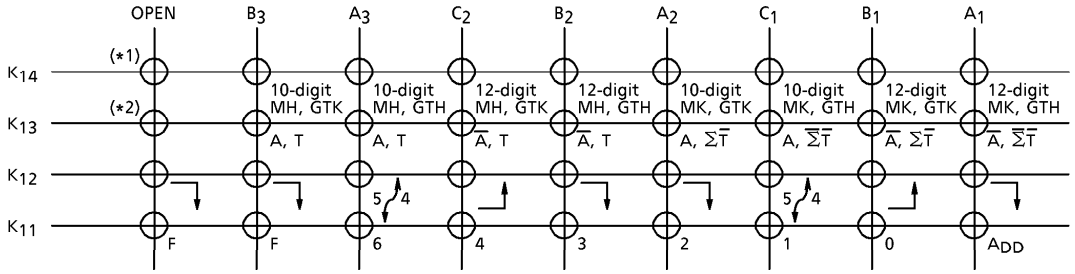
- Touch Key (Grand total memory type)



- Touch Key (TAX calculation type)



- Lock Key



K_{14} ... Selectable with calculated digits and memory hold status.
- 10digit / 12digit : Digits of calculation
- MH : Memory hold at auto power off or off function.
- MK : Memory kill at auto power off or off function.
- GTH : GT memory hold at auto power off or off function.
- GTK : GT memory kill at auto power off or off function.

K_{13} ... Selectable with auto power off mode and TAX calculation mode and total (Σ mode) switch.
- A : Auto power off enable.
- $\overline{A}$: Auto power off disable.
- (*3) T : TAX calculation mode.
- $\overline{T}$: GT memory mode.
- Σ : Σ mode enable.
- $\overline{\Sigma}$: Σ mode disable.

K_{12} ... Rounding switches.

K_{11} ... Selectable with fixed point or floating mode.

(*1), (*2) : If K_{13} or K_{14} get opened, the status before these keys open is hold. In the case of power on with K_{13} or K_{14} open, the status 10 digit and $\overline{\Sigma}$, $\overline{A}$ mode is selected automatically.

(*3) : If exchange the mode of TAX calculation and GT memory, please reset the system for [AC] key.

SPECIFICATION OF CALCULATOR

Speed of Calculator (standard oscillating frequency $f\phi$ = 48kHz)

- Numeral ..... 11.8~17.7ms
- Function
  - 1 [+] 25.6ms
  - 1 [+] 2 [+] 95.2ms
- Addition and Subtract
  - 1 2 3 [+] 1 [=] 89.1ms
  - 9999999999 [−] 0.000000001 [=] 111.8ms
- Multiply
  - 1 2 3 [×] 2 [=] 109.6ms
  - 1 [×] 9999999999 [=] 207.7ms
- Device
  - 1 2 3 [÷] 3 [=] 147.9ms
  - 9999999999 [÷] 1 [=] 249.0ms
- Memory calculation
  - 2 [M+] 143.3ms
  - 9999999999 [÷] 1 [M+] 296.2ms
- Square root
  - 9999999999 [√] 167.7ms
  - 2 [√] 125.0ms

Key for Calculator

[0 0], [0]~[9]	: Number
[·]	
[+/−]	: Changer Sign
[+] [−] [×] [÷]	: Function
[=] [√] [%] [Δ%]	
[M+] [M−] [GT+] [GT−]	: Memory
[MC] [MR] [M RC] [RC GT]	
[EX]	: Exchange
[→]	: Shift
[IC]	: Item Counter Grand total memory type ··· MAX. count 999. TAX calculation type ··· MAX. count 99.
[CE] [CE/C (ON)] [C (ON)]	: Clear
[OFF]	: OFF
[AC]	: SYSTEM RESET

Operation Example

1. Fixed Point calculation

① Key	Display	Fixed Point Place
C	0.	DP = 3 (5 / 4)
2	2.	
÷	2.	
3	3.	
=	0.667	
2	2.	
·	2.	
3	2.3	
+	2.3	
4	4.	
M+	6.300	
1	1.	
·	1.	
2	1.2	
M+	1.200	
MR	7.5	

② Key	Display	Fixed Point Place
C	0.	DP = 0 (⌐)
1	1.	
·	1.	
2	1.2	
3	1.23	
+	1.23	
1	1.	
·	1.	
1	1.1	
=	3.	
9	9.	
√	3.	
×	3.	
1	1.	
·	1.	
1	1.1	DP = F
=	3.3	

2. Adding Point mode calculation

Key	Display	Key	Display	Key	Display
C	0.	M+	0.02M	=	33.27M –
1	1.	3	3.M	2	2.M
23	123.	·	3.M	+	0.02M
+	1.23	123	3.123M	9	9.M
3	3.	M+	3.12M	·	9.M
=	1.26	MR	3.14M	√	3.M
3	3.	C	0.M	=	3.02M
2	32.	1	1.M		
×	32.	23	123.M		
3	3.	–	1.23M		
·	3.	3	3.M		
000	3.000	4	34.M		
=	96.00	·	34.M		
2	2.	5	34.5M		

3. Constant Calculation

① Multiplication

Key	Display	Constant
k	k	
×	k	
a	a	
=	k·a	k ×
b	b	k ×
=	k·b	k ×

② Division

Key	Display	Constant
a	a	
÷	a	
k	k	
=	a / k	÷ k
b	b	÷ k
=	b / k	÷ k

③ Addition

a	a	
+	a	
k	k	
=	a + k	+ k
b	b	+ k
=	b + k	+ k

④ Subtraction

a	a	
−	a	
k	k	
=	a − k	− k
b	b	− k
=	b − k	− k

⑤ Percentage

k	k	
×	k	
a	a	
%	k·a / 100	k ×
b	b	k ×
%	k·b / 100	k ×

⑥ Percentage

a	a	
÷	a	
k	k	
%	100·a / k	+ k
b	b	÷ k
%	100·b / k	÷ k

⑦ Add-on

k	k	
+	k	
a	a	
%	k· (1 + a / 100)	k +
b	b	k +
%	k· (1 + b / 100)	k +

⑧ Discount

k	k	
−	k	
a	a	
%	k· (1 − a / 100)	k −
b	b	k −
%	k· (1 − b / 100)	k −

4. Δ% Calculations

① Key Display

a	a
[+]	a
b	b
[Δ%]	100· (a + b) / b

② Key Display

a	a
[−]	a
b	b
[Δ%]	100· (a − b) / b

5. Mark-up, Mark-down Calculations

① Mark-up

Key Display

a	a
[÷]	a
b	b
[Δ%]	a / (1 − b / 100)
[Δ%]	|a / (1 − b / 100) − a|

② Mark-down

Key Display

a	a
[÷]	a
b	b
[+/−]	− b
[Δ%]	a / (1 + b / 100)
[Δ%]	|a / (1 + b / 100) − a|

6. Add-on, Discount Calculations

Add-on

Key Display

① a a
[×] a
b b
[%] a·b / 100
[+] a·b / 100
[=] a (1 + b / 100)

③ a a
[+] a
b b
[%] a (1 + b / 100)

⑤ a a
[×] a
b b
[Δ%] a (1 + b / 100)

Discount

Key Display

② a a
[×] a
b b
[%] a·b / 100
[−] a·b / 100
[=] a (1 − b / 100)

④ a a
[−] a
b b
[%] a (1 − b / 100)

⑥ a a
[×] a
b b
[+/−] − b
[Δ%] a (1 − b / 100)

7. Average Operation use of the Item Counter

Key	Display	Item Counter	Key	Display	Item Counter
A	A	0	[−]	A + B + C + D	2
[+]	A	1	D	D	2
B	B	1	[+]	A + B + C	3
[+]	A + B	2	E	E	3
C	C	2	[=]	A + B + C + E	4
[+]	A + B + C	3	[÷]	A + B + C + E	4
D	D	3	[IC]	4	4
[+]	A + B + C + D	4	[=]	(A + B + C + E) / 4	5

8. TAX Calculation

	Key Op.	Display	
(1)	A	A	
	[SHIFT]	A	[SHIFT]
	[+TAX]	A	[TAX%]
(2)	[SHIFT]	0.	[SHIFT]
	[−TAX]	A	[TAX%]
(3)	B	B	
	[+TAX]	B (1 + A / 100)	[+TAX]
	[+TAX]	B·A / 100	[TAX]
	[+TAX]	B (1 + A / 100)	[+TAX]
	[+TAX]	B·A / 100	[TAX]
(4)	B	B	
	[−TAX]	B / (1 + A / 100)	[−TAX]
	[−TAX]	B − B / (1 + A / 100)	[TAX]
	[−TAX]	B / (1 + A / 100)	[−TAX]
	[−TAX]	B − B / (1 + A / 100)	[TAX]

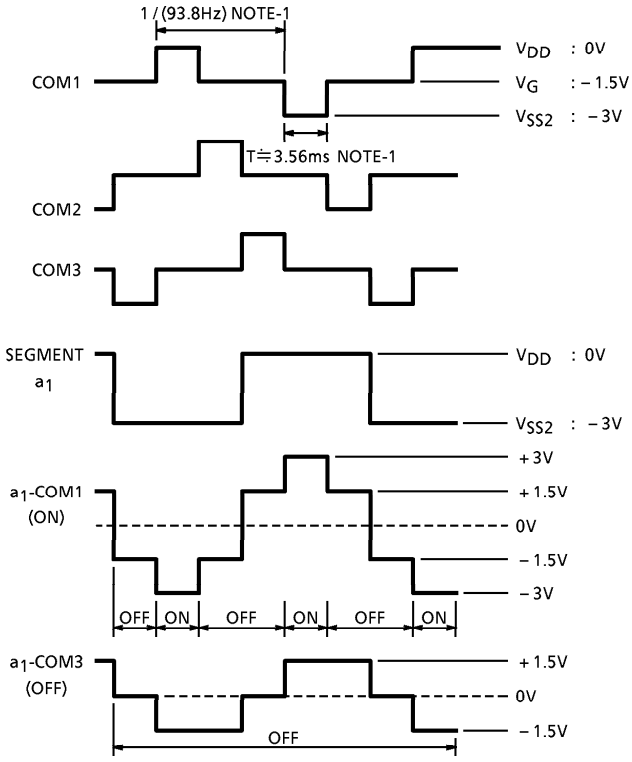
MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_G	+0.3~−2.0	V
Input Voltage	V_{IN}	+0.3~V_G−0.3	V
Operating Temperature	T_{opr}	0~40	°C
Storage Temperature	T_{stg}	−55~125	°C

ELECTRICAL CHARACTERISTICS (V_G = −1.5±0.2V, V_{SS2} = −3.0±0.4V, V_{DD} = 0V, Ta = 25°C)

PARAMETER		SYMBOL	TEST CIR-CUIT	PIN NAME	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage		V_G	—	—	—	−1.2	−1.5	−2.0	V
"1" Input Voltage		V_{IH} (1)	—	K_3~K_{10} RESET	—	V_G +0.4	—	V_G	V
"1" Input Voltage		V_{IH} (2)	—	K_{11}~K_{14}	—	V_{SS2} +0.4	—	V_{SS2}	V
"0" Input Voltage		V_{IL}	—	K_3~K_{14} RESET	—	0	—	−0.4	V
"1" Output Voltage		V_{OH} (1)	—	SEGMENT COM1~3	—	V_{SS2} +0.2	—	V_{SS2}	V
"0" Output Voltage		V_{OL} (1)	—	SEGMENT COM1~3	—	0	—	−0.2	V
"M" Output Voltage		V_{OM}	—	COM1~3	—	V_G +0.2	—	V_G −0.2	V
"1" Output Voltage		V_{OH} (2)	—	K_1~K_{10}	—	V_G +0.2	—	V_G	V
"0" Output Voltage		V_{OL} (2)	—	K_1~K_{14}	—	0	—	−0.2	V
"1" Output Resistance		R_{OH}	—	SEGMENT COM1~3	V_{OUT} = V_{SS2} + 0.5V	—	—	70	kΩ
"0" Output Resistance		R_{OL}	—	SEGMENT COM1~3	V_{OUT} = −0.5V	—	—	70	kΩ
Key Pull Up Resistance		R_{KEYH} (1)	—	RESET	V_{OUT} = 0V	156	—	364	kΩ
		R_{KEYH} (2)	—	K_1~K_{10}	V_{OUT} = 0V	240	—	560	
Key Read Pull Up Resistance		R_{KEYH} (3)	—	K_1~K_{10}	V_{OUT} = 0V	30	—	600	kΩ
Key Pull Down Resistance		R_{KEYL} (1)	—	RESET K_1~K_{10}	V_{OUT} = −0.5V	—	—	10	kΩ
		R_{KEYL} (2)	—	K_{11}~K_{14}	V_{OUT} = V_{SS2}	120	—	800	
Oscillating Frequency	(WAIT)	$f\phi$WAIT	—	—	V_G = −1.5V	5.4	9.0	12.6	kHz
	(OPERATE)	$f\phi$OP	—	—	V_G = −1.5V	28.8	48	67.2	
Frame Frequency		f_F	—	SEGMENT COM1~3	V_G = −1.5V	56.3	93.8	131	Hz
Supply Current	1 (WAIT)	I_{DDWAIT}	—	—	V_G = −1.5V	—	2.2	3.4	μA
	2 (OPERATE)	I_{DDOP}	—	—	V_G = −1.2V	—	7.0	11.0	
	3 (OFF)	I_{DDOFF}	—	—	V_G = −1.5V	—	—	2.0	
Power Off Timer Times		T	—	—	V_G = −1.5V	429	600	1001	s

WAVEFORMS FOR DISPLAY



NOTE-1 at $f\phi$ = 9kHz

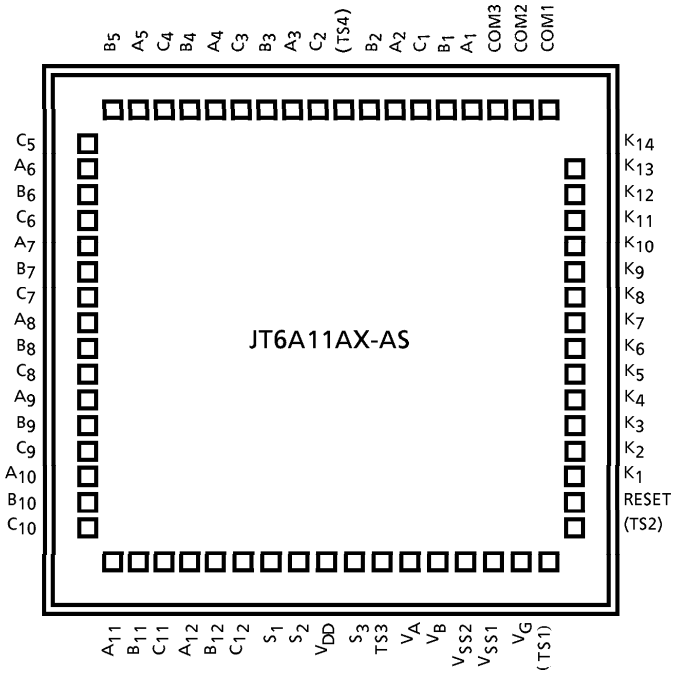
PAD LOCATION TABLE (μm)

NAME	X POINT	Y POINT
V_{SS1}	971	– 1469
V_{SS2}	775	– 1469
V_B	609	– 1469
V_A	424	– 1469
TS3	252	– 1469
S_3	100	– 1469
V_{DD}	– 52	– 1469
S_2	– 203	– 1469
S_1	– 355	– 1469
C_{12}	– 507	– 1469
B_{12}	– 659	– 1469
A_{12}	– 810	– 1469
C_{11}	– 980	– 1469
B_{11}	– 1162	– 1469
A_{11}	– 1358	– 1469
C_{10}	– 1408	– 1193
B_{10}	– 1408	– 1042
C_{10}	– 1408	– 890
C_9	– 1408	– 738
B_9	– 1408	– 586
A_9	– 1408	– 435
C_8	– 1408	– 283
B_8	– 1408	– 131
A_8	– 1408	20
C_7	– 1408	172
B_7	– 1408	324
A_7	– 1408	475
C_6	– 1408	627
B_6	– 1408	779
A_6	– 1408	936
C_5	– 1408	1119
B_5	– 1358	1469
A_5	– 1169	1469

NAME	X POINT	Y POINT
C_4	– 999	1469
B_4	– 847	1469
A_4	– 696	1469
C_3	– 544	1469
B_3	– 392	1469
A_3	– 240	1469
C_2	– 89	1469
*(TS4)	89	1469
B_2	241	1469
A_2	392	1469
C_1	544	1469
B_1	696	1469
A_1	847	1469
COM3	999	1469
COM2	1166	1469
COM1	1358	1469
K_{14}	1408	1175
K_{13}	1408	1023
K_{12}	1408	871
K_{11}	1408	720
K_{10}	1408	503
K_9	1408	352
K_8	1408	200
K_7	1408	48
K_6	1408	– 104
K_5	1408	– 255
K_4	1408	– 407
K_3	1408	– 559
K_2	1408	– 710
K_1	1408	– 862
RESET	1408	– 1023
*(TS2)	1408	– 1175
*(TS1)	1367	– 1469
V_G	1160	– 1469

*( ) Do not connect.

CHIP LAYOUT

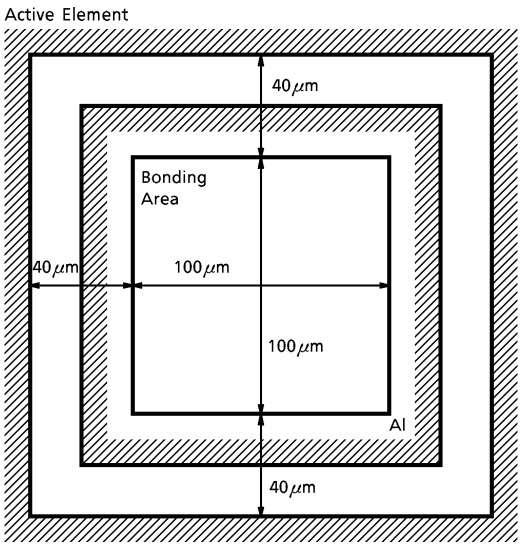


Chip size : 3.28×3.46 [mm]

Chip thickness : 440±30μm

Substrate : V_{DD}

PAD LAYOUT

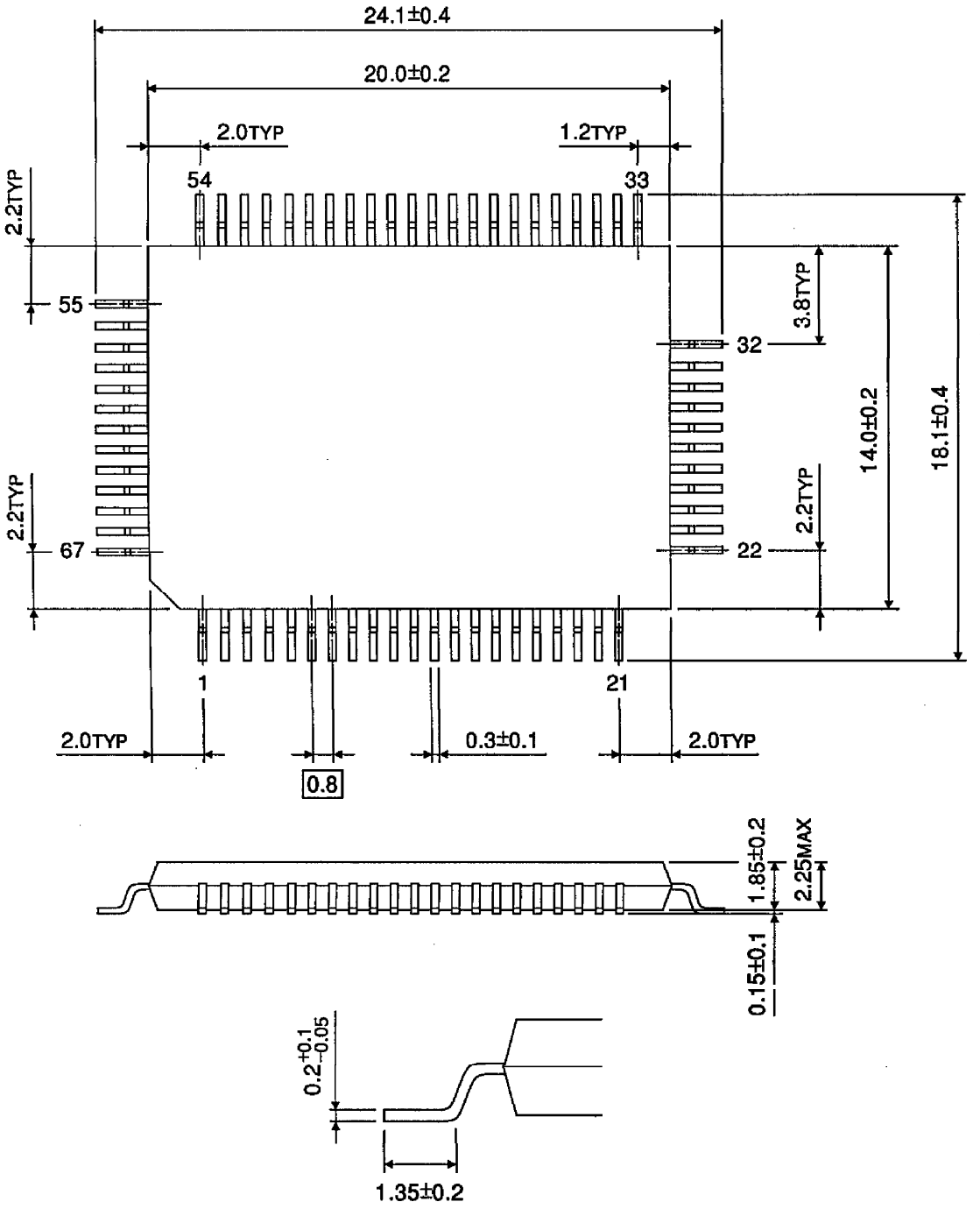


Scribe Line

PAD Pitch 160μm

OUTLINE DRAWING

QFP67-P-1420-0.80 Unit : mm



Weight : 1.20g (Typ.)

GENERAL SPECIFICATION FOR CALCULATOR LSI BARE CHIP

1. Purpose

   This is to specify the quality standard for the integrated circuit produced by TOSHIBA CORPORATION (hereinafter referred as to VENDOR) to be delivered to PURCHASER.

2. Definition

   This specification applies only to the calculator LSI bare chip produced by VENDOR and purchased by PURCHASER and defined the general specification items.

3. Priority of specifications

   When the discrepancies or questions happen to the specifications and instructions provided by VENDOR, the priority shall be ranked as follows.

   1) Individual specification for the calculator LSI bare chip.
      (Both PURCHASER and VENDOR are confirmed by the special sheets.)
   2) General specifications for the calculator LSI bare chip.
   3) Other related specifications and standards.

4. Characteristics

   To be shown in the individual specification sheets.
   The individual specification shall consist of the following 4 items in principle.

   1) Rated specifications.
   2) Electrical characteristics.
   3) Pin configuration & mechanical dimensions.
   4) Others.

5. Inspection of product for delivery

   5.1 Inspection lot

      a) Inspection lot shall consist of products produced by same material under same design, through same production process, and same facilities and assured same quality by same quality assurance method, and lot number shall be put on all trays to be able to trace the lot history.

      b) The quantity of products per Inspection lot shall consist of all the same VENDOR's lot number.

5.2 Sampling plan

Statistical sampling and inspection shall be in accordance with MIL-STD-105D single sampling plans for normal inspections, general inspection level Ⅱ.

The acceptable quality level (AQL) shall be specified in following table :

TEST ITEM	AQL (%)
Electrical	2.5
Visual	4.0

5.3 Electrical criteria

Criteria of Electrical Characteristics are prescribed in Attachment-1.

5.4 Visual criteria

Visual Criteria are prescribed in Attachment-2.

6. Incoming inspection

6.1 General

a) PURCHASER's incoming inspection should be done within 15 days after PURCHASER receives the quantity of products in principle.

b) PURCHASER shall report the results of incoming inspection to VENDOR and provide VENDOR with detailed data in failure rate and items regarding VENDOR's lot number respectively, if VENDOR demands the report from PURCHASER.

6.2 Inspection procedure

PURCHASER should do his incoming inspection according to the following procedure.

a) First : Visual inspection should be done.

b) Next : Electrical and other inspection should be done under condition with bare chip before going into PURCHASER's process.

7. Treatment for defective lot and products

Regarding the defective lot and defective products which are found through PURCHASER's incoming inspection, PURCHASER can be returned to VENDOR with detailed description on failures concerned.
However, if VENDOR cannot receive the defective items within 30 days after PURCHASER's incoming inspection, VENDOR should be able to make no reference to the defective problem.

8. Packing and labeling

a) Dice shall be placed in die tray with the top metalization facting up in order.

b) In principle, a pile consists of 5 trays and several piles are packed in a package. These piles and packages are indicated with printed labels as shown below.

Date	
Name	
Lot No.	
Net	
TOSHIBA MADE IN JAPAN	

c) PURCHASER shall return these packing materials to VENDOR on VENDOR's demand.

9. Storage criteria

Solid state chips, unlike packaged devices, are non-hermetic devices normally fragile and small in physical size, and therefore, require special handling considerations as follows :

9.1 Chips must be stored under proper conditions to insure that they are not subjected to a moist and / or contaminated atmosphere that alter their electrical, physical, or mechanical characteristics.
After the shipping container is opened, the chips must be stored under the following conditions :

A. Storage temperature, 40°C max.
B. Relative humidity, 50% max.
C. Clean, dust-free environment.

9.2 The user must exercise proper care when handling chips or wafers to prevent even the slightest physical damage to the chip.

9.3 During mounting and lead bounding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.

9.4 After the chip has been mounted and bounded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces.
In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

10. Handling criteria

The user should find the following suggested precautions helpful in handling chips.
In any event, because of the extremely small size and fragile nature of chips, care should be taken in handling these devices.

10.1 Grounding

a) Bonders, pellet pickup tools, table tops, trim and form tools, sealing equipment, and other equipment used in chip handling should be properly grounded.

b) Operator should be properly grounded.

10.2 In-process handling

a) Assemblies or subassemblies of chips should be transported and stored in conductive carriers.

b) All external leads of the assemblies or subassemblies should be shorted together.

VISUAL INSPECTION CRITERIA

1. Visual inspection magnification shall be 40 × in principle.
2. Defects defined :

2.1 Thickness

See the technical data sheet.

2.2 Chip and crack

A die shall be rejected if :

a) Any crack of chip extends greater than 35μm in length into the inside of the scribble line. (see Fig.1)

2.3 Metallization

A die shall be rejected if :

a) More than 25% of the designed area of the metallization is missing at any bonding pad.

b) There is a short or break which affects electrical characteristics in any lead pattern. (see Fig.2)

2.4 Glass protection coat

A die shall be rejected if :

a) It exhibits glass protection coat which covers more than 25% of any active bonding pad.

2.5 Attached foreign material

A die shall be rejected if :

a) A die is covered by stains or attached foreign material which size is more than 5 times as large as a bonding pad area.

b) It exhibits residual ink, stains or attached foreign material which covers more than 20% of any active bonding pad. (see Fig.3)

2.6 Others

A die shall be rejected if :

a) There have no evident probed impression on the bonding pads.

b) A inked die, defective die, is intermized.

3. Limit samples should be fized, if necessary.

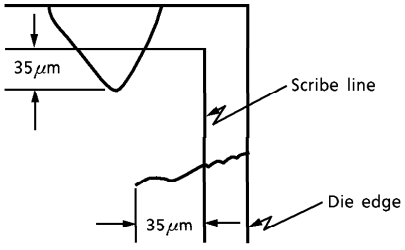


Fig.1

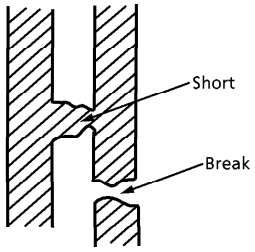


Fig.2 Lead pattern

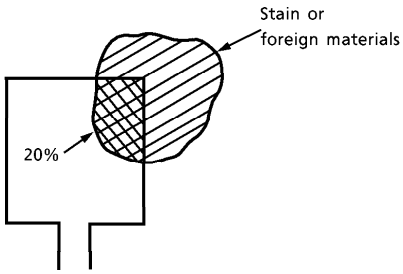
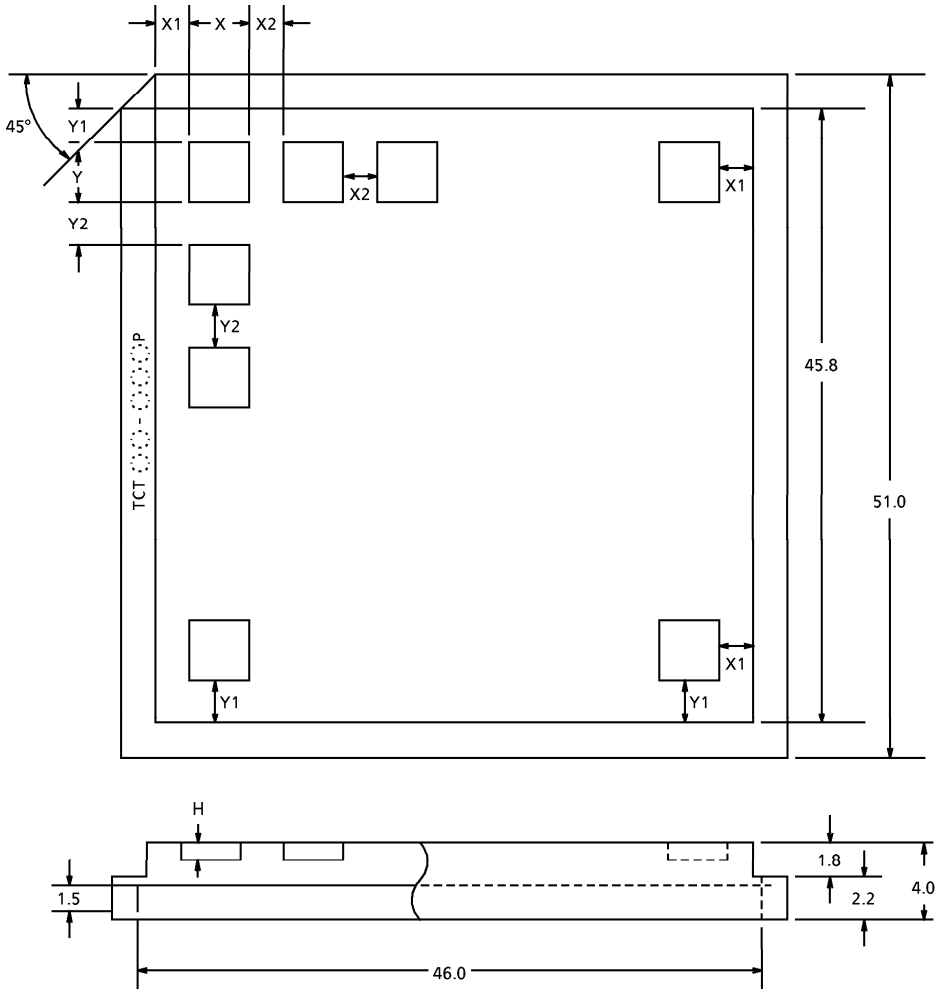


Fig.3

OUTSIDE DIMENSIONS OF CHIP TRAY



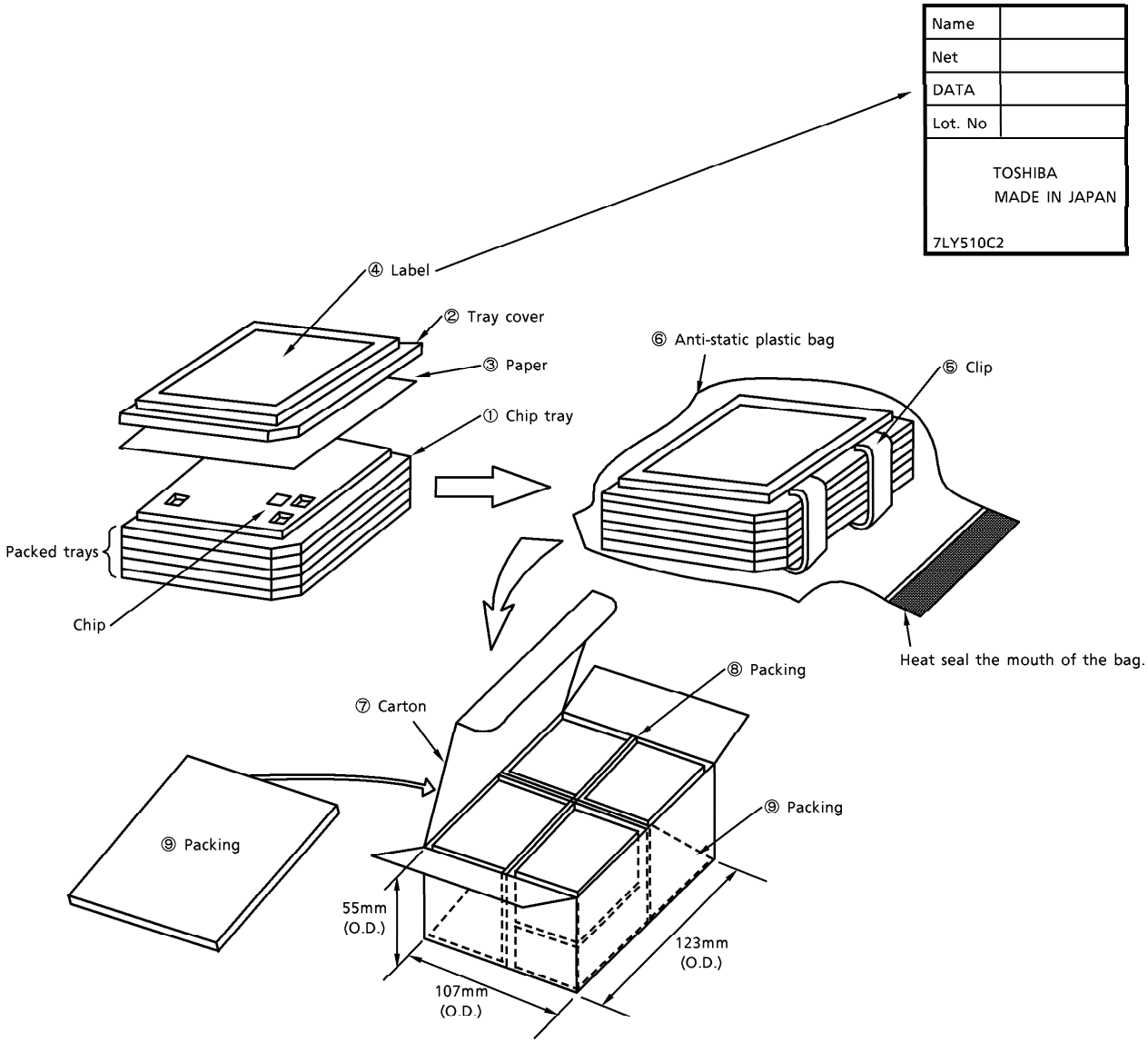
Unit : mm

CHIP NAME	TRAY NAME	X	Y	(H)	No. OF POCKETS	X1	X2	Y1	Y2
JT6A11AX-AS	TCT38-060P	3.80	3.80	0.60	10 × 10 (100)	1.200	0.600	1.200	0.600

Tray material :

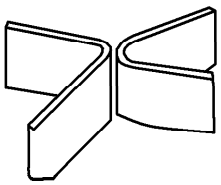
Carbon-containing polypropylene

PACKING METHOD-1



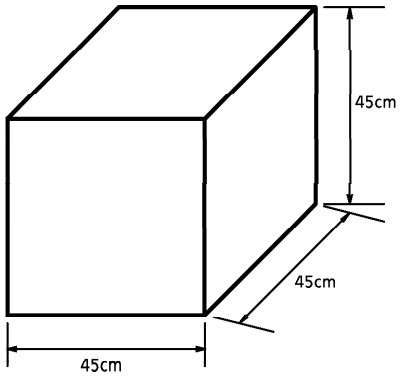
Place eight bags of chip trays in each carton box ⑦. Lay one sheet of packing ⑨ (7UF44F) before closing the lid of the cart box. (See the diagram above.)

Prepare packing ⑧ by cutting 7UF44F into halves and folding each in half as shown below ; use them as inner partitions.



PACKING METHOD-2

Shipping box



- Inner box : Containing 20 boxes
- Weight : Approx. 15kg (including packing material)
- Material : Corrugated cardboard
- IC contents : 36×5×8×20=28.8kpcs.