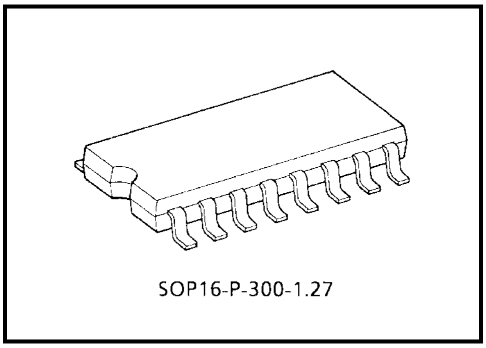
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T6B70BF

Interface IC for Water Heater

The T6B70BF incorporates two-channel 4-bit DA converter, a pseudo sine wave generator and an external analog signal detection/non-detection circuit. It is designed to be used mainly for communication between water heater and control unit.

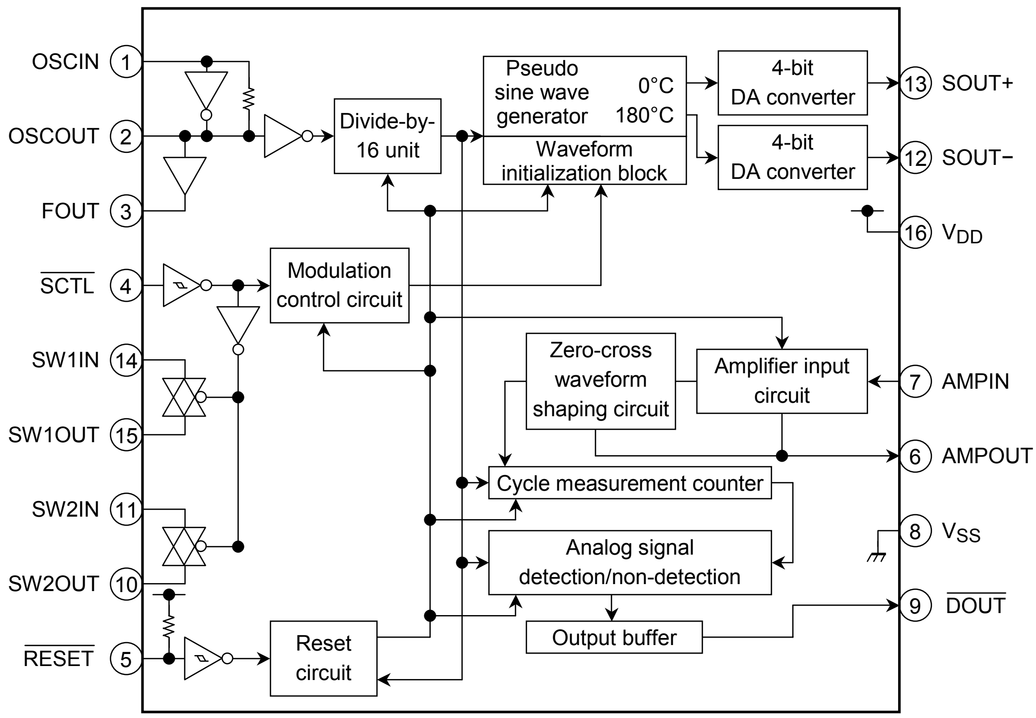


Weight: 0.16 g (typ.)

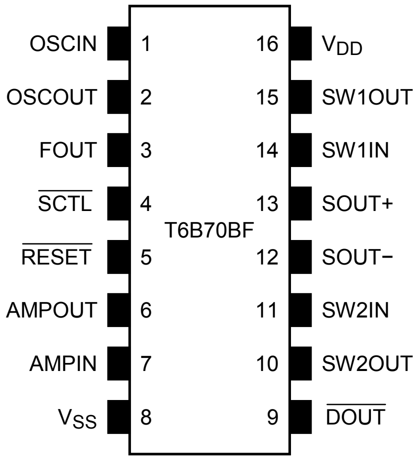
Features

- On-chip two-channel 4-bit DA converter (opposite polarities)
- On-chip pseudo sine wave generator (external clock/16)
- On-chip external analog signal detection/non-detection circuit
- On-chip two-channel analog switch

Block Diagram



Pin Assignment



Pin Function

No.	Symbol	Input/Output	Function
1	OSCIN	Input	Pins connected to oscillation
2	OSCOUT	Output	Pins connected to oscillation
3	FOUT	Output	Output pin for oscillation waveform shaping circuit
4	$\overline{SCTL}$	Input	Modulation control signal input pin
5	$\overline{RESET}$	Input	Reset signal input pin
6	AMPOUT	Output	Amplifier signal output pin
7	AMPIN	Input	Amplifier signal input pin
8	V_{SS}	—	Device GND pin (0 V)
9	$\overline{DOUT}$	Output	Output pin for amplifier input signal detector
10	SW2OUT	Output	Output pin on analog SW2 side
11	SW2IN	Input	Input pin on analog SW2 side
12	SOUT−	Output	Pseudo sine wave (opposite polarity of SOUT+ output) output pin
13	SOUT+	Output	Pseudo sine wave output pin
14	SW1IN	Input	Input pin on analog SW1 side
15	SW1OUT	Output	Output pin on analog SW1 side
16	V_{DD}	—	Device power supply pin (+5 V)

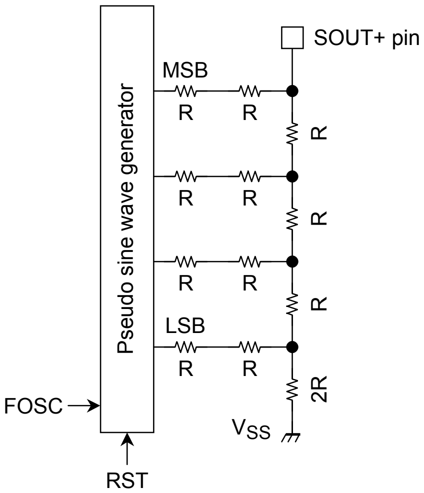
Function Description

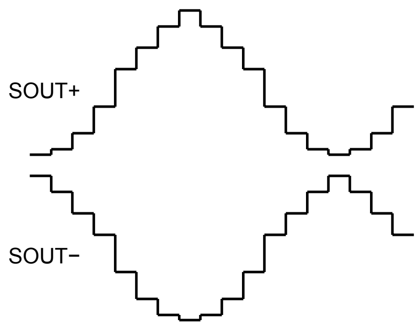
(1) Pseudo sine wave generator and 4-bit DA converters (sending block)

Pseudo sine wave signal with Fosc/16 frequency is driven out from pseudo sine wave output pin (SOUT+ and SOUT−).

The outputs of pins SOUT+ and SOUT− have the opposite polarities.

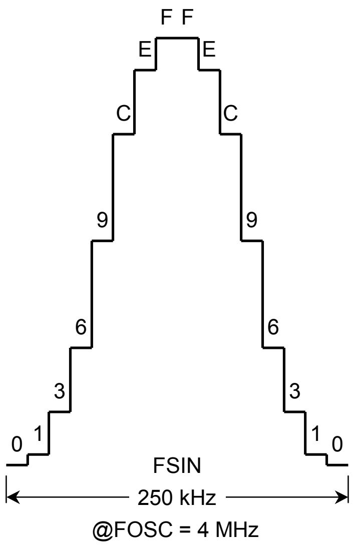
The block of pseudo sine wave generator and 4-bit DA converter (the side of SOUT+ pin) are shown below.





The data of pseudo sine wave generator is driven out in the following sequence.

0 → 1 → 3 → 6 → 9 → C → E → F → F → E → C → 9 → 6 → 3 → 1 → 0 (in hexadecimal)



Thus, the pseudo sine waveform of positive-going and negative-going outputs is like a staircase at no load.

An analog switch is incorporated so that the driver output buffer is connected to the transmission line only when transmission is performed.

However, an emitter follower circuit is externally connected to the driver output buffer.

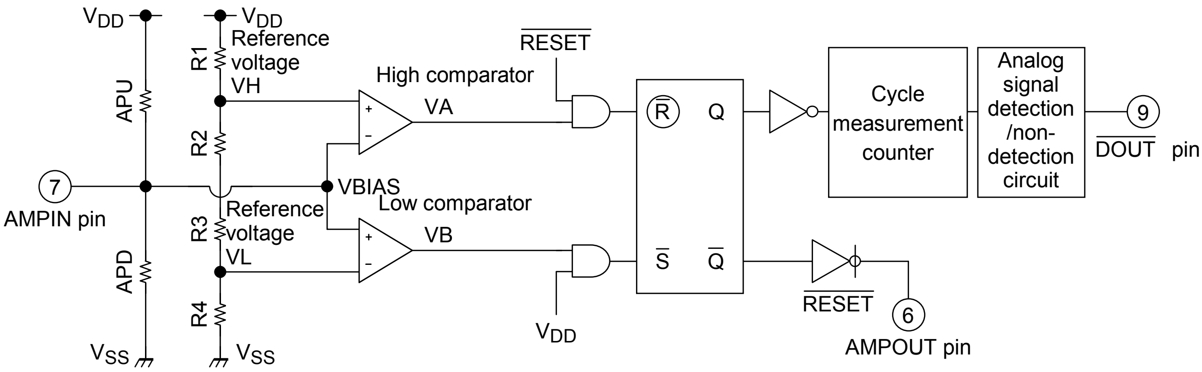
The phase difference between positive-going and negative-going outputs is within 180° ± 5°. (pseudo sine wave output phase fluctuation)

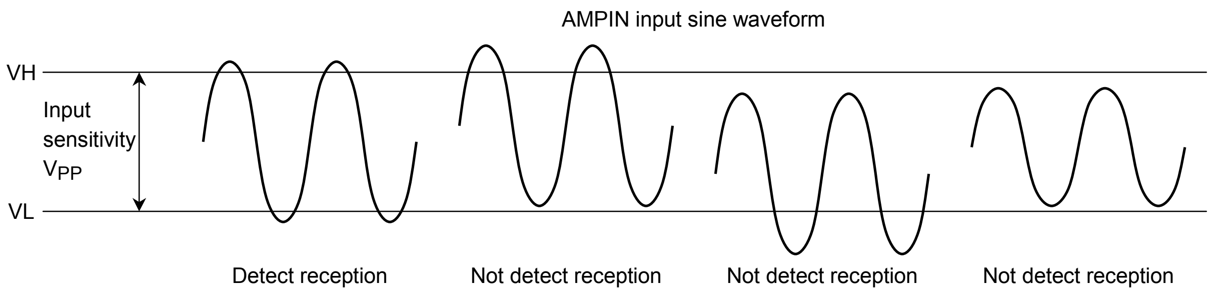
(2) Amplifier input circuit and signal detection/non-detection circuit (receiving block)

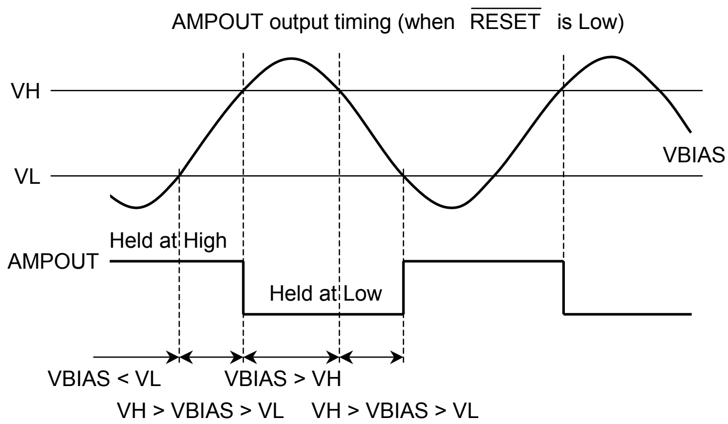
The modulation signal input block incorporates two level comparators having a high and a low threshold values to detect the external sine wave signal with amplitude higher than the specified threshold. Thus, it avoids signals with amplitude lower than the specified threshold (e.g., noise signals) being detected erroneously.

The detection frequency range (frequency window) is determined by the divider ratio 1/18 to 1/14 of Fosc.

In detection/non-detection determined condition, when the signals within the specified frequency range are detected (or not detected) sequentially, signals are controlled using the majority rule. The time which detection/non-detection is determined takes 9 to 15 waves to pass when one wave is referenced to Fosc/16 frequency.







AMPOUT Truth Table

	VA	VB	AMPOUT
VBIAS > VH	L	H	L
VH > VBIAS > VL	H	H	Hold
VBIAS < VL	H	L	H

(3) Function description and timing chart of the sending block

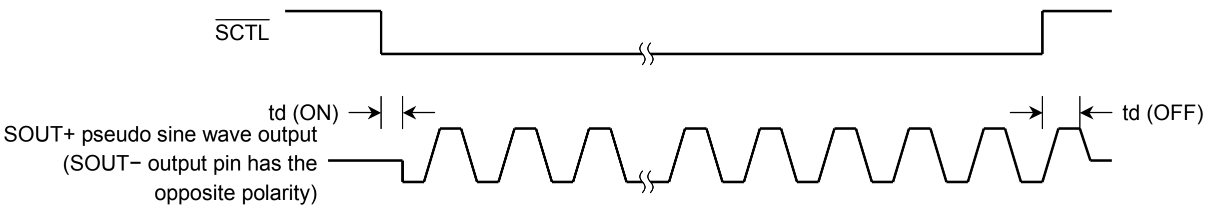
When modulation control input ($\overline{SCTL}$) is in High-level, pseudo sine wave output is held at 0° of the phase angle of pseudo sine wave. When modulation control input changes from High-level to Low-level, the pseudo sine wave output (SOUT+) starts from −90° (SOUT− starts from +90°).

In this case, the time which takes to turn ON is as follows.

td (ON) < 500 ns

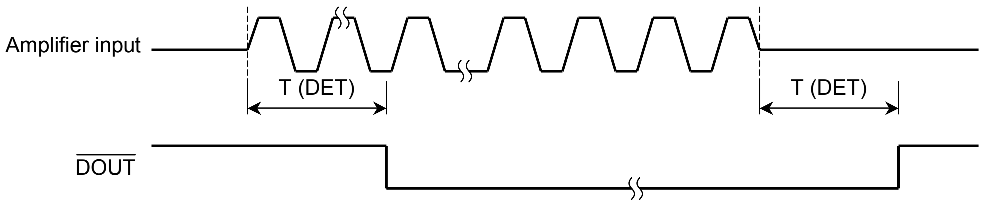
When modulation control input changes from Low-level to High-level, the phase angle is forcibly held at 0°, regardless of the phase of the pseudo sine wave output. (the pseudo sine wave output is stopped). In this case, the time which takes to turn OFF is as follows.

td (OFF) < 1 μs



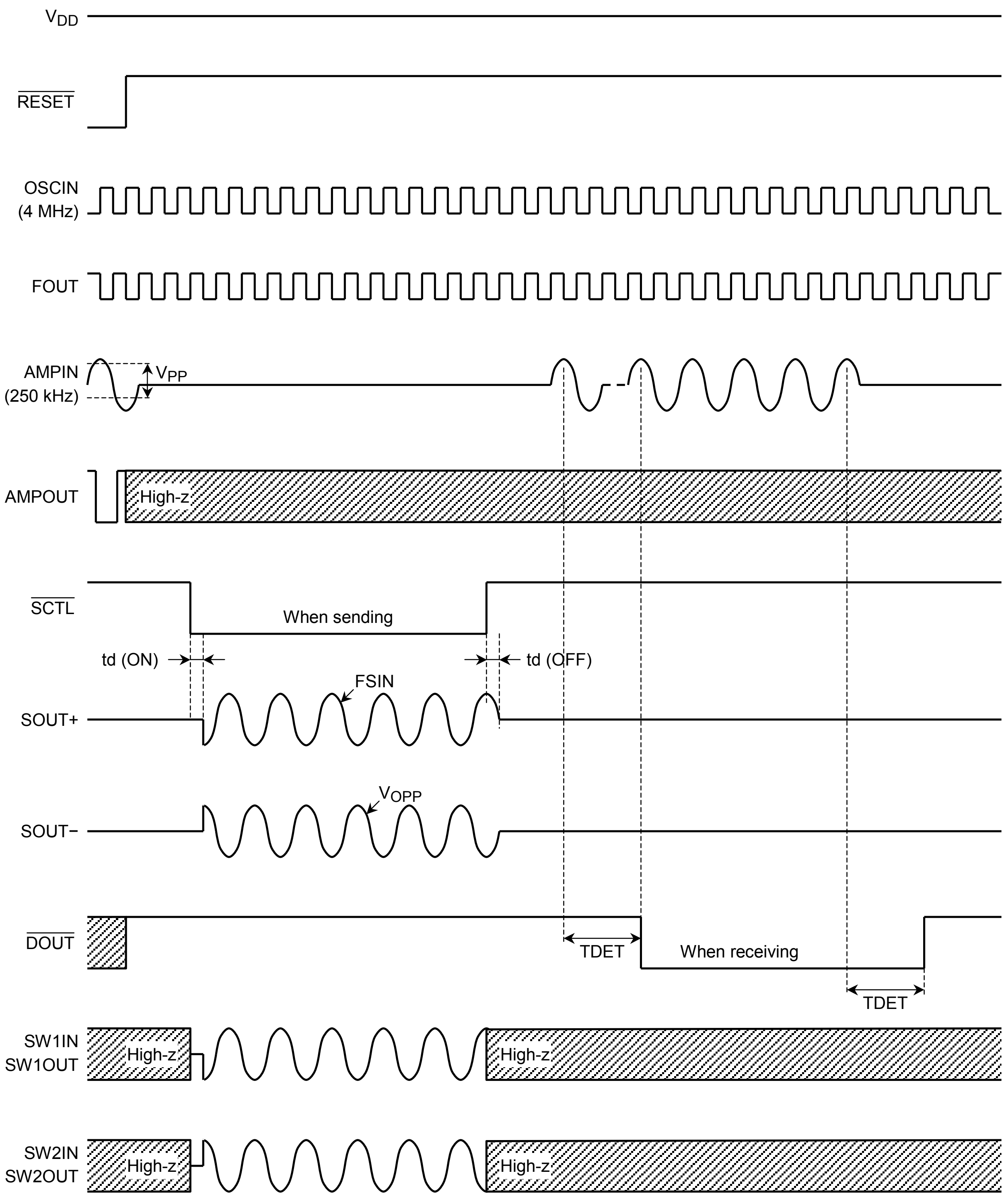
(4) Function description and timing chart of the receiving block

When it is ready to receive amplifier input signal, the time T (DET) which takes to change from High to Low at $\overline{DOUT}$ pin is within the time which 9 to 15 waves to pass. In this case, one wave is referenced to 16 Fosc clocks. The time width is determined by the internal clock and amplifier input signal. The timings of the internal clock and internal detection signal in the majority logic circuit are synchronous with each other. When input signals with the cycle, which is within the range specified by the frequency window, are detected (or not detected) sequentially, this rule is valid (the majority rule).



Note 1: Any communication protocol is used, however, it takes 15 carrier waves to pass when the signal changes its state.

Timing Chart (SOUT+ = SW1IN, SW1OUT, SOUT− = SW2IN, SW2OUT)



Maximum Ratings (Ta = 25°C ± 1.5°C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 to 6.0	V
Input voltage	VI	−0.3 to V_{DD} + 0.3	V
Input peak current	IIK	−20 to 20	mA
Operating temperature	T_{opr}	−20 to 80	°C
Storage temperature	T_{stg}	−55 to 125	°C
Power dissipation	P_D (Note 1)	0.54	W

Note 1: Decreases approximately 4.35 mW per 1°C.

Electrical Characteristics
(unless otherwise specified, V_{DD} = 5.0 V, V_{SS} = 0 V, FOSC = 4 MHz and Ta = −20 to 80°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
V_{DD} pin (pin 16)								
Operating voltage		V_{DD}	—	—	4.5	5.0	5.5	V
Current consumption		I_{DD}	1	No load, Fosc = 4 MHz	—	—	10	mA
OSCIN pin (pin 1) and OSCOUT pin (pin 2)								
Oscillation frequency		FOSC	2	—	1	4	10	MHz
Input voltage	High level	VIHOSC	3	—	0.7 V_{DD}	—	V_{DD}	V
	Low level	VILOSC	3	—	V_{SS}	—	0.3 V_{DD}	
Input current	High level	IIHROSC	4	VIN = 5 V, Ta = 25°C	3.2	6.58	13.2	μA
	Low level	IILROSC	4	VIN = 0 V, Ta = 25°C	−3.2	−6.58	−13.2	
Output voltage	High level	VOHOSC	3	IOH = −0.1 mA	V_{DD} − 1.0	—	V_{DD}	V
	Low level	VOLOSC	4	IOL = +0.1 mA	V_{SS}	—	V_{SS} + 0.6	
$\overline{\text{RESET}}$ pin (pin 5)								
Low to High input switching level		VIHRST	5	—	0.65 V_{DD}	—	V_{DD}	V
High to Low input switching level		VILRST	5	—	V_{SS}	—	0.35 V_{DD}	V
High-level input current		IIHRST	6	VIN = V_{DD}	−10	—	10	μA
Pull-up resistance 1		IILRRST1	7	VIN = V_{SS}, Ta = 25	9	15	21	kΩ
Pull-up resistance 2		IILRRST2	7	VIN = V_{SS}, Ta = −20 to 80	6.3	—	27.3	kΩ
$\overline{\text{SCTL}}$ pin (pin 4)								
Low to High input switching level		VIHSCTL	8	—	0.65 V_{DD}	—	V_{DD}	V
High to Low input switching level		VILSCTL	8	—	V_{SS}	—	0.35 V_{DD}	V
Input current	High level	IIHSCTL	9	VIN = V_{DD}	−1	—	1	μA
	Low level	IILSCTL	9	VIN = V_{DD}	−1	—	1	
FOUT pin (pin 3)								
Output voltage	High level	VOHFOUT	10	IOH = −1.0 mA	V_{DD} − 1.0	—	V_{DD}	V
	Low level	VOLFOUT	11	IOL = +1.0 mA	V_{SS}	—	V_{SS} + 0.6	

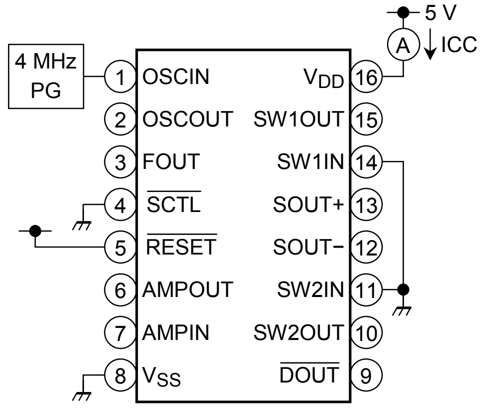
Note 2: One direction in which current flow into the IC should be + (sink) and the other direction in which current flow out from the IC should be − (drain).

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
$\overline{\text{DOUT}}$ pin (pin 9)								
Output voltage	High level	VOHDOUT	12	IOH = −1.0 mA	V_{DD} − 1.0	—	V_{DD}	V
	Low level	VOLDOUT	13	IOL = +1.0 mA	V_{SS}	—	V_{SS} + 0.6	V
Non-reception to reception detection time		TDET1	19	Fosc = 4 MHz, AMPIN = 250 kHz Time which takes $\overline{\text{DOUT}}$ to change from High to Low	40	—	60	μs
Reception to non-reception detection time		TDET2	19	Fosc = 4 MHz, AMPIN = 250 kHz Time which takes $\overline{\text{DOUT}}$ to change from Low to High	36	—	56	μs
AMPIN pin (pin 7)								
Input dynamic range		VAMPIN	14	—	V_{SS}	—	V_{DD}	V
Pull-up resistance 1		IILRAPU1	15	VIN = V_{SS}, Ta = 25	11.6	19.4	27.2	kΩ
Pull-up resistance 2		IILRAPU2	15	VIN = V_{SS}, Ta = −20 to 80	7	—	38	kΩ
Pull-down resistance 1		IIHRAPD1	16	VIN = V_{DD}, Ta = 25	5.9	9.8	13.7	kΩ
Pull-down resistance 2		IIHRAPD2	16	VIN = V_{DD}, Ta = −20 to 80	3	—	19.2	kΩ
Amplifier input bias voltage		VBIAS	17	No load (design goal)	1.54	1.63	1.71	V
Amplifier input sensitivity		V_{PP}	18	No load, receivable amplitude range is 250 kHz, when sine wave signal is applied. (design goal)	0.3	—	0.45	V
Detection frequency range		DETON	19	Fosc = 4 MHz	236	—	266	kHz
Non-detection frequency (low frequency)		DETOFF1	19	Fosc = 4 MHz	—	—	222	kHz
Non-detection frequency (high frequency)		DETOFF2	19	Fosc = 4 MHz	286	—	—	kHz
SW1IN pin (pin 14) and SW1OUT pin (pin 15)								
Analog switch input voltage		VINASW1	—	—	V_{SS}	—	V_{DD}	V
Analog switch output voltage		VOUTASW1	—	—	V_{SS}	—	V_{DD}	V
OFF-leak current of analog switch 1		IOFFASW1	20	$\overline{\text{SCTL}}$ = H, SW1IN = V_{DD}, SW1OUT = V_{SS}	−1	—	1	μA
ON-resistance of analog switch 1		RONASW1	21	$\overline{\text{SCTL}}$ = L, SW1IN = 5 V, SW1OUT = 0 V Current measure	35	—	105	Ω
SW2IN pin (pin 11) and SW2OUT pin (pin 10)								
Analog switch input voltage		VINASW2	—	—	V_{SS}	—	V_{DD}	V
Analog switch output voltage		VOUTASW2	—	—	V_{SS}	—	V_{DD}	V
OFF-leak current of analog switch 2		IOFFASW2	20	$\overline{\text{SCTL}}$ = H, SW2IN = V_{DD}, SW2OUT = V_{SS}	−1	—	1	μA
ON-resistance of analog switch 2		RONASW2	21	$\overline{\text{SCTL}}$ = L, SW2IN = 5 V, SW2OUT = 0 V Current measure	35	—	105	Ω
SOUT+ pin (pin 13) and SOUT− pin (pin 12)								
Output voltage		V_{OPP}	22	Maximum voltage value at no load	0.85 V_{DD}	—	V_{DD}	V
Pseudo sine wave output frequency		FSIN	23	FOSC = 4 MHz	—	250	—	kHz
Pseudo sine wave output start time		tdON	23	$\overline{\text{SCTL}}$ = H → L	—	—	500	ns
Pseudo sine wave output stop time		tdOFF	23	$\overline{\text{SCTL}}$ = L → H	—	—	1	μs
Equivalent output impedance		ROUTSIN	24	No load	2.8	4	5.2	kΩ

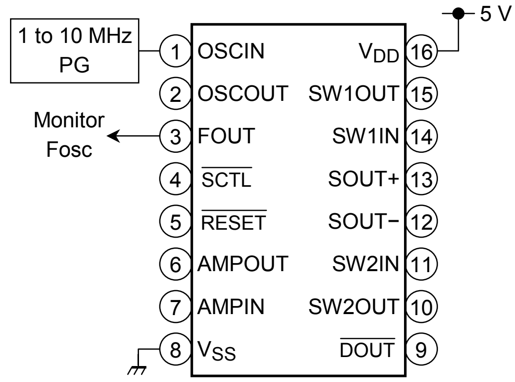
Note: One direction in which current flow into the IC should be + (sink) and the other direction in which current flow out from the IC should be − (drain).

Test Circuit

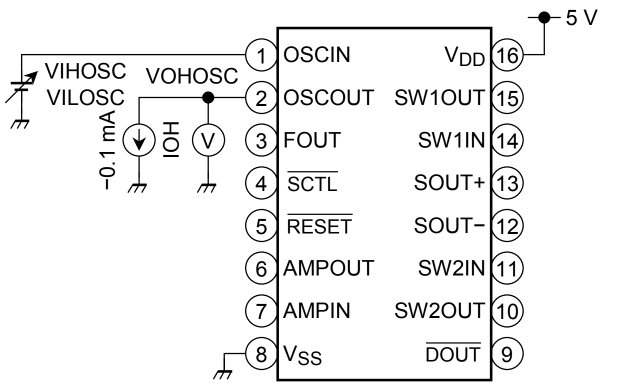
(1) Current consumption



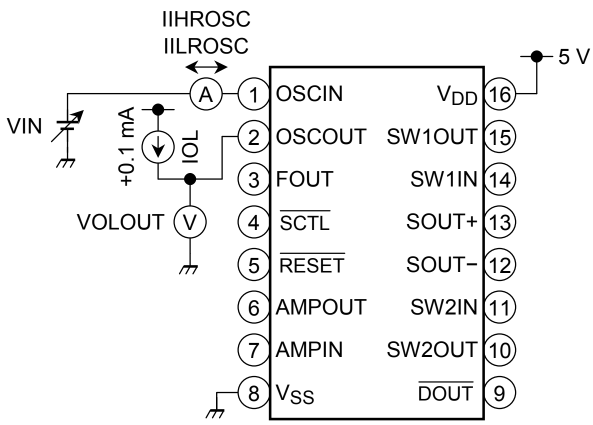
(2) Oscillation frequency



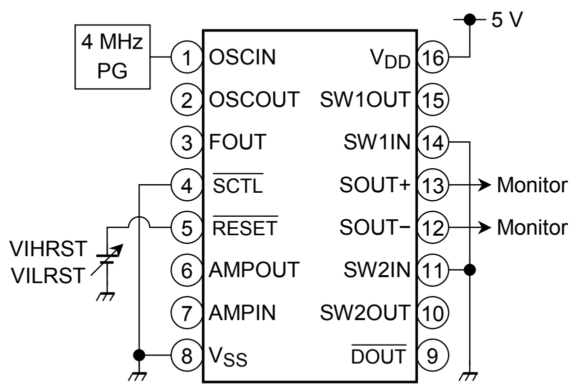
(3) High-level input voltage
Low-level input voltage
High-level output voltage



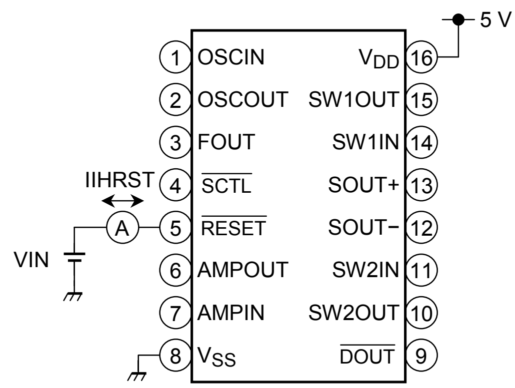
(4) High-level input current
Low-level input current
Low-level output voltage



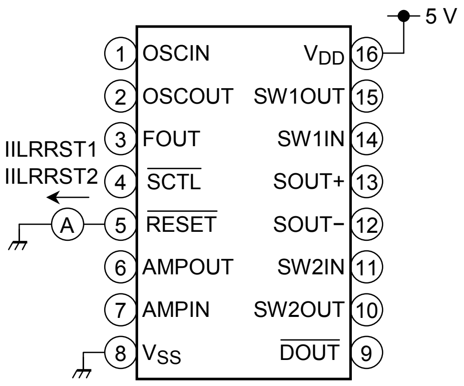
(5) Low to High input switching level
High to Low input switching level



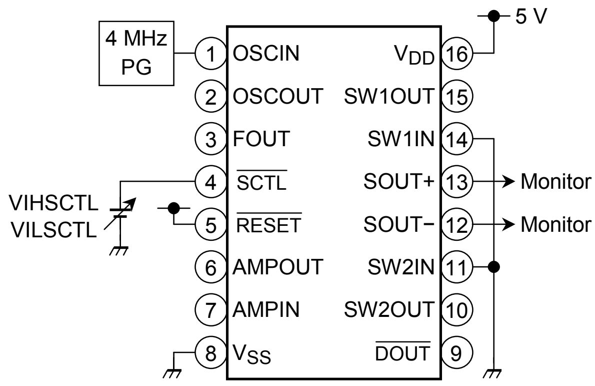
(6) High-level input current



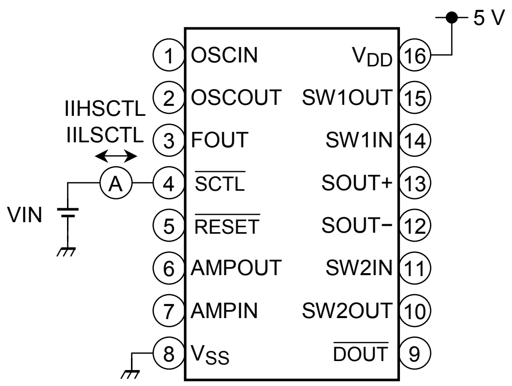
(7) Pull-up resistance 1
Pull-up resistance 2



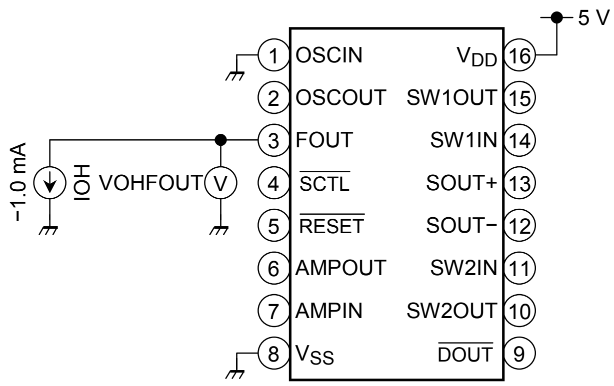
(8) Low to High input switching level
High to Low input switching level



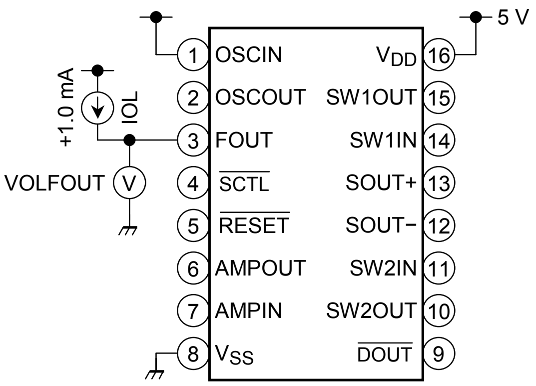
(9) High-level input current
Low-level input current



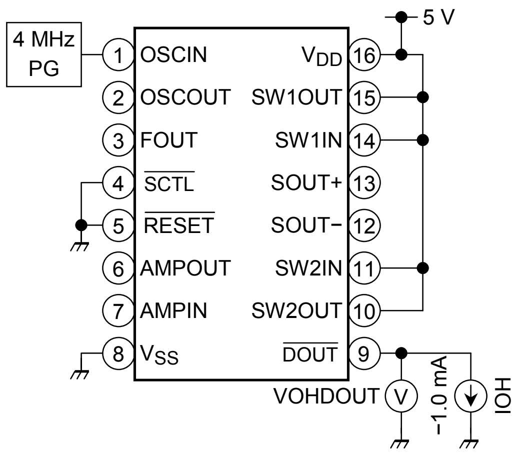
(10) High-level output voltage



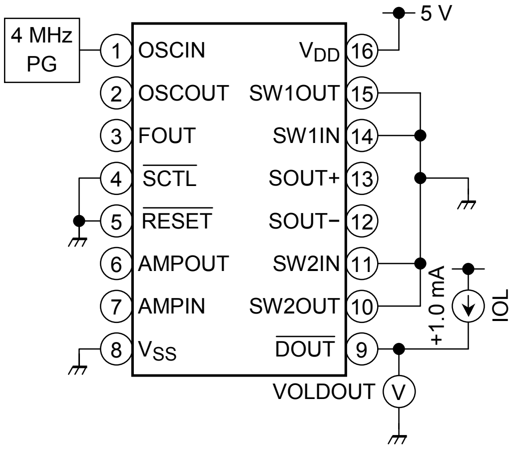
(11) Low-level output voltage



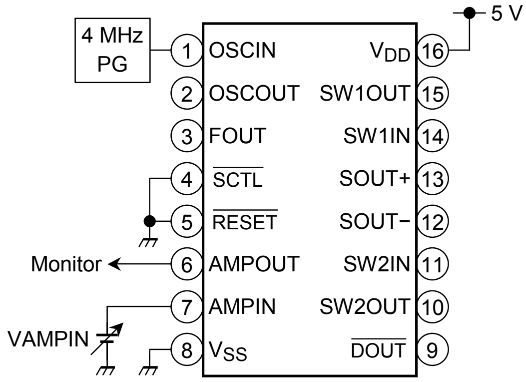
(12) High-level output voltage



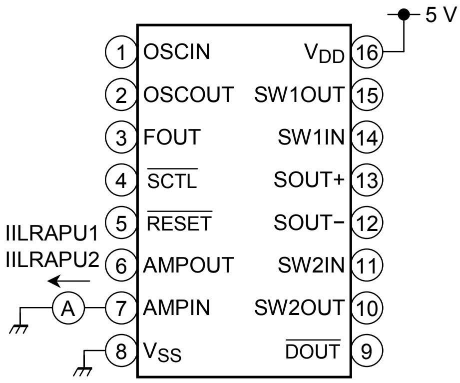
(13) Low-level output voltage



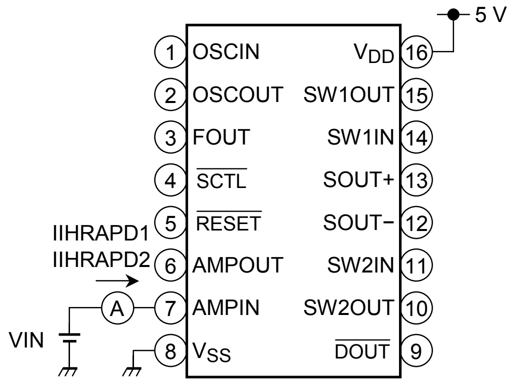
(14) Input dynamic range



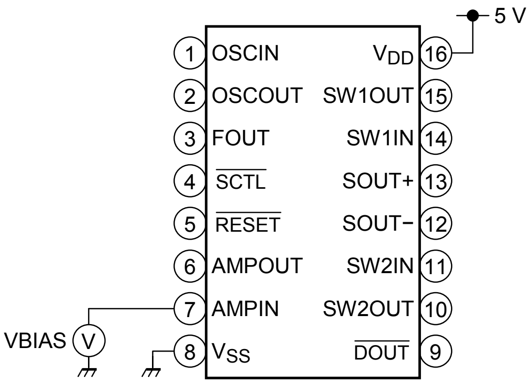
(15) Pull-up resistance 1
Pull-up resistance 2



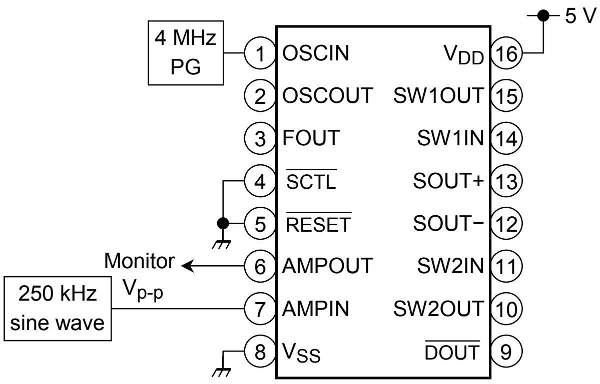
(16) Pull-down resistance 1
Pull-down resistance 2



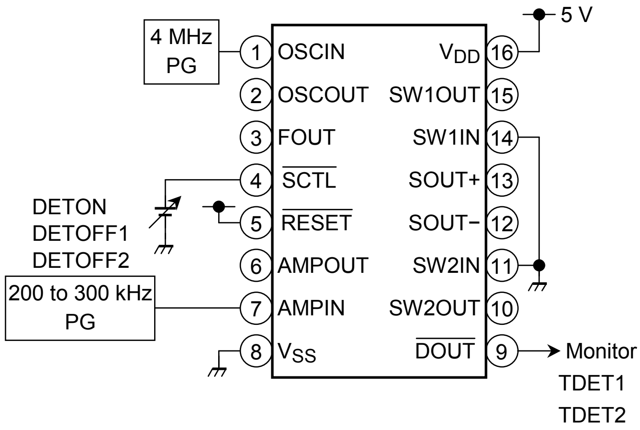
(17) Amplifier input bias voltage



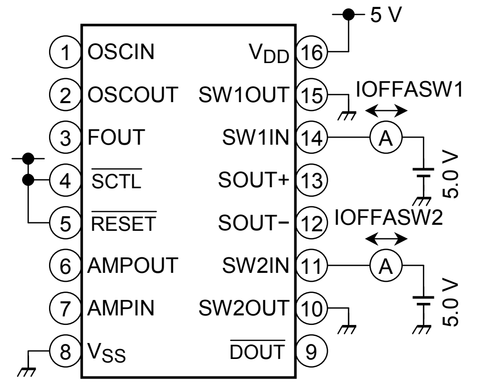
(18) Amplifier input sensitivity



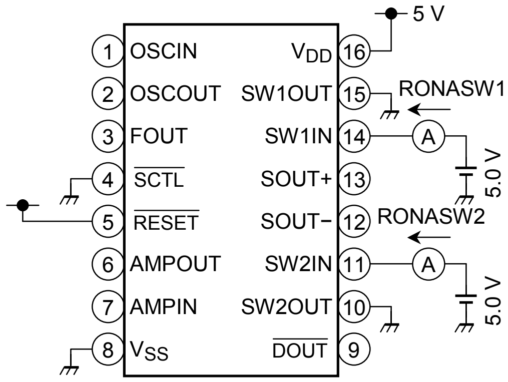
(19) Detection frequency range
Non-detection frequency (low frequency)
Non-detection frequency (high frequency)
Non-reception to reception detection time
Reception to non-reception detection time



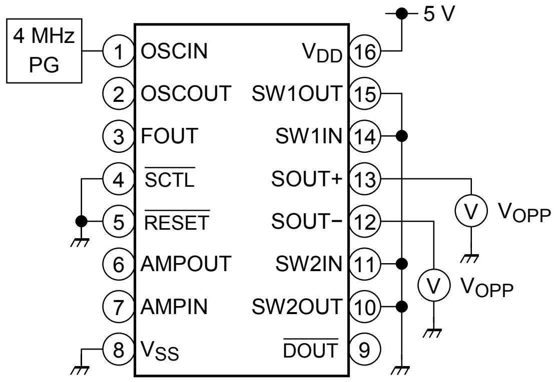
(20) OFF-leak current of analog switch 1
OFF-leak current of analog switch 2



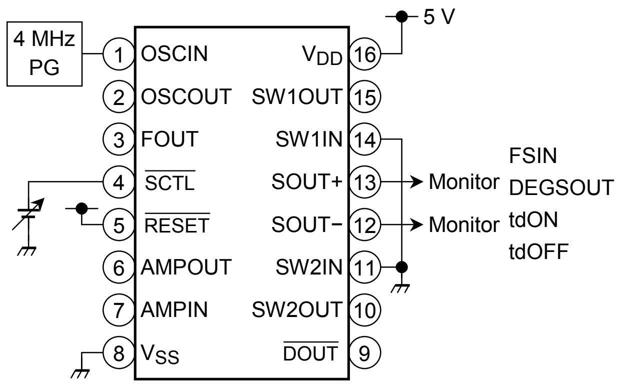
(21) ON-resistance of analog switch 1
ON-resistance of analog switch 2



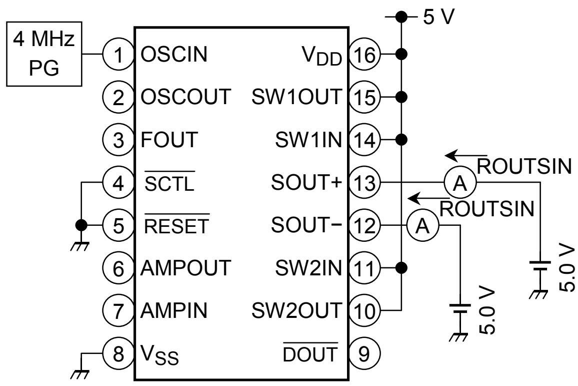
(22) Output voltage



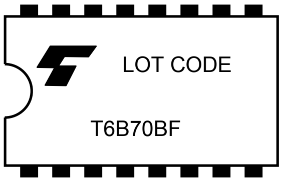
(23) Pseudo sine wave output frequency
Pseudo sine wave output start time
Pseudo sine wave output stop time



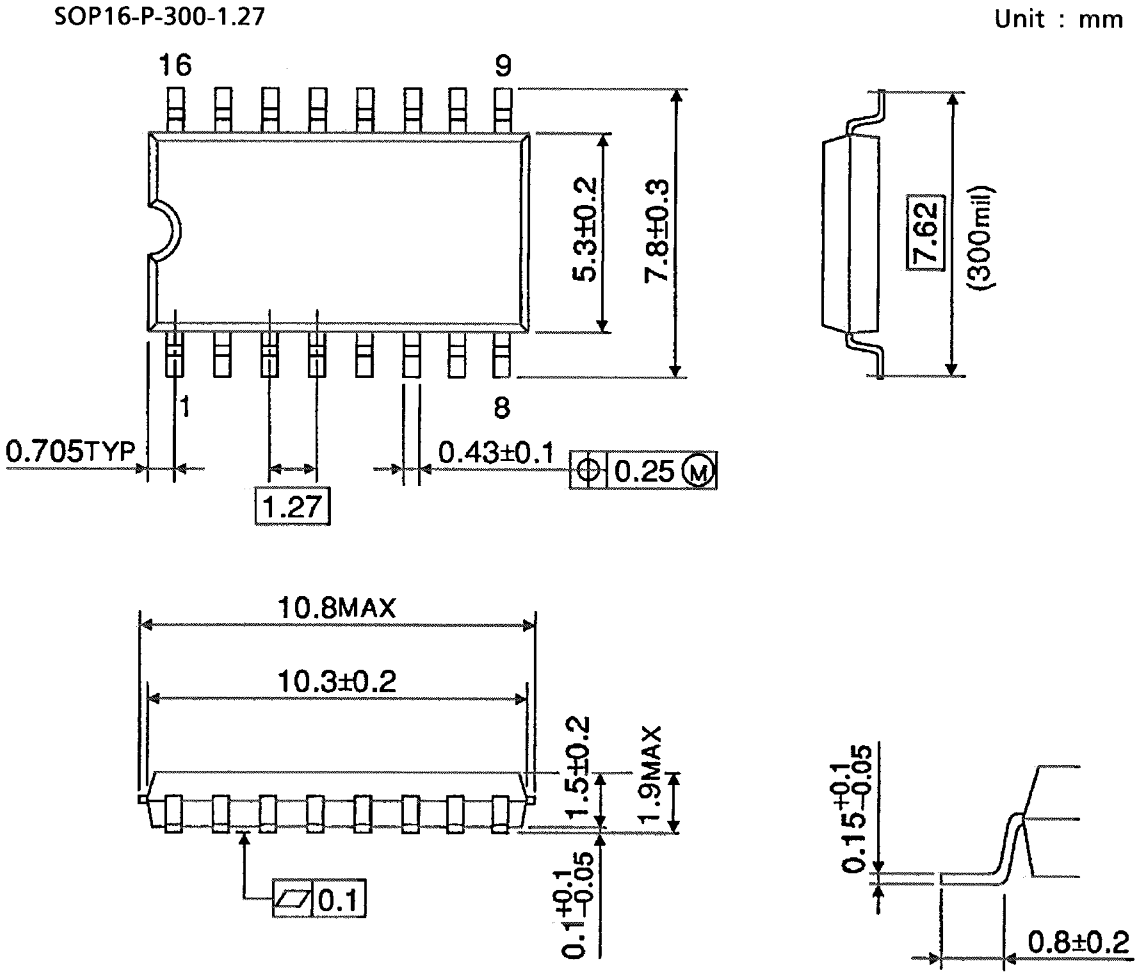
(24) Equivalent output impedance



Markings



Package Dimensions



Weight: 0.16 g (typ.)

RESTRICTIONS ON PRODUCT USE

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