75 Ω VIDEO LINE DRIVER

FEATURES

- **Internal Y-C Summing Circuit**
- **Internal Switch Circuit for Composite Signal or Y-C Signal**
- **Voltage Gain is 6 dB Fixed**
- **Internal 75 Ω Driver**
- **Very Small Output Capacitor Using SAG Function Pin**
- **Very Small Package (SOT23L-8)**

APPLICATIONS

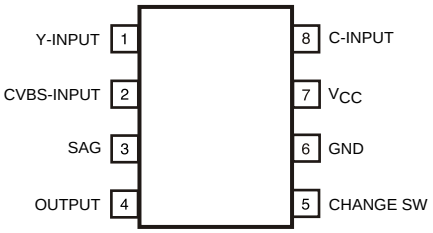
- **Video Equipment**
- **Camcorder**
- **CCD Cameras**
- **DVD Player/RW**
- **Video Board**
- **Video Tape Recorders**
- **LCD TV/Monitor**

DESCRIPTION

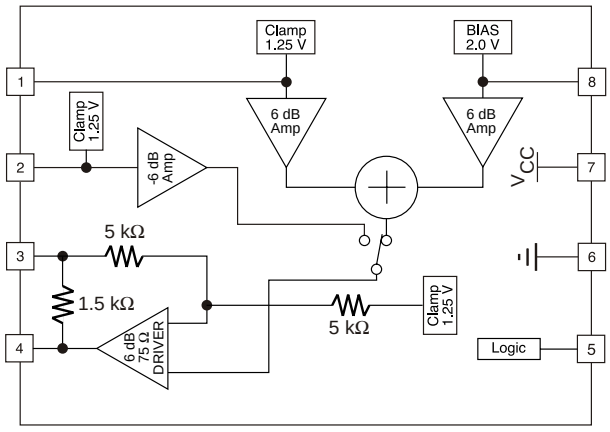
Operating from a single +5 V supply, the TK15414M is a 75 Ω video line driver IC with an internal Y-C summing circuit. It has an internal switch circuit for the CVBS compostie signal and the Y-C signal. The internal 1.5 k SAG function resistor provides gain compensation for low frequency signals. (Voltage gain from the CVBS signal input terminal is 0 dB.)

The TK15414M is available in the very small SOT23L-8 surface mount package.

TK15414



BLOCK DIAGRAM



ORDERING INFORMATION

TK15414M □□

Tape/Reel Code

TAPE/REEL CODE
TL: Tape Left

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 6 V
Operating Voltage Range..... 4.5 to 5.5 V
Power Dissipation (Note 1) ..... 200 mW
Maximum Input Frequency..... 20 MHz
Storage Temperature Range ..... -55 to +150 °C
Operating Temperature Range .....-25 to +75 °C

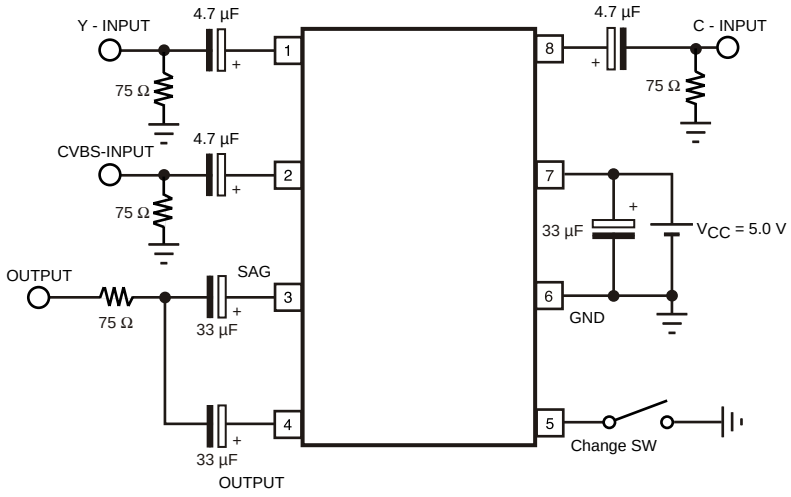
TK15414M ELECTRICAL CHARACTERISTICS

Test conditions: V_{CC} = 5.0 V, V_{IN} = 1.0 V_{P-P}, R_L = 150 Ω, T_A = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Supply Current	No input		24.5	36.0	mA
$V_{THL(SW)}$	Switch Threshold Voltage (High to Low)	Pin 5, S-VHS to CVBS			0.3	V
$V_{TLH(SW)}$	Switch Threshold Voltage (Low to High)	Pin 5, CVBS to S-VHS	1.8			V
S-VHS (Pin 5 OPEN)						
V_{CMP}	Clamp Voltage	Pin 1, Y signal input terminal	1.10	1.28	1.50	V
V_{BIAS}	Bias Voltage	Pin 8, C signal input terminal	1.70	2.00	2.30	V
GVA-Y	Voltage Gain, Y channel	f_{IN} = 1 MHz, Y signal input	5.2	5.7	6.2	dB
GVA-C	Voltage Gain, C channel	f_{IN} = 1 MHz, C signal input	5.1	5.6	6.1	dB
DG-S	Differential Gain	Staircase signal input	-3.0	-1.5	+3.0	%
DP-S	Differential Phase	Staircase signal input	-3.0	0.0	+3.0	deg
fr-S	Frequency Response	f_{in} = 1 MHz / 5 MHz		-0.5		dB
CVBS (Pin 5 GND)						
V_{CMP}	Clamp Voltage	Pin 2, CVBS input terminal	1.10	1.28	1.50	V
GVA	Voltage Gain	f_{IN} = 1 MHz	-0.9	-0.4	-0.1	dB
DG	Differential Gain	Staircase signal input	-3.0	-0.7	+3.0	%
DP	Differential Phase	Staircase signal input	-3.0	0.2	+3.0	deg
fr	Frequency Response	f_{in} = 1 MHz / 5 MHz		-0.5		dB

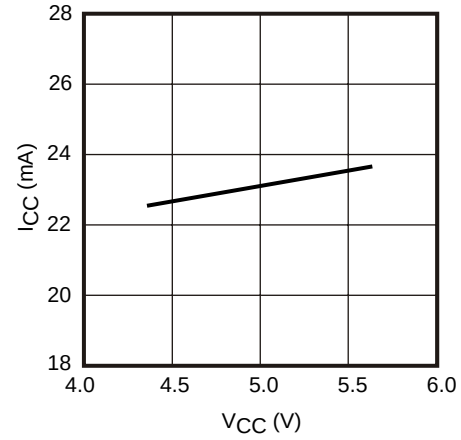
Note 1: Power dissipation is 200 mW in free air. Derate at 1.6 mW/°C for operation above 25°C.

TEST CIRCUIT

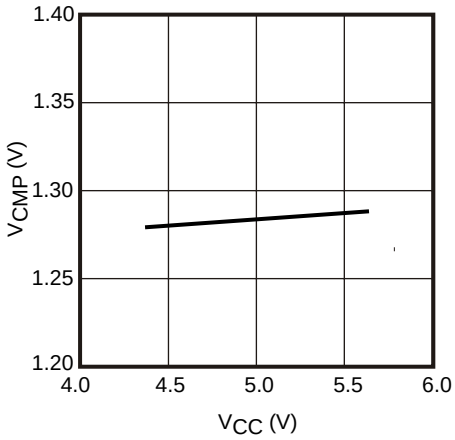


TYPICAL PERFORMANCE CHARACTERISTICS

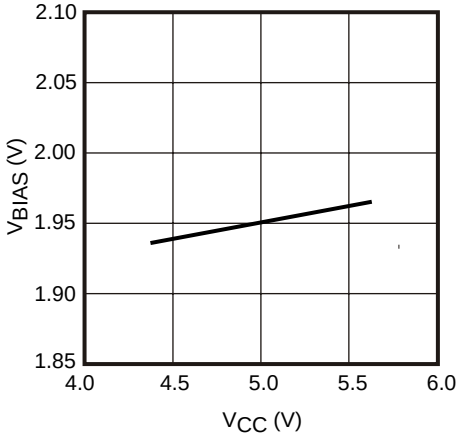
SUPPLY CURRENT vs. SUPPLY VOLTAGE



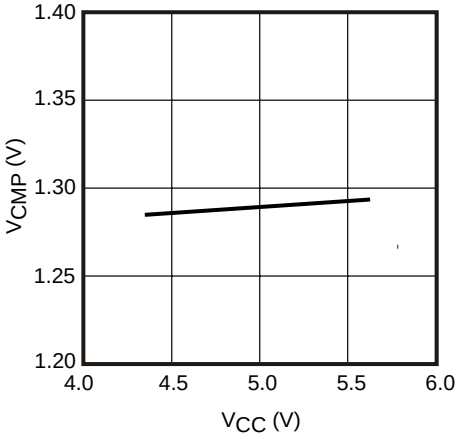
Y-INPUT CLAMP VOLTAGE vs. SUPPLY VOLTAGE



C-INPUT BIAS VOLTAGE vs. SUPPLY VOLTAGE

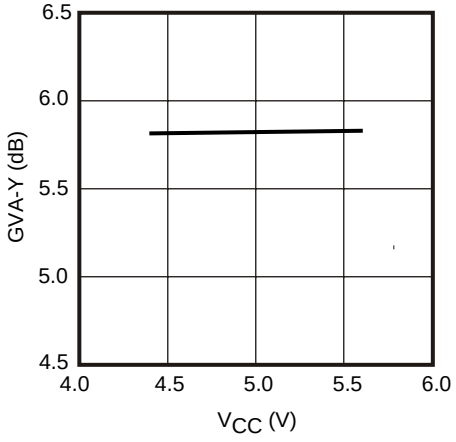


CVBS INPUT CLAMP VOLTAGE vs. SUPPLY VOLTAGE

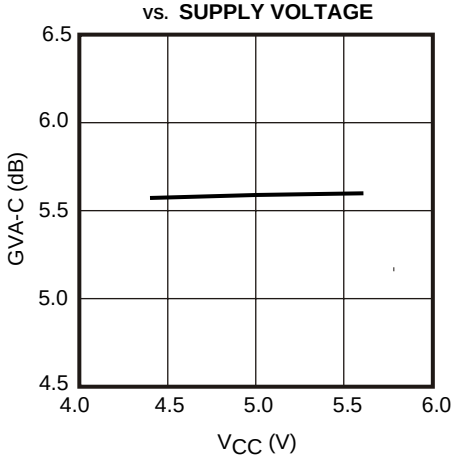


TYPICAL PERFORMANCE CHARACTERISTICS

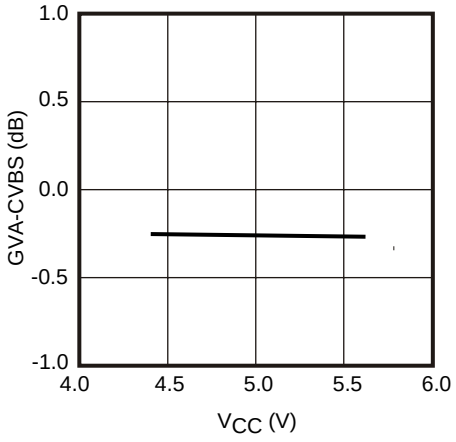
Y-CHANNELVOLTAGE GAIN vs. SUPPLY VOLTAGE



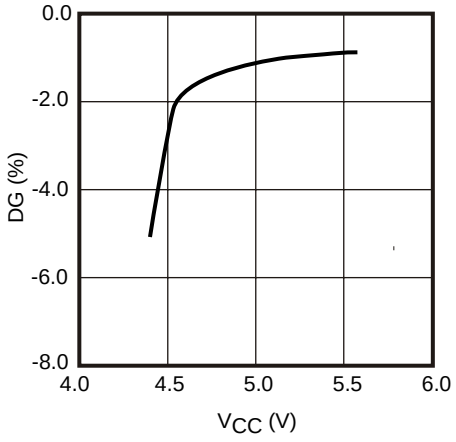
C-CHANNEL VOLTAGE GAIN vs. SUPPLY VOLTAGE



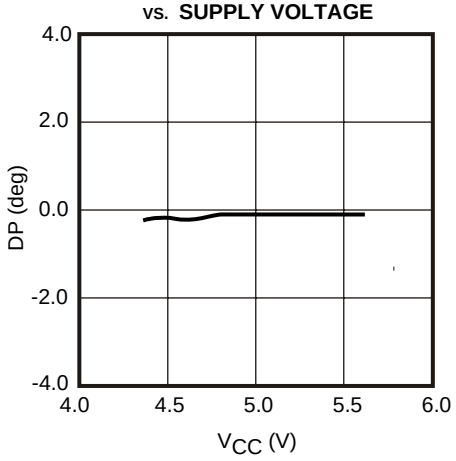
CVBS CHANNEL VOLTAGE GAIN vs. SUPPLY VOLTAGE



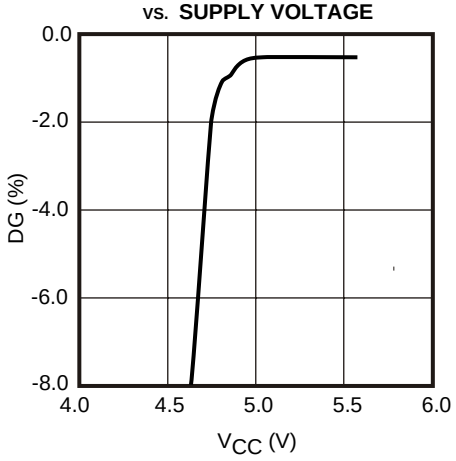
S-VHS DIFFERENTIAL GAIN vs. SUPPLY VOLTAGE



S-VHS DIFFERENTIAL PHASE vs. SUPPLY VOLTAGE

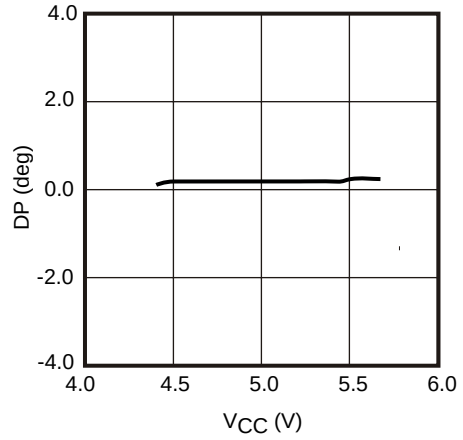


CVBS DIFFERENTIAL GAIN vs. SUPPLY VOLTAGE

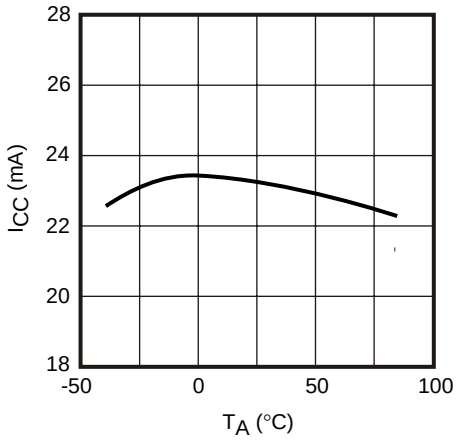


TYPICAL PERFORMANCE CHARACTERISTICS

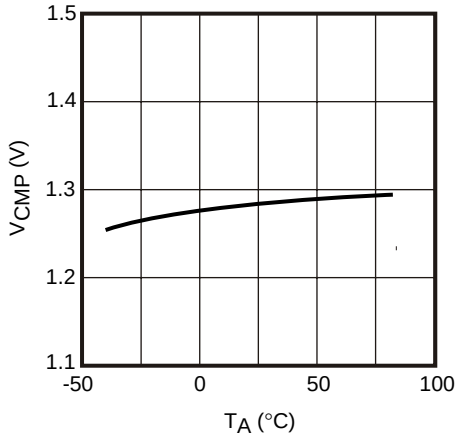
CVBS DIFFERENTIAL PHASE vs. SUPPLY VOLTAGE



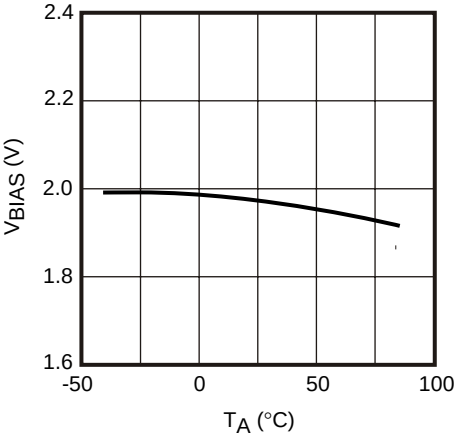
SUPPLY CURRENT vs. TEMPERATURE



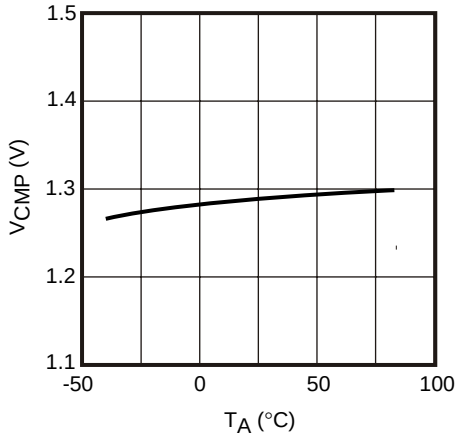
Y-INPUT CLAMP VOLTAGE vs. TEMPERATURE



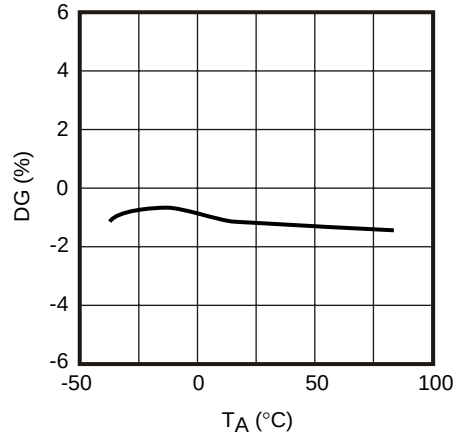
C- INPUT BIAS VOLTAGE vs. TEMPERATURE



CVBS INPUT CLAMP VOLTAGE vs. TEMPERATURE

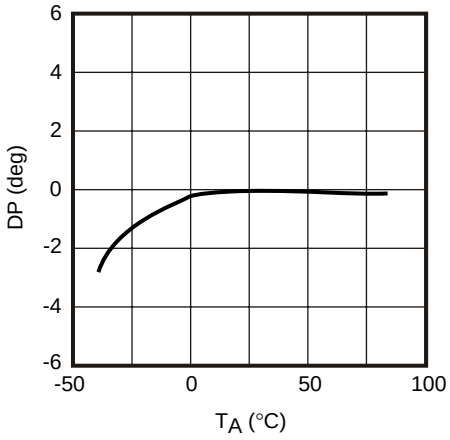


S-VHS DIFFERENTIAL GAIN vs. TEMPERATURE

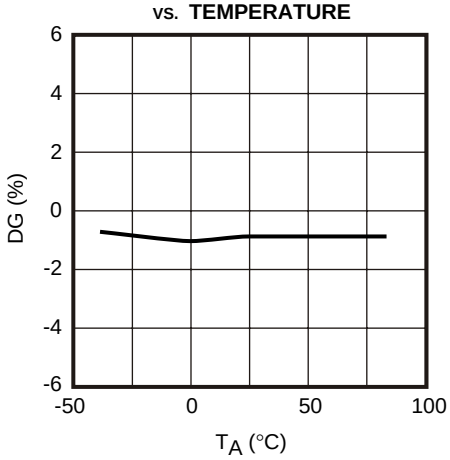


TYPICAL PERFORMANCE CHARACTERISTICS

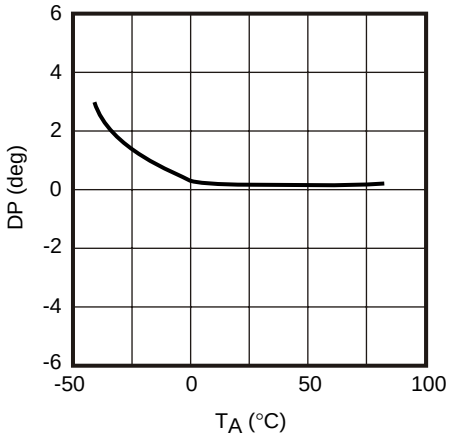
S-VHS DIFFERENTIAL PHASE vs. TEMPERATURE



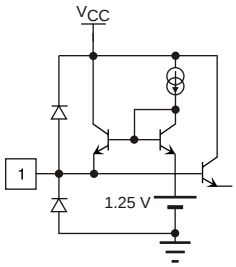
CVBS DIFFERENTIAL GAIN vs. TEMPERATURE



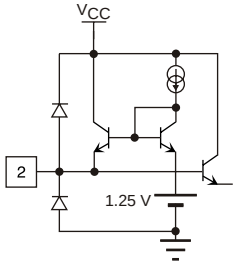
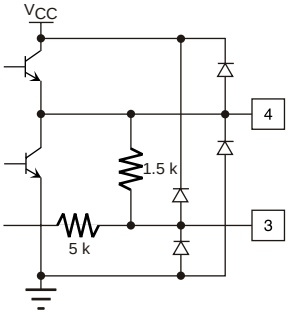
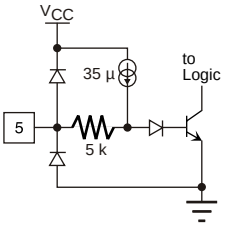
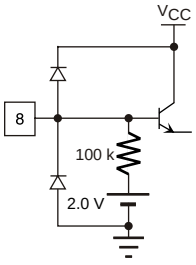
CVBS DIFFERENTIAL PHASE vs. TEMPERATURE



PIN FUNCTION DESCRIPTION

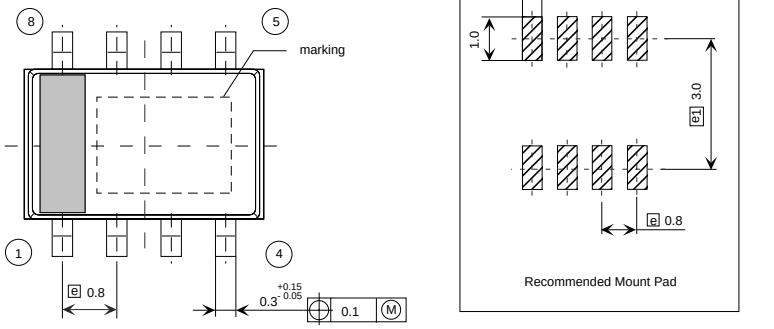
PIN NO.	SYMBOL	INTERNAL EQUIVALENT CIRCUIT	DESCRIPTION
1	Y-INPUT		Luminance Input Terminal. The luminance input signal is clamped at 1.25 V.

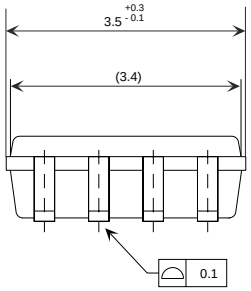
PIN FUNCTION DESCRIPTION (CONT.)

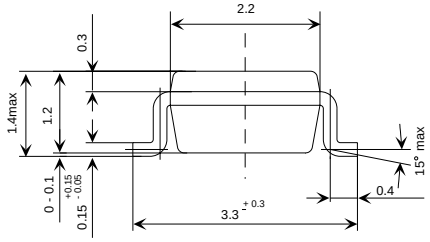
PIN NO.	SYMBOL	INTERNAL EQUIVALENT CIRCUIT	DESCRIPTION
2	CVBS-INPUT		CVBS Signal Input Terminal. The CVBS input signal is clamped at 1.25 V.
3 4	SAG OUTPUT		Pin 3: SAG Terminal Pin 4: Signal Output Terminal. The output is available to drive a 75 Ω + 75 Ω load.
5	CHANGE SW		Change-Over Switch Terminal for selecting S-VHS or CVBS. The S-VHS signal is applied to the output when Pin 5 is connected to High or Open. The CVBS signal is applied to the output when Pin 5 is connected to Low.
6	GND		GND Terminal
7	V_{CC}		Power Supply Terminal
8	C-INPUT		Chromanance Input Terminal. The chromanance input signal is biased to 2.0 V by a 100 kΩ bias resistor.

PACKAGE OUTLINE

SOT23L-8







Dimensions are shown in millimeters
Tolerance: x.x = ± 0.2 mm (unless otherwise specified)

Marking Information

	Marking
TK15414	414

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