Low Threshold Dual N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Dual N-channel device
- Low threshold 2.0V max.
- High input impedance
- ► Low input capacitance 200pF
- Fast switching speeds
- ▶ Low caps ON resistance
- Free from secondary breakdown
- Low input and output leakage

Applications

- Logic level interfaces ideal for TTL and CMOS
- Solid state relays
- Medical ultrasound pulsers
- Analog switches
- General purpose line drivers
- Telecom switches

General Description

The Supertex TN2425TG is a dual low threshold enhancement mode (normally off) transistor utilizing a vertical DMOS structure and Supertex's well proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

	Device	Package Option	DV /DV	D (max)	V (max)	l (min)
		8-Lead SOIC (Narrow Body)	BV _{DSS} /BV _{DGS}	R _{DS(ON)} (max)	V _{GS(th)} (max)	I _{D(ON)} (min)
	TN2425TG	TN2425TG	250V	3.5Ω	2.0V	1.8A

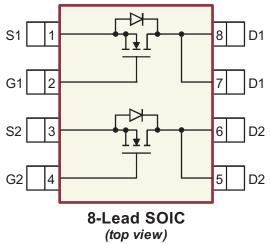
Absolute Maximum Ratings

Parameter	Value
Drain to source voltage	BV _{DSS}
Drain to gate voltage	BV _{DGS}
Gate to source voltage	±20V
Thermal resistance, Junction to drain lead	50°C/W
Operating and storage temperature	-55°C to +150°C
Soldering temperature ¹	+300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Note 1. Distance of 1.6mm from case for 10 seconds.

Pin Configuration



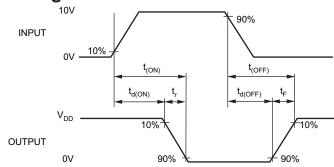
Electrical Characteristics (each device, T_j=25°C unless otherwise specified)

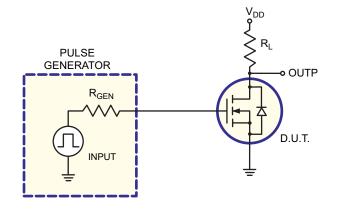
BV _{DSS} Drain-to-source breakdown voltage 250 - - V V _{GS} = 0V, I _D = 250μA	Symbol	Parameter	Min	Тур	Max	Units	Conditions
V _{OS(III)} Gate threshold voltage 0.6 - 2.0 V V _{OS} = V _{DS} , I _D = 1mA ΔV _{Mation} Change in V _{GS(III)} with temperature - - 25 mV V _{OS} = V _{DS} , I _D = 1mA ΔV _{GS(III)} V _{GS(III)} change with temperature - - -5.0 mV/°C V _{OS} = V _{DS} , I _D = 1mA I _{OSS} Gate body leakage current - - - 100 nA V _{OS} = V _{DS} , I _D = 1mA I _{DSS} Gate body leakage current - - - 100 nA V _{OS} = 250V, V _{DS} = 0V I _{DSS} Zero gate voltage drain current - - 10 mA V _{OS} = 0.W, V _{DS} = 0V I _{DSS} Zero gate voltage drain current 1.5 - - A V _{OS} = 0.W, V _{DS} = 0V I _{DSS} Zero gate voltage drain current 1.5 - - A V _{OS} = 0.W, V _{DS} = 0V I _{DSS} Static drain-to-source ON-state resistance - 5.0 A V _{OS} = 6.0V, V _{DS} = 25V R _{DSS} Static drain-to-source ON-state resistance	BV _{DSS}	Drain-to-source breakdown voltage	250	-	-	V	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Gate threshold voltage	0.6	-	2.0	V	$V_{GS} = V_{DS}$, $I_{D} = 1mA$
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	ΔV _{Match}	Change in $V_{_{\mathrm{GS(th)}}}$ with temperature	-	-	25	mV	$V_{GS} = V_{DS}, I_{D} = 1 \text{mA},$ $T_{.} = 10^{\circ}\text{C} - 80^{\circ}\text{C}$
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\Delta V_{GS(th)}$	V _{GS(th)} change with temperature	-	-	-5.0	mV/°C	$V_{GS}^{A} = V_{DS}, I_{D} = 1mA$
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		Gate body leakage current	-	-	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
1.0			-	-	10	μA	V_{DS} = Max rating, V_{GS} = 0V
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	DSS	Zero gate voltage drain current	ı	1	1.0	mA	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$		ON-state drain current	1.5	-	-	A	$V_{GS} = 6.0V, V_{DS} = 25V$
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	D(ON)		1.8	-	-		$V_{GS} = 10V, V_{DS} = 25V$
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	D	I F	-	-	5.0	Ω	$V_{GS} = 4.5V, I_{D} = 300mA$
$ \begin{array}{ c c c c c c c c } \hline \text{NMATCH} & \text{Noision} \\ \hline \text{AR}_{DS(ON)} & \text{Change in R}_{DS(ON)} \text{ with temperature} & - & - & 1.4 & \%/^{\circ}\text{C} & \text{V}_{GS} = 10\text{V}, \text{I}_{D} = 400\text{mA} \\ \hline \text{G}_{FS} & \text{Forward transconductance} & 300 & - & - & \text{mmho} \\ \hline \text{G}_{FSMATCH} & \text{Channel to channel G}_{FS} \text{ matching} & - & - & 5 & \% & \text{V}_{DS} = 15\text{V}, \text{I}_{D} = 50\text{mA} \\ \hline \text{C}_{ISS} & \text{Input capacitance} & - & 115 & 200 \\ \hline \text{C}_{OSS} & \text{Common source output capacitance} & - & 10 & 40 \\ \hline \text{C}_{ISSMATCH} & \text{Channel to channel C}_{ISS} \text{ matching} & - & - & 25 \\ \hline \text{C}_{OSSMATCH} & \text{Channel to channel C}_{OSS} \text{ matching} & - & - & 25 \\ \hline \text{C}_{CSSMATCH} & \text{Channel to channel C}_{RSS} \text{ matching} & - & - & 25 \\ \hline \text{C}_{RSSMATCH} & \text{Channel to channel C}_{RSS} \text{ matching} & - & - & 25 \\ \hline \text{C}_{RSSMATCH} & \text{Channel to channel C}_{RSS} \text{ matching} & - & - & 25 \\ \hline \text{C}_{TITO-ON delay time} & - & 5 & 15 \\ \hline \text{C}_{RSS II} & \text{Turn-ON delay time} & - & 25 & 35 \\ \hline \text{C}_{ISSMATCH} & \text{Turn-OFF delay time} & - & 25 & 35 \\ \hline \text{C}_{ISSMATCH} & \text{Turn-OFF delay time} & - & 25 & 35 \\ \hline \text{C}_{ISSMATCH} & \text{Channel to channel C}_{RSS} & \text{Channel to channel C}_{RSS$	DS(ON)		-	-	3.5		$V_{GS} = 10V, I_{D} = 400mA$
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	R _{MATCH}	Channel to channel R _{DS(ON)} matching	-	-	20	%	$V_{GS} = 10V, I_{D} = 400mA$
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\Delta R_{DS(ON)}$	Change in R _{DS(ON)} with temperature	-	-	1.4	%/°C	$V_{GS} = 10V, I_{D} = 400mA$
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Forward transconductance	300	-	-	mmho	$V_{DS} = 15V, I_{D} = 400mA$
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	G	Channel to channel G _{FS} matching	-	-	5	%	$V_{DS} = 15V, I_{D} = 50mA$
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			-	-	5	%	$V_{GS} = 15V, I_{D} = 1.50A$
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	C _{ISS}	Input capacitance	-	115	200		V _{GS} = 0V, V _{DS} = 25V, f = 1MHz
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Common source output capacitance	-	30	100	pF	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Reverse transfer capacitance	-	10	40		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	C _{ISSMATCH}	Channel to channel C _{ISS} matching	-	-	25		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Channel to channel C _{oss} matching	-	-	25	%	$V_{GS} = 0V, V_{DS} = 25V, f = 1MHz$
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Channel to channel C _{RSS} matching	-	-	25		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		Turn-ON delay time	-	5	15		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	t _r	Rise time	-	10	25	ns	
t_f Fall time-515 V_{SD} Diode forward voltage drop1.8V $V_{GS} = 0V$, $I_{SD} = 500 mA$	t _{d(OFF)}	Turn-OFF delay time	-	25	35		
		Fall time	-	5	15		
	V _{SD}	Diode forward voltage drop	-	-	1.8	V	$V_{GS} = 0V, I_{SD} = 500 \text{mA}$
		Reverse recovery time	-	300	-	ns	$V_{GS} = 0V$, $I_{SD} = 500$ mA

Notes:

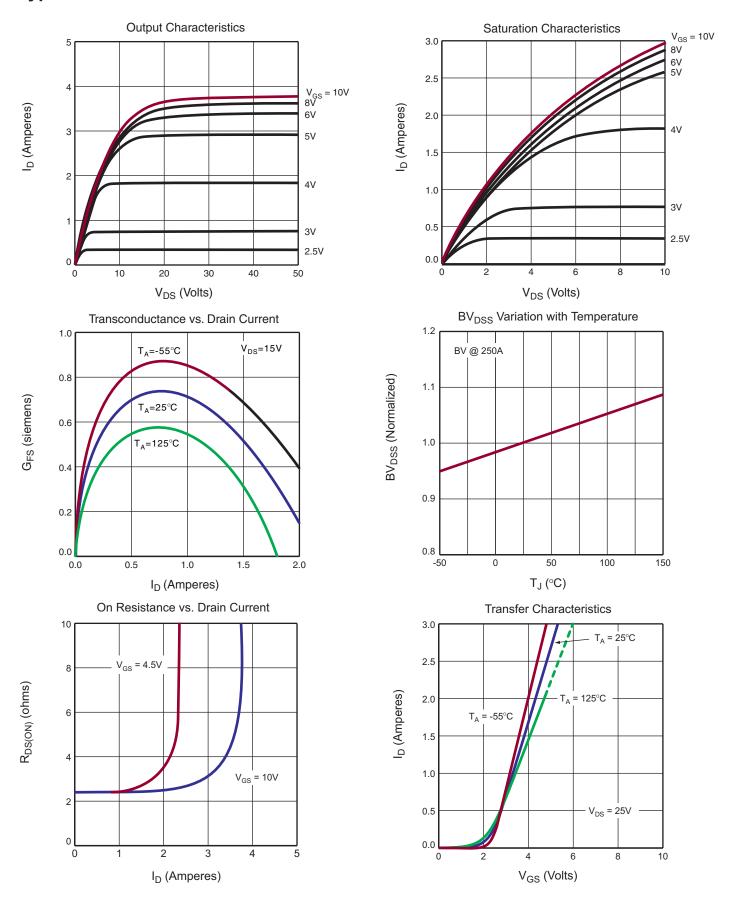
1.All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.) 2.All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

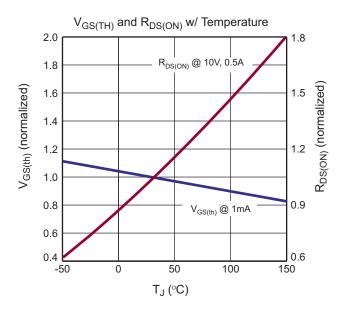


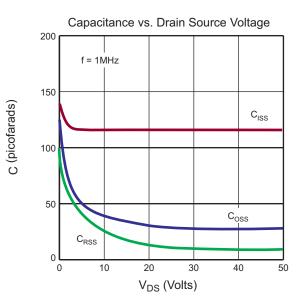


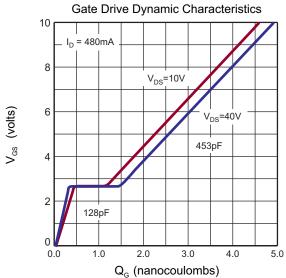
Typical Performance Curves



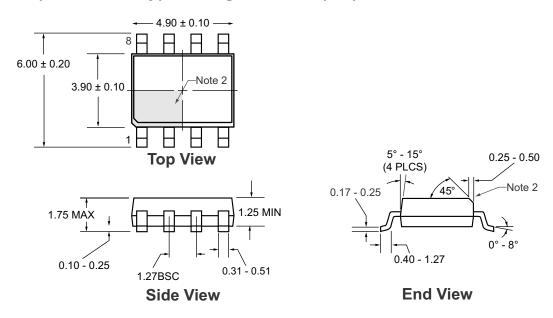
Typical Performance Curves (cont.)







8-Lead SOIC (Narrow Body) Package Outline (TG)



Notes:

- 1. All dimensions in millimeters. Angles in degrees.
- If the corner is not chamfered, then a Pin 1 identifier must be located within the area indicated.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc. does not recommend the use of its products in life support applications, and will not knowingly sell its products for use in such applications, unless it receives an adequate "product liability indemnification insurance agreement". **Supertex** does not assume responsibility for use of devices described and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions or inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications, refer to the **Supertex** website: http://www.supertex.com.

©2007 **Supertex inc.** All rights reserved. Unauthorized use or reproduction is prohibited.