



# TSM7104D

## 20V Dual P-Channel Enhancement Mode MOSFET

SOP-8



Pin assignment:

1. Source 1
2. Gate 1
3. Source 2
4. Gate 2
- 5, 6. Drain 2
- 7, 8. Drain 1

$V_{DS} = -20V$

$R_{DS(on)}, V_{GS} @ -4.5V, I_{DS} @ -2.3A = 130m\Omega$

$R_{DS(on)}, V_{GS} @ -2.5V, I_{DS} @ -2.0A = 190m\Omega$

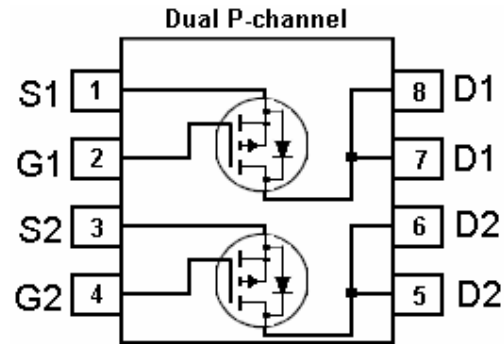
### Features

- ◇ Advanced trench process technology
- ◇ High density cell design for ultra low on-resistance
- ◇ Excellent thermal and electrical capabilities
- ◇ Surface mount
- ◇ Fast switching

### Ordering Information

Part No.	Packing	Package
TSM7104DCS	Tape & Reel	SOP-8

### Block Diagram



### Absolute Maximum Rating (Ta = 25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-20V	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	V
Continuous Drain Current, $V_{GS} @ 4.5V$ .	$I_D$	-2.3	A
Pulsed Drain Current, $V_{GS} @ 4.5V$	$I_{DM}$	-10	A
Maximum Power Dissipation	$P_D$	Ta = 25 °C	2
		Ta > 25 °C	16
Operating Junction Temperature	$T_J$	+150	°C
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	°C

### Thermal Performance

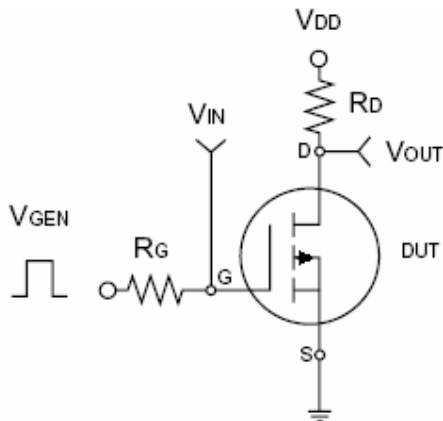
Parameter	Symbol	Limit	Unit
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta ja}$	62.5	°C/W

Note: Surface mounted on FR4 board  $t \leq 5sec$ .

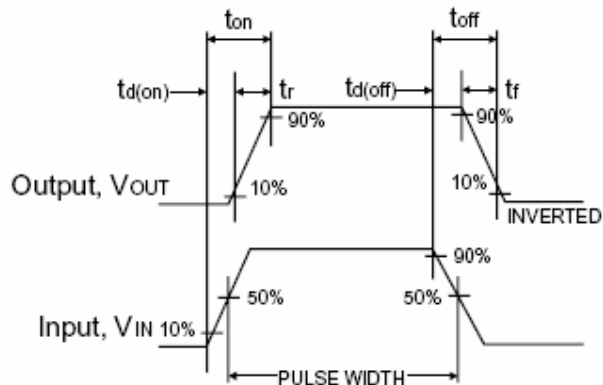


Electrical Characteristics						
Rate $I_D = -2.3A$ , ( $T_a = 25^\circ C$ unless otherwise noted)						
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	$BV_{DSS}$	-20	--	--	V
Drain-Source On-State Resistance	$V_{GS} = -4.5V, I_D = -2.3A$	$R_{DS(ON)}$	--	90	130	m $\Omega$
Drain-Source On-State Resistance	$V_{GS} = -2.5V, I_D = -2.0A$	$R_{DS(ON)}$	--	120	190	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	$V_{GS(TH)}$	-0.45	--	--	V
Zero Gate Voltage Drain Current	$V_{DS} = -16V, V_{GS} = 0V$	$I_{DSS}$	--	--	-1.0	$\mu A$
Gate Body Leakage	$V_{GS} = \pm 8V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	nA
Forward Transconductance	$V_{DS} = -5V, I_D = -2.3A$	$g_{fs}$	--	6.5	--	S
<b>Dynamic</b>						
Total Gate Charge	$V_{DS} = -6V, I_D = -2.3A,$ $V_{GS} = -4.5V$	$Q_g$	--	5.4	10	nC
Gate-Source Charge		$Q_{gs}$	--	0.8	--	
Gate-Drain Charge		$Q_{gd}$	--	1.1	--	
Turn-On Delay Time	$V_{DD} = -6V, R_L = 6\Omega,$ $I_D = -1A, V_{GEN} = -4.5V,$ $R_G = 6\Omega$	$t_{d(on)}$	--	5	25	nS
Turn-On Rise Time		$t_r$	--	19	60	
Turn-Off Delay Time		$t_{d(off)}$	--	95	110	
Turn-Off Fall Time		$t_f$	--	65	80	
Input Capacitance	$V_{DS} = -6V, V_{GS} = 0V,$ $f = 1.0MHz$	$C_{iss}$	--	447	--	pF
Output Capacitance		$C_{oss}$	--	127	--	
Reverse Transfer Capacitance		$C_{rss}$	--	80	--	
<b>Source-Drain Diode</b>						
Max. Diode Forward Current		$I_S$	--	--	-1.6	A
Diode Forward Voltage	$I_S = -1.6A, V_{GS} = 0V$	$V_{SD}$	--	-0.8	-1.2	V

Note : pulse test: pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$

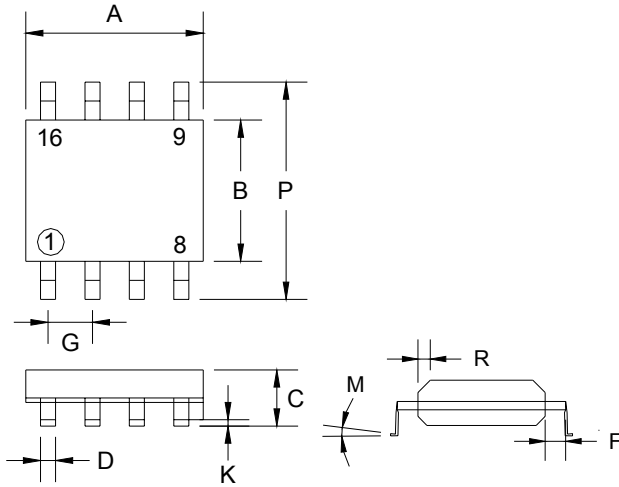


Switching Test Circuit



Switchin Waveforms

## SOP-8 Mechanical Drawing



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 (typ)		0.05 (typ)	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019