NEC

AGC/UP-CONVERTER WITH IQ MODULATOR

UPC8158K

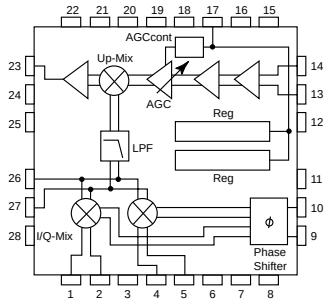
FEATURES

- **SUPPLY VOLTAGE:**
  V_{CC} = 2.7 to 4.0 V, I_{CC} = 28 mA @ V_{CC} = 3.0 V
- **BUILT-IN LPF:**
  Suppresses spurious multipled by TX local (LO1)
- **AGC AMPLIFIER INSTALLED IN LOCAL PORT OF UPCONVERTER:**
  GCR = 35 dB MIN. @ fout = 1.5 GHz
- **EXCELLENT PERFORMANCE:**
  Padj = -65dBc TYP. @ $\Delta f = \pm 50$ KHz, EVM = 1.2 %rms TYP.
- **EXTERNAL IF FILTER:**
  Can be applied between modulator output and up converter input terminal

APLICATIONS

- **Digital cellular phones**
  (PDC800M, PDC1.5G,TDMA1900 and so on)
- **Wireless Communiaction Systems**
  (MMDS, Broadband wireless access)

INTERNAL BLOCK DIAGRAM



DESCRIPTION

The UPC8158K is a silicon microwave monolithic integrated circuit designed as a quadrature modulator for digital mobile communication systems. This MMIC consist of a 0.8 GHz to 1.5 GHz up-converter and 100 MHz to 300 MHz quadrature modulator which are equipped with AGC and power save functions. This configuration suits IF modulation systems and is packaged in a 28-pin QFN suitable for high density mounting. The chip is manufactured using NEC's 20 GHz f_T silicon bipolar process NESAT™ III to realize low power consumption. Consequently the UPC8158K can contribute to make RF blocks smaller size, higher performance and lower power consumption.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC1} = V_{CC2} = V_{CC3} = 3.0 V, V_{PS}/V_{AGC} = 2.5 V)

PART NUMBER PACKAGE OUTLINE			UPC8158K		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
	UP-CONVERTER + QUADRATURE MODULATOR TOTAL				
$I_{CC\ (TOTAL)}$	Total Circuit Current, No input signal	mA	23.7	28	37.6
$I_{CC(PS)\ TOTAL}$	Total Circuit Current at Power Save Mode, $V_{PS} \leq 0.5$ V(low), No input signal	µA		0.3	10
$P_{RFout}1$	Total Output Power 1, V_{AGC} = 2.5 V	dBm	-15	-11.5	-8
$P_{RFout}2$	Total Output Power 2, V_{AGC} = 1.0 V	dBm	-56.5	-52	-46.5
LOL	LO Carrier Leak, $f_{LOL} = f_{LO1} + f_{LO2}$	dBc		-40	-30
ImR	Image Rejection (Side Band Leak)	dBc		-40	-30
$IM_{3(I/Q)}$	I/Q 3rd Order Distortion	dBc		-50	-30
GCR	AGC Gain Control Range, V_{AGC} = 2 V $\rightarrow$1 V	dB	35	40	
EVM	Error Vector Magnitude, MOD Pattern PN9	%rms		1.2	3.0
P_{adj}	Adjacent Channel Interference, $\Delta f = \pm 50$KHz, MOD Pattern: PN9	dBc		-65	-60
P_{out}(8fLO1)	Spurious Suppression, fLO1 × 8, fLO1 × 8 (image)[Note]	dBc		-70	-65
T_{PS}(Rise)	Power Save Rise Time, V_{PS}(Low) $\rightarrow$ V_{PS}(High)	µs		2	5
T_{PS}(Fall)	Power Save Fall Time, V_{PS}(High) $\rightarrow$ V_{PS}(Low)	µs		2	5
$Z_{I/Q}$	I/Q Input Impedance, Between pin I/Ib, Q/Qb	kΩ	80	200	
$I_{I/Q}$	I/Q Input Bias Current, Between pin I/Ib, Q/Qb	µA		5	13
Z_{LO1}	LO1 Input VSWR, f_{LO1} = 100 M to 300 MHz	-		1.5 :1	

Note:
1. Without external LC between Fil1 and Fil2 pin on this frequency conditions. Spectrum analyzer conditions: VBW = 300 Hz, RBW = 300 Hz.

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

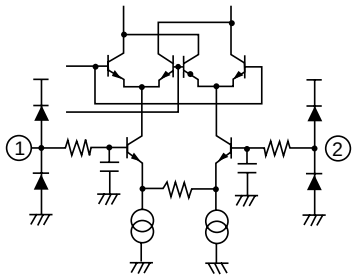
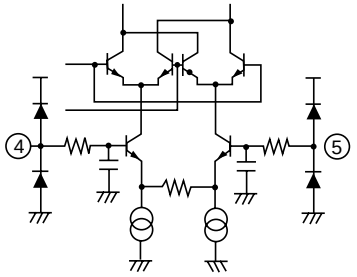
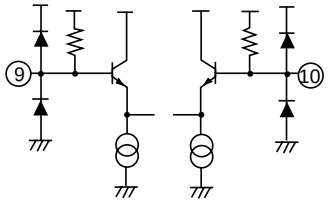
SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CC}	Supply Voltage	V	5.0
V_{PS}/V_{AGC}	Power Save & AGC Control	V	5.0
P_D	Power Dissipation[2]	mW	430
T_A	Operating Ambient Temp.	°C	-40 to +85
T_{STG}	Storage Temperature	°C	-55 to +150

Note:
1. Operation in excess of any one of these conditions may result in permanent damage.
2. T_A = +85º C

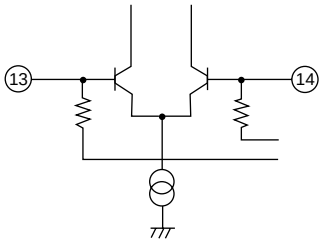
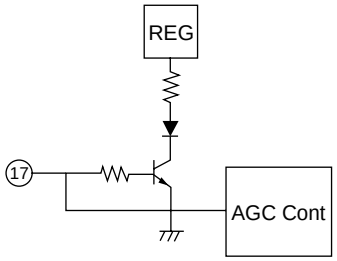
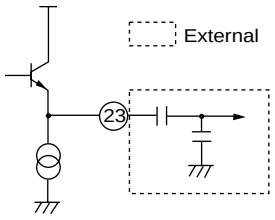
RECOMMENDED OPERATING CONDITIONS

PART NUMBER			UPC8158K		
SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{CC}	Supply Voltage	V	2.7	3.0	4.0
V_{PS}	Power Save Voltage	V	0		0.3
V_{AGCPS}	AGC Control Voltage	V	1.0		2.5
T_A	Operating Ambient Temp.	°C	-30	+25	+80
f_{RFout}	Upconv. RF Output Freq.	MHz	800		1500
f_{LO2in}	LO2 Input Frequency	MHz	600		1750
$f_{I/Qin}$	I/Q Input Frequency	MHz	DC		10
P_{LO1in}	LO1 Input Level	dBm	-18	-15	-12
P_{LO2in}	LO2 Input Level	dBm	-18	-15	-12
$V_{I/Qin}$	I/Q Input Amplitude	mV_{P-P}		420	500
$f_{UPCONin}$	Upconverter Input Freq.	MHz	100		300
f_{MODout}	Modulator Output Freq.				
f_{LO1in}	LO1 Input Frequency				

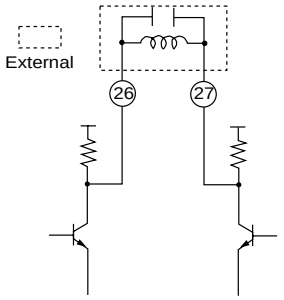
PIN EXPLANATIONS

PIN NO.	SYMBOL	SUPPLY VOLTAGE (V)	PIN VOLTAGE (V)	FUNCTION AND APPLICATION	EQUIVALENT CIRCUIT
1	lin	Vcc/2	–	Input for I signal. This input impedance is 200 kΩ. In the case of that I/Q input signals are single ended, amplitude of the signal 500 m V_{P-P} max.	
2	linb	Vcc/2	–	Input for I signal. This input impedance is 200 kΩ. In the case of that I/Q input signals are single ended,Vcc/2 biased DC signal should be input. In the case of the I/Q input signals are differential, amplitude of the signal is 500 m V_{P-P} max.	
3	N.C.	–	–	This pin is not connected to internal circuit. This pin should be opened or grounded.	
4	Qinb	Vcc/2	–	Input for Q signal. This input impedance is 200 KΩ. In the case of that I/Q input signals are single ended, amplitude of the signal is 500 m V_{P-P} max.	
5	Qin	Vcc/2	–	Input for I signal. This input impedance is 200 kΩ. In the case of that I/Q input signals are single ended,Vcc/2 biased DC signal should be input. In the case of the I/Q input signals are differential, amplitude of the signal is 500 m V_{P-P} max.	
6	N.C.	–	–	These pins is not connected to internal circuit. These pins should be opened or grounded.	
7	N.C.	–	–		
8	N.C.	–	–		
9	LO1inb	–	2.98	Bypass pin of modulator's local input. This pin should be decoupled with 330 pF capacitor.	
10	LO1in	–	2.98	Local signal for modulator. This pin must be coupled with DC cut capacitor 330 pF and should be terminated with 51 Ω resistor	
11	Vcc	2.7 to 4.0	–	Supply Voltage pin modulator, up-converter and AGC circuits.	

PIN EXPLANATIONS (CONT.)

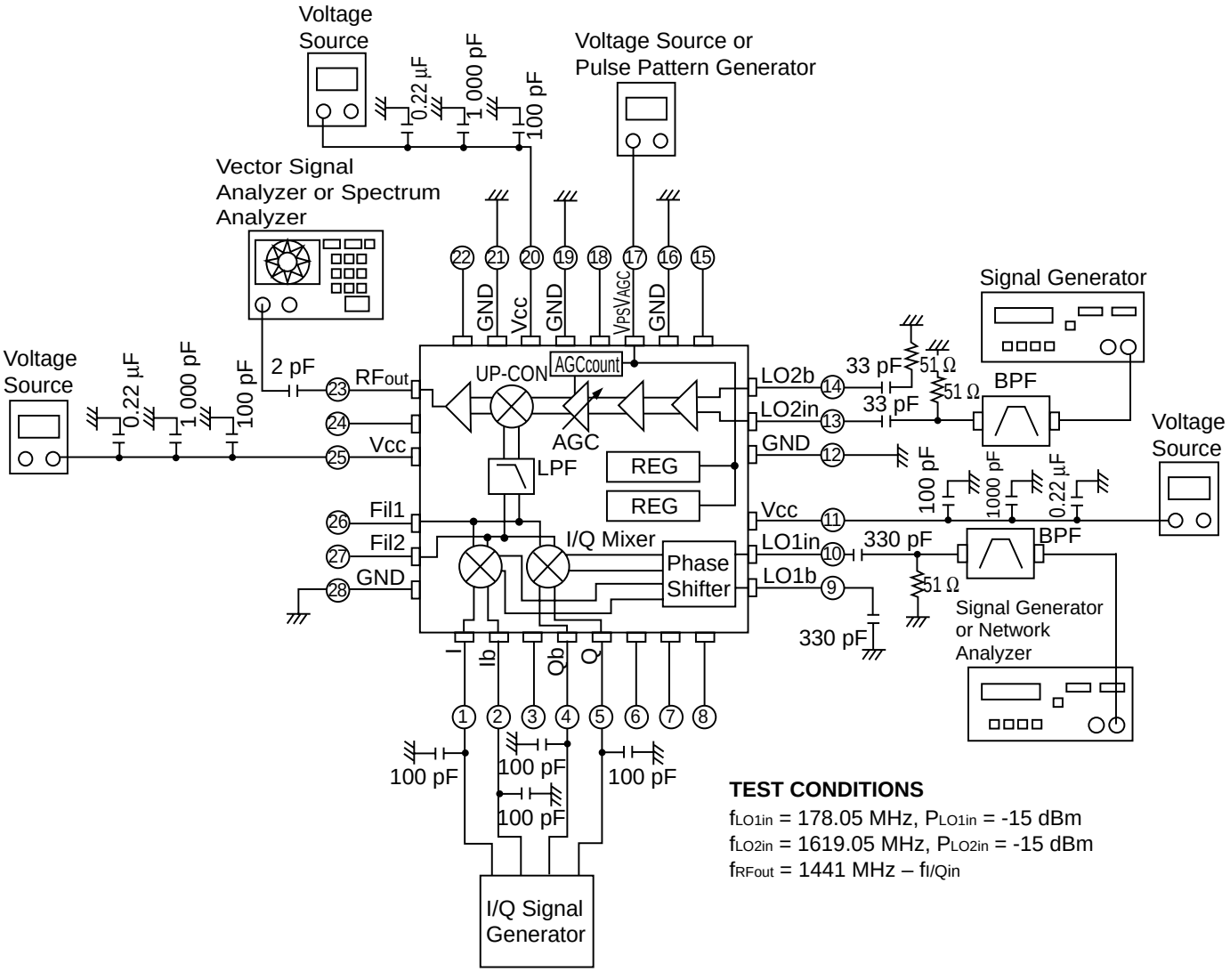
PIN NO.	SYMBOL	SUPPLY VOLTAGE (V)	PIN VOLTAGE (V)	FUNCTION AND APPLICATION	EQUIVALENT CIRCUIT
12	GND	0	–	Ground pin for modulator, up-converter and AGC circuits. This pin should be grounded with minimum inductance. Form the ground pattern as widely as possible to minimize ground impedance.	
13	LO2in	–	1.8	Local signal input for modulator. This pin must be coupled with DC cut capacitor 33 pF and should be terminated with 51 Ω resistor.	
14	LO2inb	–	1.8	Bypass pin of up-converter's local signal input. This pin should be decoupled with 33 pF capacitor.	
15	N.C.	–	–	This pin is not connected to internal circuit. This pin should be opened or grounded.	
16	GND	0	–	Ground pin for modulator, up-converter and AGC circuits. This pin should be grounded with minimum inductance.	
17	V_{PS}/V_{AGC}	V_{PS}/V_{AGC}	–	Power save control pin for modulator, upconverter and AGC circuits. This pin also assigned as gain control pin forAGC circuits. Operation status with applied voltages are as follows. V_{PS}/V_{AGC} (V) / STATE 0 to 0.4 / OFF (Sleep Mode) 1 to 2.5 / On (AGC Mode)	
18	N.C.	–	–	These pins is not connected to internal circuit. These pins should be opened or grounded.	
19	GND	0	–	Ground pin for modulator, up-converter and AGC circuits. This pin should be grounded with minimum inductance.	
20	Vcc	2.7 to 4.0	–	Supply Voltage pin for modulator, up-converter and AGC circuits.	
21	GND	0	–	Ground pin for RF output buffer. This pin should be grounded with minimum inductance.	
22	N.C.	–	–	This pin is not connected to internal circuit. This pin should be opened or grounded.	
23	RF_{OUT}	–	1.75	RF output pin. This pin is emitter follower which is low impedance output port. This pin can be easily matched to 50 Ω impedance using external coupling and decoupling capacitors.	
24	N.C.	–	–	These pins are not connected to internal circuit. These pins should be opened or grounded.	
25	Vcc	2.7 to 4.0	–	Supply Voltage pin for RF output buffer.	

PIN EXPLANATIONS (CONT.)

PIN NO.	SYMBOL	SUPPLY VOLTAGE (V)	PIN VOLTAGE (V)	FUNCTION AND APPLICATION	EQUIVALENT CIRCUIT
26	FIL1	–	2.76	External inductor and capacitor can supress harmonics spurious of LO1 frequency. LC value should be determined according to LO1 input frequency and suppression level.	
27	FIL2	–	2.76		
28	GND	0	–	Ground pin for modulator, up-converter and AGC circuits. This pin should be grounded with minimum inductance. Form the ground pattern as widely as possible to minimize ground impedance.	

Note:
1. Pin Votages are measured on Vcc = 3.0 V.

TEST CIRCUIT

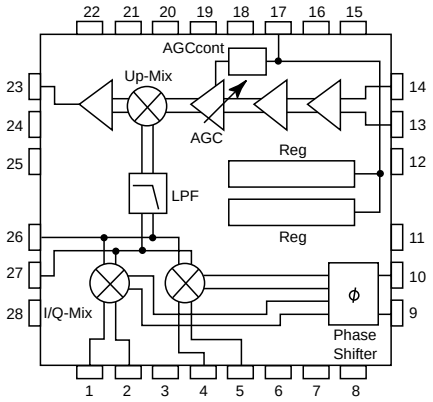


TEST CONDITIONS

f_{LO1in} = 178.05 MHz, P_{LO1in} = -15 dBm
f_{LO2in} = 1619.05 MHz, P_{LO2in} = -15 dBm
f_{RFout} = 1441 MHz – $f_{I/Qin}$

INTERNAL BLOCK DIAGRAM AND PIN CONNECTIONS (Top View)

UPC8158K



1. lin	8. N.C.	15. N.C.	22. N.C.
2. linb	9. LO1inb	16. GND	23. RFout
3. N.C.	10. LO1in	17. Vps/Vagc	24. N.C.
4. Qinb	11. Vcc	18. N.C.	25. Vcc
5. Qin	12. GND	19. GND	26. Fil1
6. N.C.	13. LO2in	20. Vcc	27. Fil2
7. N.C.	14. LO2inb	21. GND	28. GND

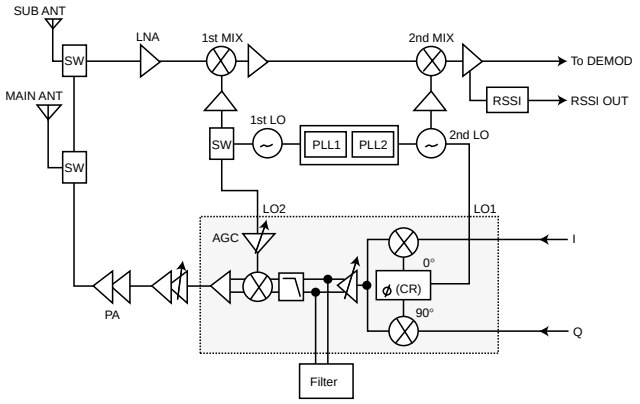
ORDERING INFORMATION

PART NUMBER	PACKAGE	QUANTITY
UPC8158K-E1	28-pin plastic QFN (5.1x0.95mm)	QTY. 2.5 kp/Reel.

Notes:
1. Embossed tape 12 mm wide. Pin 1 is in pull-out direction.

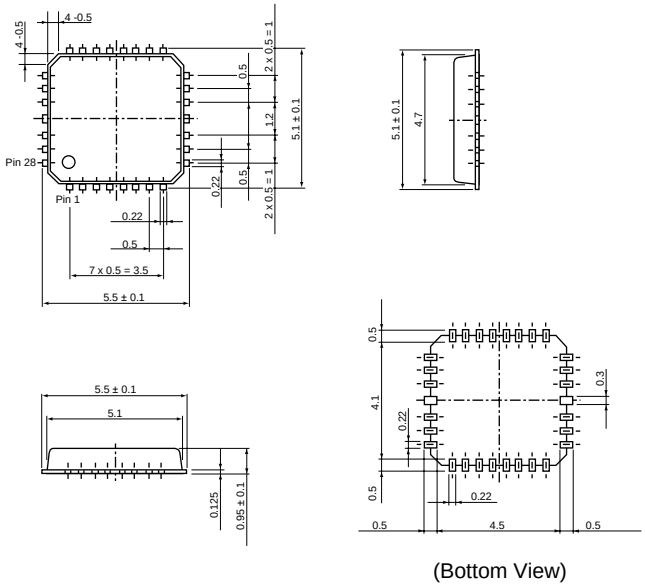
SYSTEM APPLICATION

PCS/TDMA PHONE



PACKAGE OUTLINE (Units in mm)

UPC8158K
28 PIN PLASTIC QFN



(Bottom View)