

**32-BIT FLUORESCENT DISPLAY TUBE DRIVER**

The  $\mu$ PD16326 is a fluorescent display tube driver using a high breakdown voltage CMOS process. It consists of 32-bit bidirectional shift registers, a latch circuit, and a high breakdown voltage CMOS driver block. The logic block operates on a 5 V power supply designed to be connected directly to a microcontroller (CMOS level input). The driver block has a 130 V and 20 mA high breakdown voltage output, and both the logic block and driver block consist of CMOS, allowing operation with low power consumption.

**FEATURES**

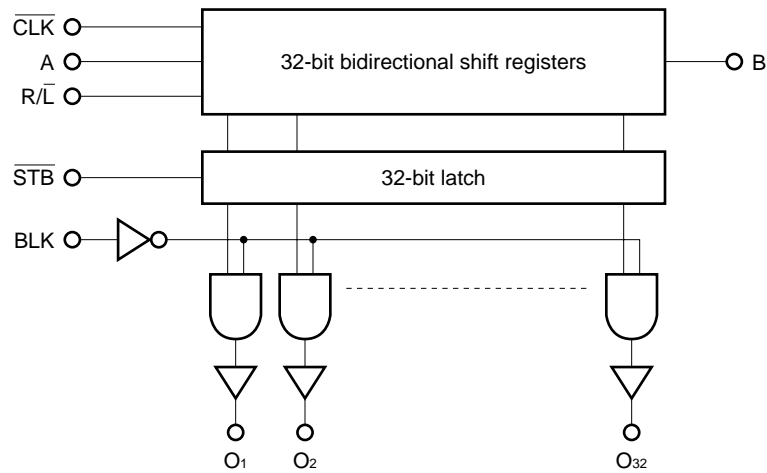
- High breakdown voltage CMOS structure
- High breakdown voltage, high current output (130 V, 20 mA)
- 32-bit bidirectional shift registers on chip
- Data control by transfer clock (external) and latch
- High-speed data transfer capability ( $f_{\max} = 8.0 \text{ MHz}_{\text{MIN}}$ )
- Wide operating temperature range ( $T_A = -40 \text{ to } 85 \text{ }^\circ\text{C}$ )

**ORDERING INFORMATION**

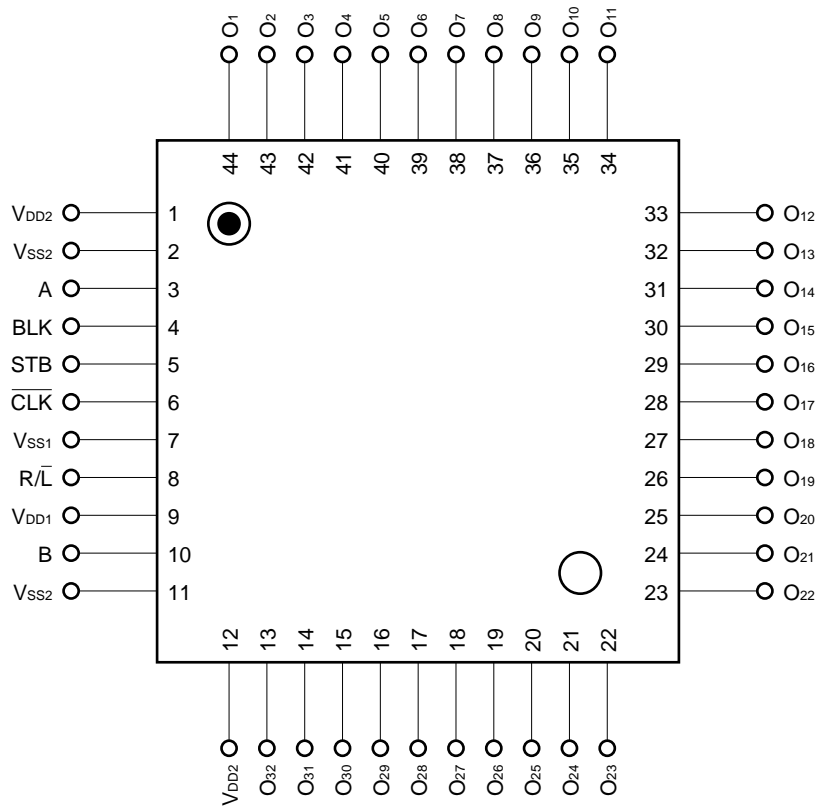
Part Number	Package
$\mu$ PD16326GB-3B4	44-pin plastic QFP (4-direction leads)

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



**Remark** Be sure to enter the power to V<sub>DD1</sub>, logic signal, and V<sub>DD2</sub>, in that order, and turn off the power in the reverse order.

**PIN DESCRIPTION**

Pin Symbol	Pin Name	Pin Number	Description
STB	Latch strobe input	5	H: Data through L: Data retention
A	RIGHT data input	3	When $R/\bar{L} = H$ , A: Input B: Output When $R/\bar{L} = L$ , A: Output B: Input
B	LEFT data input	10	
$\overline{CLK}$	Clock input	6	Shift is executed on a fall.
BLK	Blanking input	4	H: $O_1$ to $O_{32}$ : ALL "L"
$R/\bar{L}$	Shift control input	8	H: Right shift mode $A \rightarrow O_1 \dots O_{32} \rightarrow B$ L: Left shift mode $B \rightarrow O_{32} \dots O_1 \rightarrow A$
$O_1$ to $O_{32}$	High breakdown voltage output	13 - 44	130 V, 20 mA <sub>MAX</sub>
$V_{DD1}$	Logic block power supply	9	5 V ±10 %
$V_{DD2}$	Driver block power supply	1, 12	30 to 125 V
$V_{SS1}$	Logic ground	5	Connected to system GND
$V_{SS2}$	Driver ground	2, 11	Connected to system GND

**TRUTH TABLE 1 (SHIFT REGISTER BLOCK)**

Input		Output		Shift Register
$R/\bar{L}$	$\overline{CLK}$	A	B	
H	↓	Input	Output <sup>Note 1</sup>	Execution of right shift
H	H or L		Output	Retained
L	↓	Output <sup>Note 2</sup>	Input	Execution of left shift
L	H or L			Output

- Notes** 1. On a clock fall, the data items of  $S_{31}$  are shifted to  $S_{32}$ , and output from B.  
2. On a clock fall, the data items of  $S_2$  are shifted to  $S_1$ , and output from A.

**TRUTH TABLE 2 (LATCH BLOCK)**

STB	Operation
L	Retains $S_n$ data immediately before $\overline{STB}$ becomes L.
H	Outputs shift register data.

**TRUTH TABLE 3 (DRIVER BLOCK)**

$L_n$ <sup>Note</sup>	STB	BLK	Driver output state
×	×	H	L (all driver outputs: L)
×	L	L	Outputs $S_n$ data on STB fall.
L	H	L	L
H	H	L	H

**Note**  $L_n$ : Latch output

**Remark** × = H or L, H = high level, L = Low level

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C, V<sub>SS</sub> = 0 V)**

Item	Symbol	Rating	Unit
Logic block supply voltage	V <sub>DD1</sub>	-0.5 to +7.0	V
Driver block supply voltage	V <sub>DD2</sub>	-0.5 to +130	V
Logic block input voltage	V <sub>I</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver block output current	I <sub>O</sub>	20	mA
Package allowable power dissipation	P <sub>D</sub>	800 <sup>Note</sup>	mW
Operating ambient temperature	T <sub>A</sub>	-40 to +85	°C
Storage temperature	T <sub>stg</sub>	-65 to +150	°C

**Note** When T<sub>A</sub> ≥ 25 °C, load should be alleviated at a rate of -8.0 mW/°C. (T<sub>j</sub> = 125 °C (MAX.))

**RECOMMENDED OPERATING RANGE (T<sub>A</sub> = -40 to +85 °C, V<sub>SS</sub> = 0 V)**

Item	Symbol	MIN.	TYP.	MAX.	Unit
Logic block supply voltage	V <sub>DD1</sub>	4.5	5.0	5.5	V
Driver block supply voltage	V <sub>DD2</sub>	30		125	V
Input voltage high	V <sub>IH</sub>	0.7·V <sub>DD1</sub>		V <sub>DD1</sub>	V
Input voltage low	V <sub>IL</sub>	0		0.2·V <sub>DD1</sub>	V
Driver output current	I <sub>OH</sub>			-10	mA
	I <sub>OL</sub>			+2.5	mA

**ELECTRICAL SPECIFICATIONS (T<sub>A</sub> = 25 °C, V<sub>DD1</sub> = 4.5 to 5.5 V, V<sub>DD2</sub> = 125 V, V<sub>SS</sub> = 0 V)**

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage high	V <sub>OH1</sub>	Logic, I <sub>OH</sub> = -1.0 mA	0.9·V <sub>DD1</sub>		V <sub>DD1</sub>	V
Output voltage low	V <sub>OL1</sub>	Logic, I <sub>OL</sub> = 1.0 mA	0		0.1·V <sub>DD1</sub>	V
Output voltage high	V <sub>OH21</sub>	O <sub>1</sub> to O <sub>40</sub> , I <sub>OH</sub> = -0.5 mA	121			V
	V <sub>OH22</sub>	O <sub>1</sub> to O <sub>40</sub> , I <sub>OH</sub> = -5.0 mA	115			V
Output voltage low	V <sub>OL2</sub>	O <sub>1</sub> to O <sub>40</sub> , I <sub>OL</sub> = 0.5 mA			2.5	V
Input leakage current	I <sub>IL</sub>	V <sub>I</sub> = V <sub>DD1</sub> or V <sub>SS1</sub>			±1.0	μA
Input voltage high	V <sub>IH</sub>		0.7·V <sub>DD1</sub>		V <sub>DD1</sub>	V
Input voltage low	V <sub>IL</sub>		0		0.2·V <sub>DD1</sub>	V
Static consumption current	I <sub>DD1</sub>	Logic, T <sub>A</sub> = -40 to +85 °C			1 000	μA
	I <sub>DD1</sub>	Logic, T <sub>A</sub> = 25 °C			100	μA
	I <sub>DD2</sub>	Driver, T <sub>A</sub> = -40 to +85 °C			1 000	μA
	I <sub>DD2</sub>	Driver, T <sub>A</sub> = 25 °C			100	μA

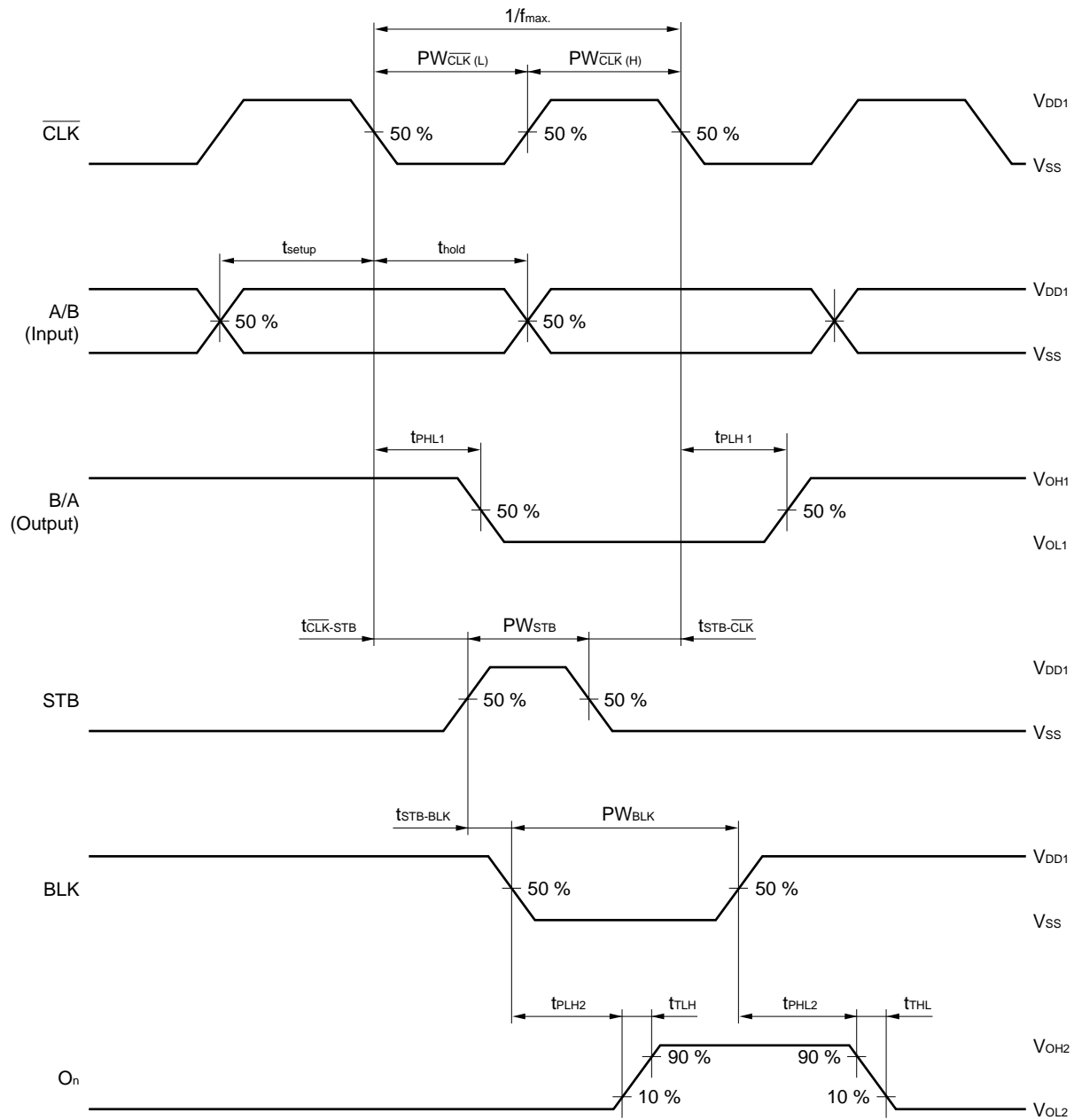
**SWITCHING CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ ,  $V_{DD1} = 5.0\text{ V}$ ,  $V_{DD2} = 125\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , logic  $C_L = 15\text{ pF}$ , driver  $C_L = 50\text{ pF}$ , driver  $R_L = 220\text{ k}\Omega$ ,  $t_r = t_f = 10\text{ ns}$ )

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transmission delay time	$t_{PHL1}$	$\overline{\text{CLK}} \downarrow \rightarrow \text{A/B}$			110	ns
	$t_{PLH1}$				110	ns
	$t_{PHL2}$	$\overline{\text{BLK}} \downarrow \rightarrow O_1 \text{ to } O_{32}$			300	ns
	$t_{PLH2}$				300	ns
Fall time	$t_{THL}$	$O_1 \text{ to } O_{32}$			600	ns
Rise time	$t_{TLH}$	$O_1 \text{ to } O_{32}$			500	ns
Maximum clock frequency	$f_{\text{max}}$	With cascading, Duty = 50 %	8.0			MHz
Input capacitance	$C_i$				15	pF

**TIMING REQUIREMENTS** ( $T_A = -40 \text{ to } +85\text{ }^\circ\text{C}$ ,  $V_{DD1} = 4.5 \text{ to } 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $t_r = t_f = 10\text{ ns}$ )

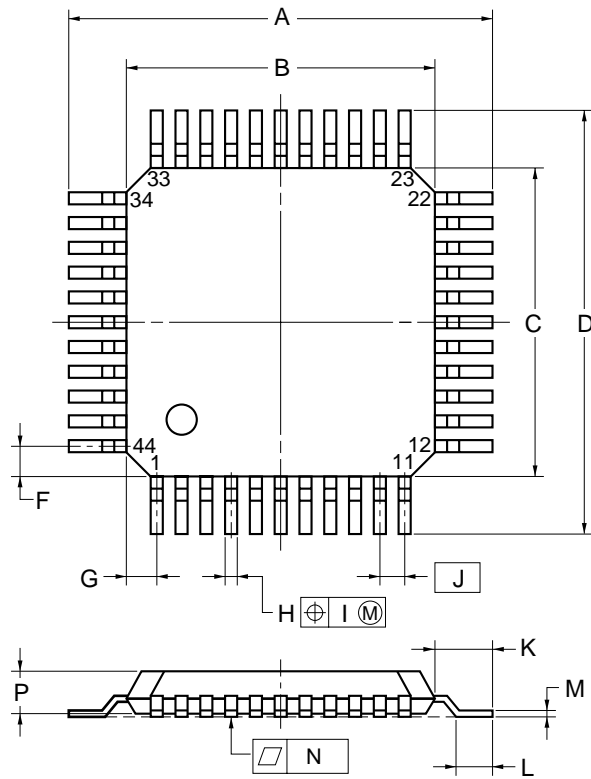
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	$PW_{\text{CLK}}$		40			ns
Strobe pulse width	$PW_{\text{STB}}$		80			ns
Blank pulse width	$PW_{\text{BLK}}$		1 500			ns
Data setup time	$t_{\text{setup}}$		15			ns
Data hold time	$t_{\text{hold}}$		30			ns
Clock-strobe time	$t_{\overline{\text{CLK}}\text{-STB}}$	$\overline{\text{CLK}} \downarrow \rightarrow \text{STB} \uparrow$	45			ns
Strobe-clock time	$t_{\text{STB-CLK}}$	$\text{STB} \downarrow \rightarrow \overline{\text{CLK}} \downarrow$	45			ns
Strobe-blank time	$t_{\text{STB-BLK}}$	$\text{STB} \uparrow \rightarrow \text{BLK} \downarrow$	80			ns

SWITCHING CHARACTERISTIC WAVEFORM (R/L = H)

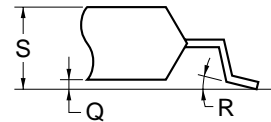


PACKAGE DRAWINGS

44 PIN PLASTIC QFP (Unit: mm)



detail of lead end



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	13.6±0.4	0.535 <sup>+0.017</sup> <sub>-0.016</sub>
B	10.0±0.2	0.394 <sup>+0.008</sup> <sub>-0.009</sub>
C	10.0±0.2	0.394 <sup>+0.008</sup> <sub>-0.009</sub>
D	13.6±0.4	0.535 <sup>+0.017</sup> <sub>-0.016</sub>
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	0.014 <sup>+0.004</sup> <sub>-0.005</sub>
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P)
K	1.8±0.2	0.071 <sup>+0.008</sup> <sub>-0.009</sub>
L	0.8±0.2	0.031 <sup>+0.009</sup> <sub>-0.008</sub>
M	0.15 <sup>+0.10</sup> <sub>-0.05</sub>	0.006 <sup>+0.004</sup> <sub>-0.003</sub>
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

P44GB-80-3B4-3

**RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered and mounted under the conditions recommended below.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

**SURFACE MOUNT TYPE**

For details of recommended soldering conditions, refer to the information document “Semiconductor Device Mounting Technology Manual” (C10535E).

**μPD16326GB-3B4**

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. MAX. (at 210 °C or above), Number of times: Twice, Time limit: None <sup>Note</sup>	IR35-00-2
VPS	Package peak temperature: 215 °C, Duration: 40 sec. MAX. (at 200 °C or above), Number of times: Twice, Time limit: None <sup>Note</sup>	VP15-00-2
Wave soldering	Solder bath temperature: 260 °C MAX., Duration: 10 sec. MAX., Number of times: Once, Time limit: None <sup>Note</sup>	WS60-00-1
Pin partial heating	Pin partial temperature: 300 °C MAX., Duration: 10 sec. MAX., Time limit: None <sup>Note</sup>	

**Note** For the storage period after dry-pack decapsulation, storage conditions are max. 25 °C, 65 % RH.

**Caution** Use of more than one soldering method should be avoided (except in the case of pin partial heating).

**REFERENCES**

NEC Semiconductor Device Reliability/Quality Control System (IEI-1212)

Quality Grade on NEC Semiconductor Devices (IEI-1209)



[MEMO]

[MEMO]

[MEMO]

No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.

NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.

While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.

NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.