

# MOS INTEGRATED CIRCUIT

# $\mu$ PD23C64340, 23C64380

### 64M-BIT MASK-PROGRAMMABLE ROM

### 8M-WORD BY 8-BIT (BYTE MODE) / 4M-WORD BY 16-BIT (WORD MODE)

### PAGE ACCESS MODE

#### Description

The  $\mu$ PD23C64340 and  $\mu$ PD23C64380 are 67,108,864 bits mask-programmable ROM. The word organization is selectable (BYTE mode : 8,388,608 words by 8 bits, WORD mode : 4,194,304 words by 16 bits).

The active levels of OE (Output Enable Input) can be selected with mask-option.

The  $\mu$ PD23C64340 and  $\mu$ PD23C64380 are packed in 48-pin TAPE FBGA.

#### Features

- Pin compatible with NOR Flash Memory
- Word organization
  - 8,388,608 words by 8 bits (BYTE mode)
  - 4,194,304 words by 16 bits (WORD mode)
- Page access mode
  - BYTE mode : 8 byte random page access ( $\mu$ PD23C64340)
  - 16 byte random page access ( $\mu$ PD23C64380)
  - WORD mode : 4 word random page access ( $\mu$ PD23C64340)
  - 8 word random page access ( $\mu$ PD23C64380)
- Operating supply voltage :  $V_{CC} = 2.7\text{ V to }3.6\text{ V}$

Operating supply voltage $V_{CC}$	Access time / Page access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)		Standby current (CMOS level input) $\mu$ A (MAX.)
		$\mu$ PD23C64340	$\mu$ PD23C64380	
3.0 V $\pm$ 0.3 V	100 / 25	40	60	30
3.3 V $\pm$ 0.3 V	90 / 25	55	75	

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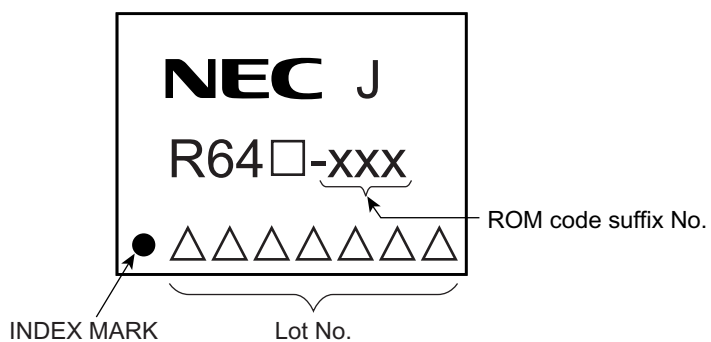
**Ordering Information**

Part Number	Package
μPD23C64340F9-xxx-BC3	48-pin TAPE FBGA (8 x 6)
μPD23C64380F9-xxx-BC3	48-pin TAPE FBGA (8 x 6)

(xxx : ROM code suffix No.)

**Marking Image**

Part Number	Marking ( □ )
μPD23C64340F9-xxx-BC3	B
μPD23C64380F9-xxx-BC3	C

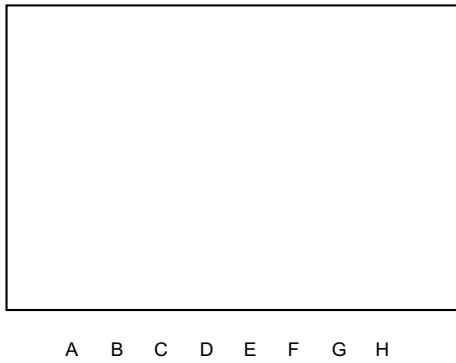


Pin Configuration

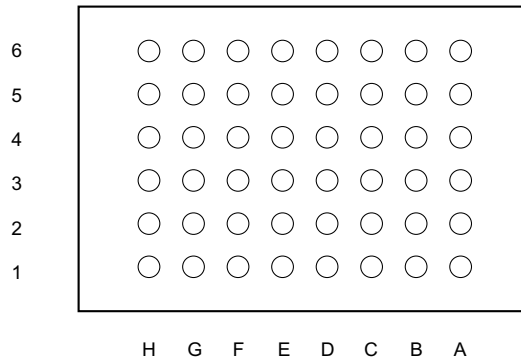
/xxx indicates active low signal.

48-pin TAPE FBGA (8 x 6)

Top View



Bottom View



	A	B	C	D	E	F	G	H
6	A13	A12	A14	A15	A16	WORD, /BYTE	O15, A-1	GND
5	A9	A8	A10	A11	O7	O14	O13	O6
4	NC	NC	A21	A19	O5	O12	V <sub>cc</sub>	O4
3	NC	NC	A18	A20	O2	O10	O11	O3
2	A7	A17	A6	A5	O0	O8	O9	O1
1	A3	A4	A2	A1	A0	/CE	/OE or OE	GND

	H	G	F	E	D	C	B	A
6	GND	O15, A-1	WORD, /BYTE	A16	A15	A14	A12	A13
5	O6	O13	O14	O7	A11	A10	A8	A9
4	O4	V <sub>cc</sub>	O12	O5	A19	A21	NC	NC
3	O3	O11	O10	O2	A20	A18	NC	NC
2	O1	O9	O8	O0	A5	A6	A17	A7
1	GND	/OE or OE	/CE	A0	A1	A2	A4	A3

- A0 to A21 : Address inputs
- O0 to O7, O8 to O14 : Data outputs
- O15, A-1 : Data output 15 (WORD mode),  
LSB Address input (BYTE mode)
- WORD, /BYTE : Mode select
- /CE : Chip Enable
- /OE or OE : Output Enable
- V<sub>cc</sub> : Supply voltage
- GND : Ground
- NC<sup>Note</sup> : No Connection
- DC : Don't Care

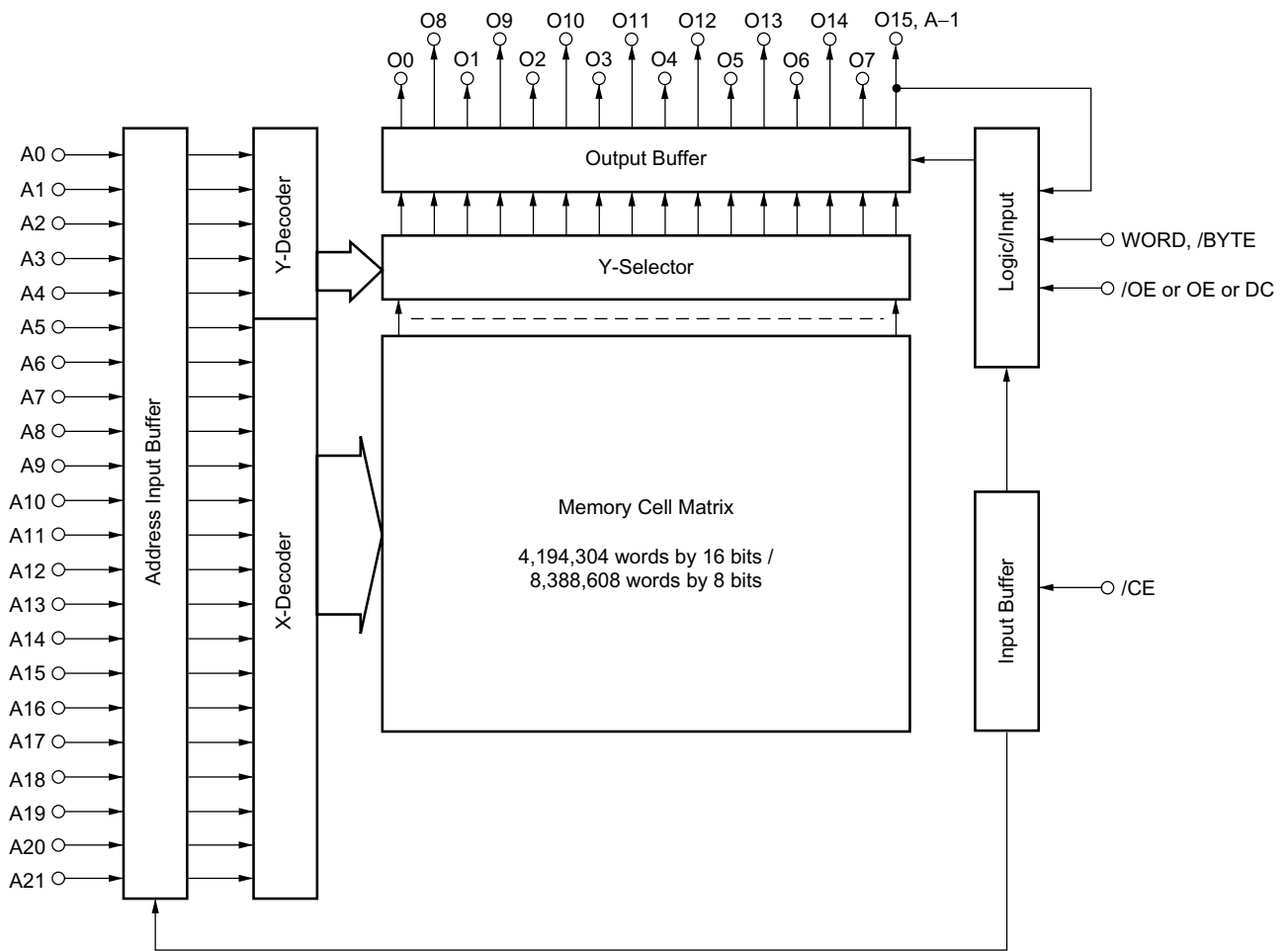
**Note** Some signals can be applied because this pin is not connected to the inside of the chip.

**Remark** Refer to **Package Drawing** for the index mark.

Input / Output Pin Functions

Pin name	Input / Output	Function
WORD, /BYTE	Input	The pin for switching WORD mode and BYTE mode. <b>High level</b> : WORD mode (4M-word by 16-bit) <b>Low level</b> : BYTE mode (8M-word by 8-bit)
A0 to A21 (Address inputs)	Input	Address input pins. A0 to A21 are used differently in the WORD mode and the BYTE mode. <b>WORD mode (4M-word by 16-bit)</b> A0 to A21 are used as 22 bits address signals. <b>BYTE mode (8M-word by 8-bit)</b> A0 to A21 are used as the upper 22 bits of total 23 bits of address signal. (The least significant bit (A-1) is combined to O15.)
O0 to O7, O8 to O14 (Data outputs)	Output	Data output pins. O0 to O7, O8 to O14 are used differently in the WORD mode and the BYTE mode. <b>WORD mode (4M-word by 16-bit)</b> The lower 15 bits of 16 bits data outputs to O0 to O14. (The most significant bit (O15) combined to A-1.) <b>BYTE mode (8M-word by 8-bit)</b> 8 bits data outputs to O0 to O7 and also O8 to O14 are high impedance.
O15, A-1 (Data output 15, LSB Address input)	Output, Input	O15, A-1 are used differently in the WORD mode and the BYTE mode. <b>WORD mode (4M-word by 16-bit)</b> The most significant output data bus (O15). <b>BYTE mode (8M-word by 8-bit)</b> The least significant address bus (A-1).
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. <b>High level</b> : High-Z <b>Low level</b> : Data out
/OE or OE or DC (Output Enable, Don't care)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
Vcc	-	Supply voltage
GND	-	Ground
NC	-	Not internally connected. (The signal can be connected.)

Block Diagram



**Mask Option**

The active levels of output enable pin (/OE or OE or DC) are mask programmable and optional, and can be selected from among " 0 " " 1 " " x " shown in the table below.

Option	/OE or OE or DC	OE active level
0	/OE	L
1	OE	H
x	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High-Z
H	H or L	Standby	High-Z

Operation mode (Option : 1)

/CE	OE	Mode	Output state
L	L	Active	High-Z
	H		Data out
H	H or L	Standby	High-Z

Operation mode (Option : x)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High-Z

**Remark** L : Low level input

H : High level input

**Electrical Specifications**

**Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V <sub>CC</sub>		-0.3 to +4.6	V
Input voltage	V <sub>I</sub>		-0.3 to V <sub>CC</sub> +0.3	V
Output voltage	V <sub>O</sub>		-0.3 to V <sub>CC</sub> +0.3	V
Operating ambient temperature	T <sub>A</sub>		-10 to +70	°C
Storage temperature	T <sub>stg</sub>		-65 to +150	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Capacitance (T<sub>A</sub> = 25 °C)**

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>I</sub>	f = 1 MHz			10	pF
Output capacitance	C <sub>O</sub>				12	pF

**DC Characteristics (T<sub>A</sub> = -10 to +70 °C, V<sub>CC</sub> = 2.7 to 3.6 V)**

Parameter	Symbol	Test conditions		MIN.	TYP.	MAX.	Unit	
High level input voltage	V <sub>IH</sub>			2.0		V <sub>CC</sub> + 0.3	V	
Low level input voltage	V <sub>IL</sub>	V <sub>CC</sub> = 3.0 V ± 0.3 V		-0.3		+0.5	V	
		V <sub>CC</sub> = 3.3 V ± 0.3 V		-0.3		+0.8		
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -100 μA		2.4			V	
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1 mA				0.4	V	
Input leakage current	I <sub>LI</sub>	V <sub>I</sub> = 0 V to V <sub>CC</sub>		-10		+10	μA	
Output leakage current	I <sub>LO</sub>	V <sub>O</sub> = 0 V to V <sub>CC</sub> , Chip deselected		-10		+10	μA	
Power supply current	I <sub>CC1</sub>	/CE = V <sub>IL</sub> (Active mode), I <sub>O</sub> = 0 mA	μPD23C64340	V <sub>CC</sub> = 3.0 V ± 0.3 V			40	mA
				V <sub>CC</sub> = 3.3 V ± 0.3 V			55	
		μPD23C64380	V <sub>CC</sub> = 3.0 V ± 0.3 V			60		
			V <sub>CC</sub> = 3.3 V ± 0.3 V			75		
Standby current	I <sub>CC3</sub>	/CE = V <sub>CC</sub> - 0.2 V (Standby mode)				30	μA	

**AC Characteristics (TA = -10 to +70 °C, Vcc = 2.7 to 3.6 V)**

Parameter	Symbol	Test condition	V <sub>CC</sub> = 3.0 V ± 0.3 V			V <sub>CC</sub> = 3.3 V ± 0.3 V			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Address access time	t <sub>ACC</sub>				100			90	ns
Page access time	t <sub>PAC</sub>				25			25	ns
Address skew time	t <sub>SKEW</sub>	<b>Note</b>			10			10	ns
Chip enable access time	t <sub>CE</sub>				100			90	ns
Output enable access time	t <sub>OE</sub>				25			25	ns
Output hold time	t <sub>OH</sub>		0			0			ns
Output disable time	t <sub>DF</sub>		0		25	0		25	ns
WORD, /BYTE access time	t <sub>WB</sub>				100			90	ns

**Note** t<sub>SKEW</sub> indicates the following three types of time depending on the condition.

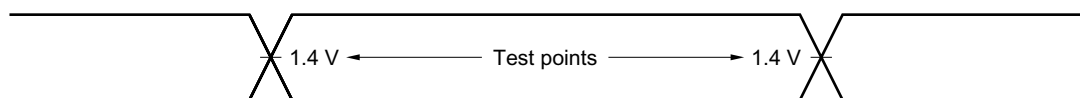
- 1) When switching /CE from high level to low level, t<sub>SKEW</sub> is the time from the /CE low level input point until the next address is determined.
- 2) When switching /CE from low level to high level, t<sub>SKEW</sub> is the time from the address change start point to the /CE high level input point.
- 3) When /CE is fixed to low level, t<sub>SKEW</sub> is the time from the address change start point until the next address is determined.

Since specs are defined for t<sub>SKEW</sub> only when /CE is active, t<sub>SKEW</sub> is not subject to limitations when /CE is switched from high level to low level following address determination, or when the address is changed after /CE is switched from low level to high level.

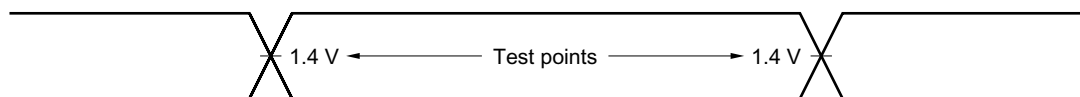
**Remark** t<sub>DF</sub> is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

**AC Test Conditions**

**Input waveform (Rise / Fall time ≤ 5 ns)**



**Output waveform**



**Output load**

1TTL + 100 pF

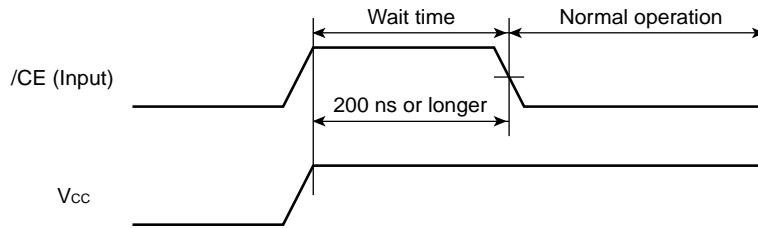


**Cautions on power application**

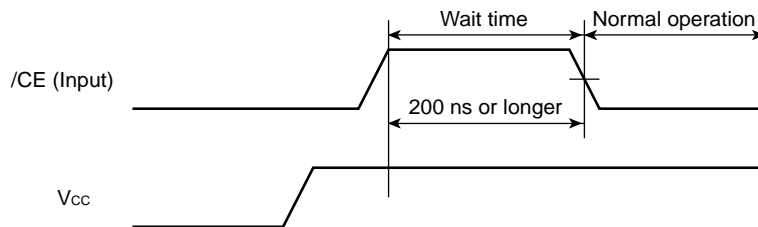
To ensure normal operation, always apply power using /CE following the procedure shown below.

- 1) Input a high level to /CE during and after power application.
- 2) Hold the high level input to /CE for 200 ns or longer (wait time).
- 3) Start normal operation after the wait time has elapsed.

**Power Application Timing Chart 1 (When /CE is made high at power application)**

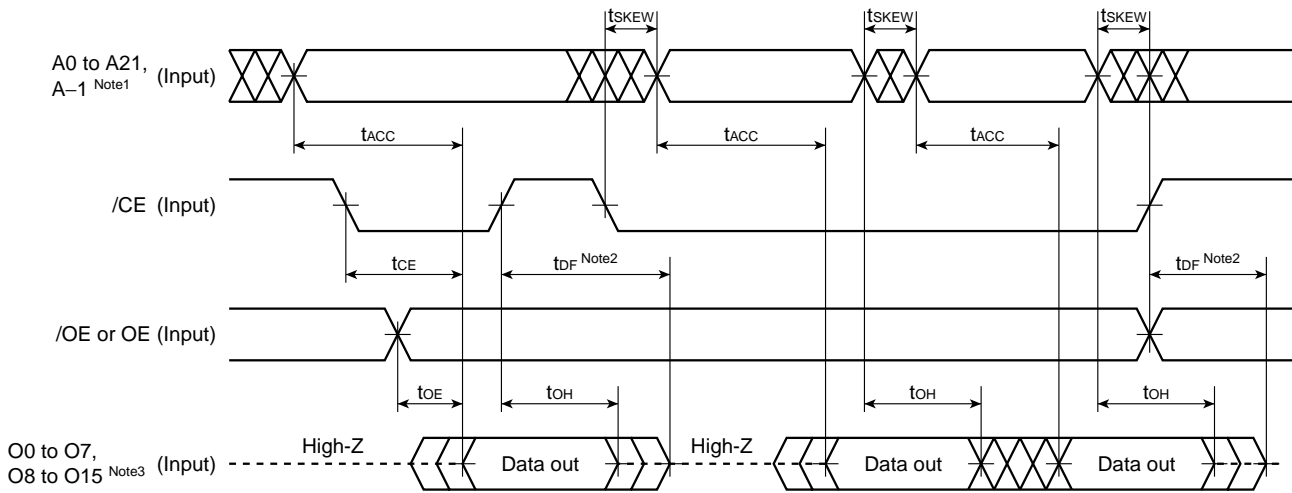


**Power Application Timing Chart 2 (When /CE is made high after power application)**



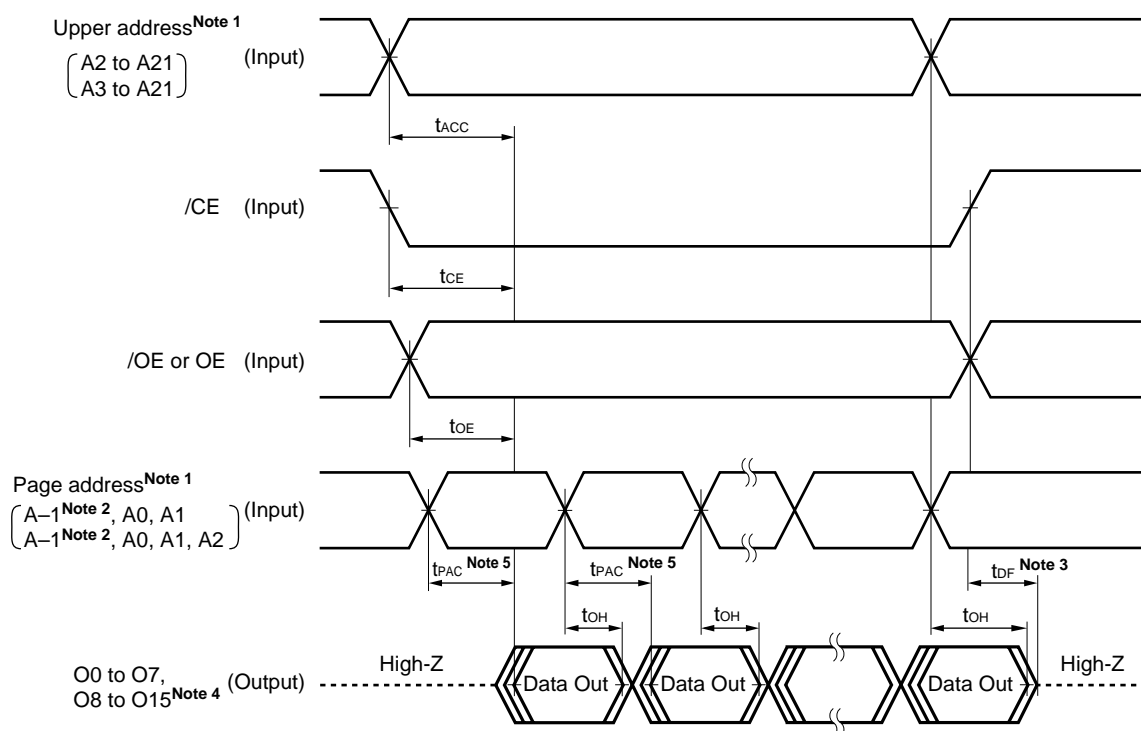
**Caution** Other signals can be either high or low during the wait time.

Read Cycle Timing Chart 1



- Notes**
1. During WORD mode, A-1 is O15.
  2.  $t_{DF}$  is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.
  3. During BYTE mode, O8 to O14 are high impedance and O15 is A-1.

Read Cycle Timing Chart 2 (Page Access Mode)



Notes 1. The address differs depending on the product as follows.

Part Number	Upper address	Page address
$\mu$ PD23C64340	A2 to A21	A-1, A0, A1
$\mu$ PD23C64380	A3 to A21	A-1, A0, A1, A2

- During WORD mode, A-1 is O15.
- $t_{DF}$  is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.
- During BYTE mode, O8 to O14 are high impedance and O15 is A-1.
- The definition of page access time is as follows.

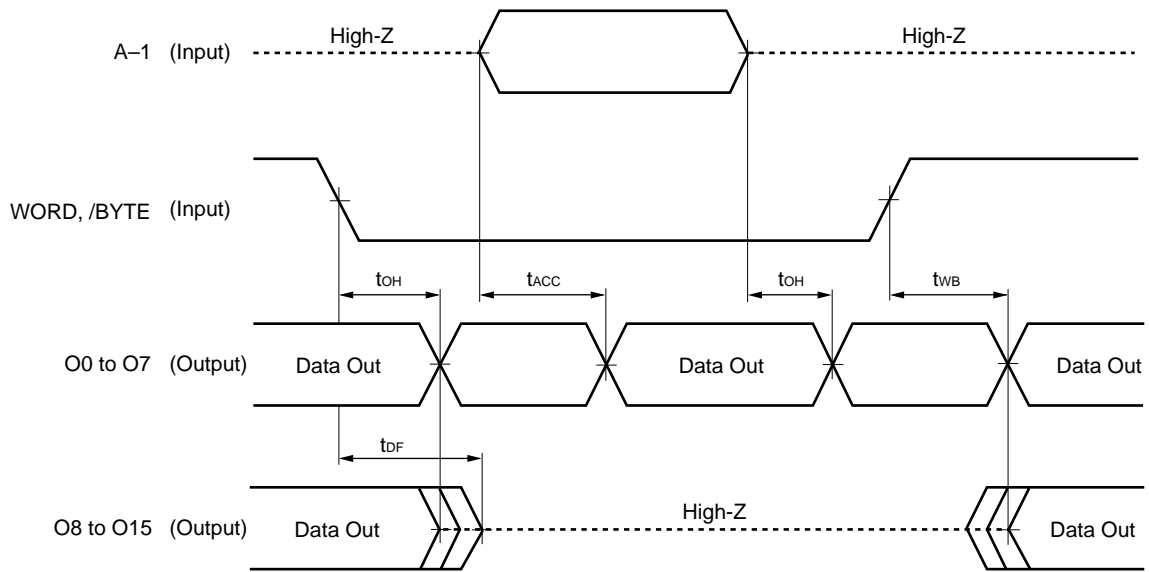
[  $\mu$ PD23C64340 ]

Page access time	Upper address (A2 to A21) inputs condition	/CE input condition	/OE or OE input condition
$t_{PAC}$	Before $t_{ACC} - t_{PAC}$	Before $t_{CE} - t_{PAC}$	Before stabilizing of page address (A-1, A0, A1)

[  $\mu$ PD23C64380 ]

Page access time	Upper address (A3 to A21) inputs condition	/CE input condition	/OE or OE input condition
$t_{PAC}$	Before $t_{ACC} - t_{PAC}$	Before $t_{CE} - t_{PAC}$	Before stabilizing of page address (A-1, A0, A1, A2)

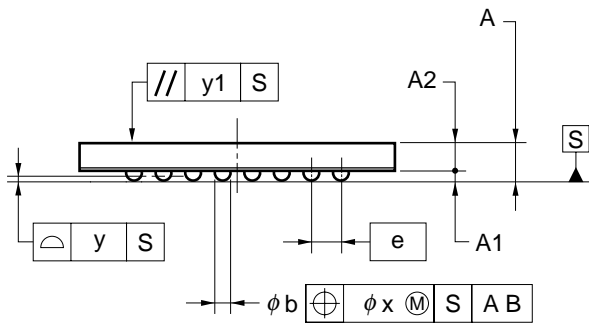
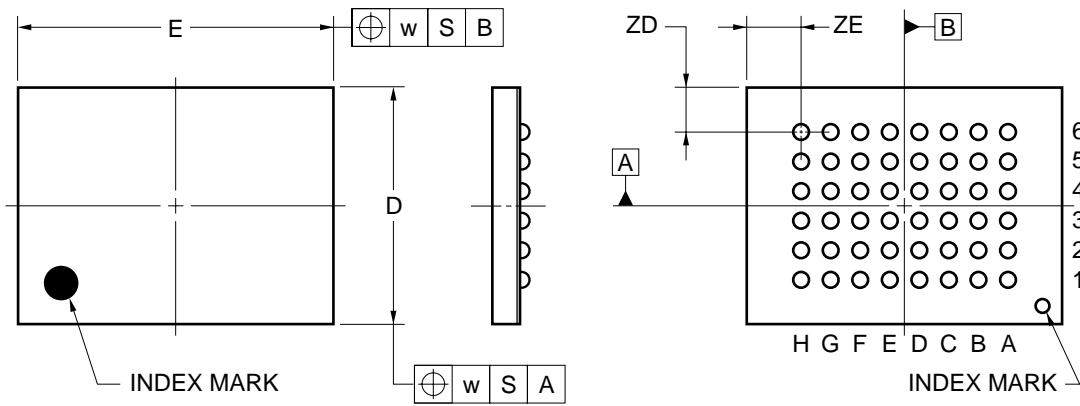
**WORD, /BYTE Switch Timing Chart**



**Remark** Chip Enable ( $/CE$ ) and Output Enable ( $/OE$  or  $OE$ ) : Active.

Package Drawing

48-PIN TAPE FBGA(8x6)



ITEM	MILLIMETERS
D	6.0±0.1
E	8.0±0.1
w	0.2
e	0.80
A	0.97±0.10
A1	0.27±0.05
A2	0.70
b	0.45±0.05
x	0.08
y	0.1
y1	0.2
ZD	1.00
ZE	1.20

P48F9-80-BC3

**Recommended Soldering Conditions**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD23C64340 and  $\mu$ PD23C64380.

**Types of Surface Mount Device**

$\mu$ PD23C64340F9-BC3 : 48-pin TAPE FBGA (8 x 6)

$\mu$ PD23C64380F9-BC3 : 48-pin TAPE FBGA (8 x 6)

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
3rd edition/ Feb. 2004	Throughout	Throughout	Deletion	Ordering Information	μPD23C64340GZ-xxx-MJH μPD23C64380GZ-xxx-MJH
				Package	48-pin PLASTIC TSOP (I) (12 x 20) (Normal bent)

[MEMO]



[MEMO]

[MEMO]

## NOTES FOR CMOS DEVICES

**① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

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