CONVERTING AEROFLEX UTMC UT9Q512 4M SRAM into an SEU IMMUNE 1M X 1 SRAM

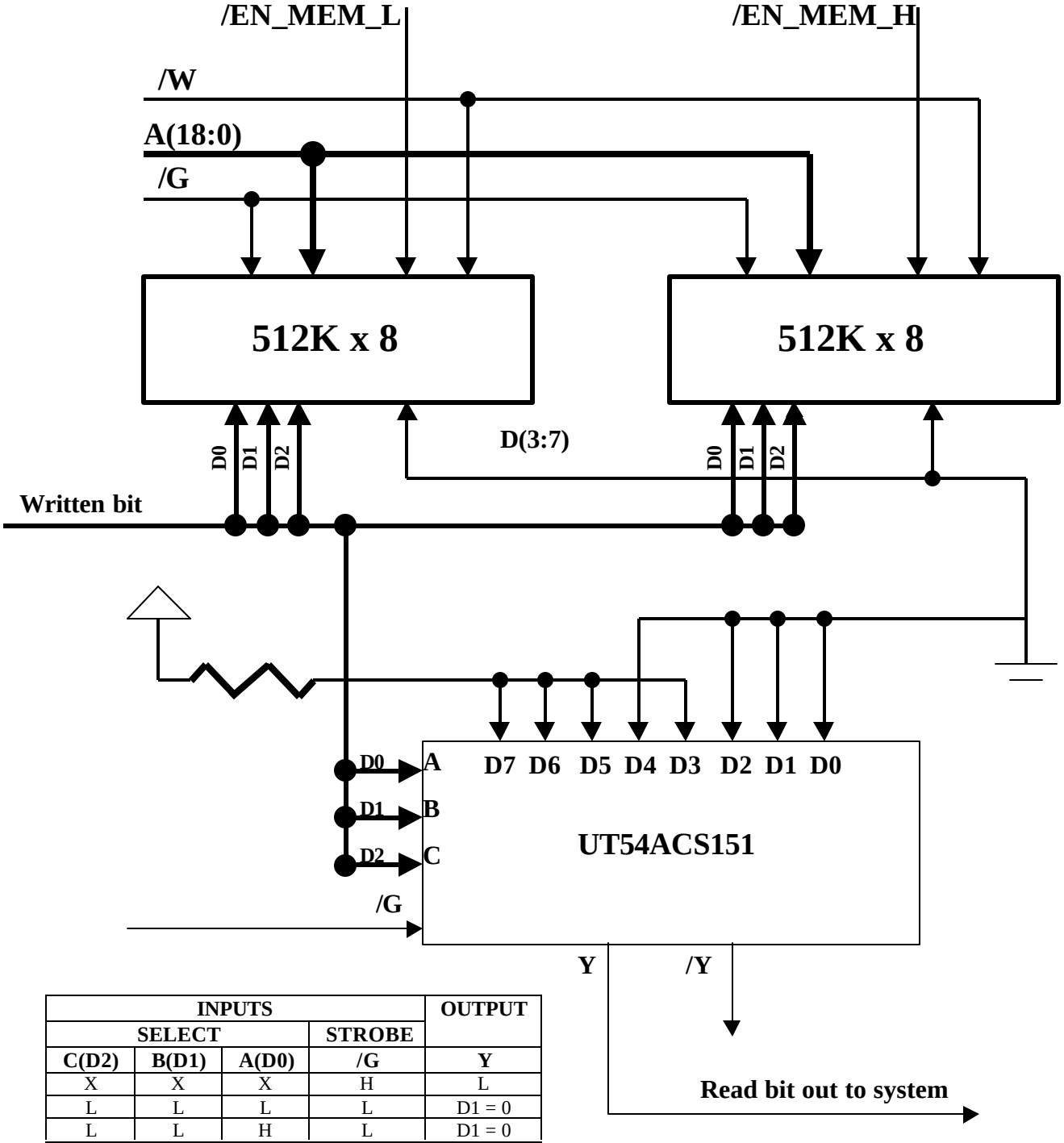
This application note describes how to use two UT9Q512 4M SRAMs and one UT54ACS151 logic device to mimic a 1Mx1 SRAM. As shown below, the single bit is written into three locations of the same. When the data is read out, it is used in a voting system to select either a 0 or a 1 output. This voting method virtually makes it immune to SEU hits. Since the bits of a word are not physically adjacent on the die, it is nearly impossible for one particle to cause two bits to flip in the same word. As such, it would require multiple particle hits to cause an upset.

The system timing results in maximum read cycle of 48ns, (25ns SRAM read + 23ns input to Y). For better system performance Aeroflex UTMC can screen for memories with read cycles access times down to 17 ns. The timing analysis above assumes capacitive output loads of 50 pF or less. If the system loading is greater than 50 pF, the user should consult the "Operational Frequency vs. Load Capacitance" application note to calculate the true performance of the design. This application note can be downloaded from: http://www.utmc.com/products/msi_switch.pdf.

If a tri-statable output is required, then additional logic would be required. Aeroflex UTMC has the following logic devices with tristate controlled outputs: UT54ACS244, UT54ACS245, UT54ACS365, UT54ACS373, UT54ACS374, and UT54ACS541. Each of these devices has a non-inverting tri-statable output.

If the 4M SRAMs are packaged in our shielded package, they can withstand a total dose of 100K rads(Si) in most orbits. The logic devices can be purchased with a total dose hardness ranging from 100K rads(Si) to 1 Mrad.

This design example requires more board real estate and a new board layout, along with the additional timing analysis, mentioned above, to replace the obsoleted BAE Systems 1M x 1 SRAM parts. The parts shown would use approximately 1.75 square inches of board space.



INPUTS				OUTPUT
SELECT			STROBE	
C(D2)	B(D1)	A(D0)	/G	Y
X	X	X	H	L
L	L	L	L	D1 = 0
L	L	H	L	D1 = 0
L	H	L	L	D2 = 0
L	H	H	L	D3 = 1
H	L	L	L	D4 = 0
H	L	H	L	D5 = 1
H	H	L	L	D6 = 1
H	H	H	L	D7 = 1

Truth Table