WM8759

24-bit 192kHz Stereo DAC with Headphone Buffer

DESCRIPTION

The WM8759 is a high performance stereo DAC with an integrated headphone driver. It is designed for audio applications such as portable DVD, MP3 players or consumer equipment with line output and headphone output connections.

The WM8759 supports data input word lengths from 16 to 24-bits and sampling rates up to 192kHz. The WM8759 consists of a serial interface port, digital interpolation filters, multi-bit sigma delta modulators and stereo DAC in a 14-pin SOIC package.

The hardware control interface is used for the selection of audio data interface format, enable and de-emphasis. The WM8759 supports I^2S, right Justified or DSP interfaces.

Operating on split analog digital supplies the WM8759 allows very lower power consumption from the digital section, whilst supporting large output powers from the analog headphone driver.

FEATURES

- Stereo DAC with headphone driver
- 50mW power into 16R load on 3.3V supply
- Audio Performance
  - 100dB SNR ('A' weighted @ 48kHz)
  - -88dB THD line level
  - -72dB THD headphone
- DAC Sampling Frequency: 8kHz – 192kHz
- Pin Selectable Audio Data Interface Format
  - I^2S, 16-bit Right Justified or DSP
- 2.7V - 5.5V Supply Operation, Split Analog-digital supplies
- 14-lead SOIC Package
- Typical power consumption 20mW on 2.7V supply

APPLICATIONS

- Portable music Players
- Home music players
- Digital TV

BLOCK DIAGRAM

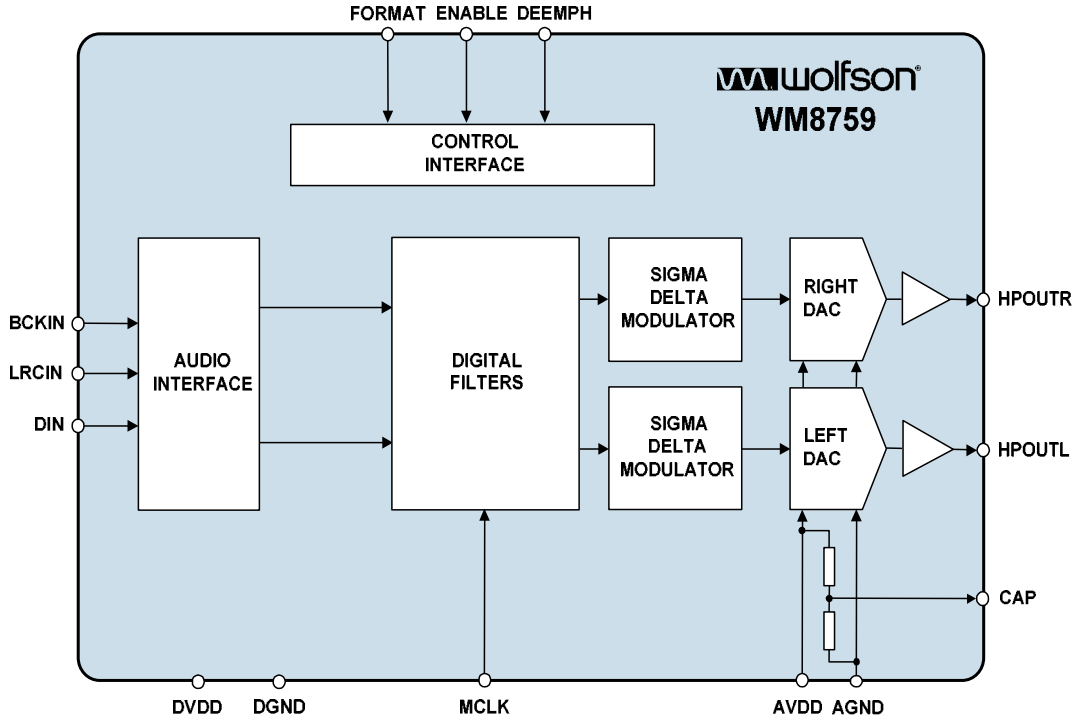
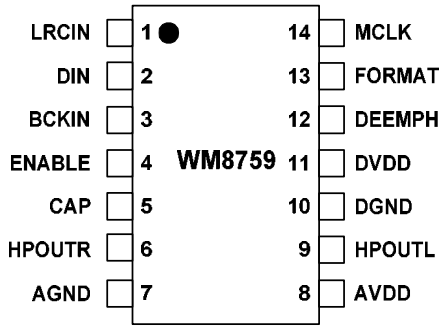


TABLE OF CONTENTS

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8759GED/V	-25 to +85°C	14-lead SOIC (Pb-free)	MSL3	260°C
WM8759GED/RV	-25 to +85°C	14-lead SOIC (Pb-free, tape and reel)	MSL3	260°C

Note:
Reel quantity = 3,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	LRCIN	Digital input	Sample rate clock input
2	DIN	Digital input	Serial audio data input
3	BCKIN	Digital input	Bit clock input
4	ENABLE	Digital input	Enable input – 0 = powered down, 1 = enabled
5	CAP	Analogue output	Analogue internal reference
6	HPOUTR	Analogue output	Right channel DAC output
7	AGND	Supply	Ground reference for analog circuits and substrate connection
8	AVDD	Supply	Positive supply for analog circuits
9	HPOUTL	Analogue output	Left channel DAC output
10	DGND	Digital Supply	Digital ground supply
11	DVDD	Digital Supply	Digital positive supply
12	DEEMPH	Digital input	De-emphasis select, Internal pull down High = de-emphasis ON Low = de-emphasis OFF
13	FORMAT	Digital input	Data input format select, Internal pull up Low = 16-bit right justified or DSP 'late' High = 16-24-bit I^2S or DSP 'early'
14	MCLK	Digital input	Master clock input

Note:

1. Digital input pins have Schmitt trigger input buffers.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltage	-0.3V	+7V
Voltage range digital inputs	GND -0.3V	VDD +0.3V
Master Clock Frequency		50MHz
Operating temperature range, T_A	-25°C	+85°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply range	AVDD, DVDD		2.7		5.5	V
Ground	AGND, DGND			0		V
Analog supply current		AVDD = 5V		12		mA
		AVDD = 3.3V				
Digital supply current		DVDD = 5V		8		mA
		DVDD = 3.3V		4		
Power down current (note 4)		AVDD=DVDD=5V		0.01		mA

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 5V, DVDD = 3.3V, GND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2.0			V
Output LOW	V_{OL}	I_{OL} = 2mA			DGND + 0.3V	V
Output HIGH	V_{OH}	I_{OH} = 2mA	DVDD – 0.3V			V
Analogue Reference Levels						
Reference voltage (CAP)				AVDD/2		V
Potential divider resistance	R_{CAP}	AVDD to CAP and CAP to GND		50k		Ω
DAC Output (Load = 10kΩ. 50pF)						
0dBFs Full scale output voltage		At DAC outputs		1.1 x AVDD/5		Vrms
SNR (Note 5,6,7)		A-weighted, @ fs = 48kHz	94	100		dB
SNR (Note 5,6,7)		A-weighted @ fs = 96kHz		97		dB
SNR (Note 5,6,7)		A-weighted @ fs = 192kHz		97		dB
SNR (Note 5,6,7)		A-weighted, @ fs = 48kHz VDD = 3.3V		95		dB
SNR (Note 5,6,7)		A-weighted @ fs = 96kHz VDD = 3.3V		95		dB
SNR (Note 5,6,7)		Non 'A' weighted @ fs = 48kHz		97		dB
THD+N (Note 7)	10k load	1kHz, 0dBFs		-88		dB
THD+N driving headphone	16R load	1kHz, 0dBFs		-72		dB
DAC channel separation				93		dB

Test Conditions

AVDD = 5V, DVDD = 3.3V, GND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Output Levels						
Output level		Load = 10kΩ, 0dBFS		1.1		Vrms
		Load = 10kΩ, 0dBFS, (AVDD = 3.3V)		0.72		Vrms
Gain mismatch channel-to-channel				±1		%FSR
Minimum resistance load		To midrail or a.c. coupled		16		Ω
		To midrail or a.c. coupled (AVDD = 3.3V)		16		Ω
Output d.c. level				AVDD/2		V

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. CAP pin decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).
4. Power down occurs 1.5µs after MCLK is stopped.
5. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
6. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
7. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
8. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
9. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

MASTER CLOCK TIMING

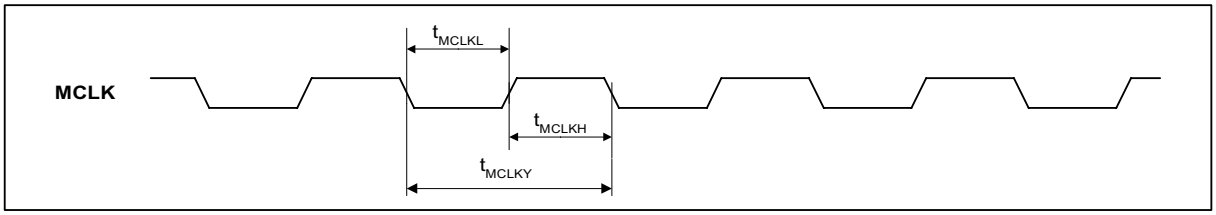


Figure 1 Master Clock Timing Requirements

Test Conditions

VDD = 5V, GND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK Master clock pulse width high	t_{MCLKH}		8			ns
MCLK Master clock pulse width low	t_{MCLKL}		8			ns
MCLK Master clock cycle time	t_{MCLKY}		20			ns
MCLK Duty cycle			40:60		60:40	
Time from MCLK stopping to power down.			1.5		12	µs

DIGITAL AUDIO INTERFACE

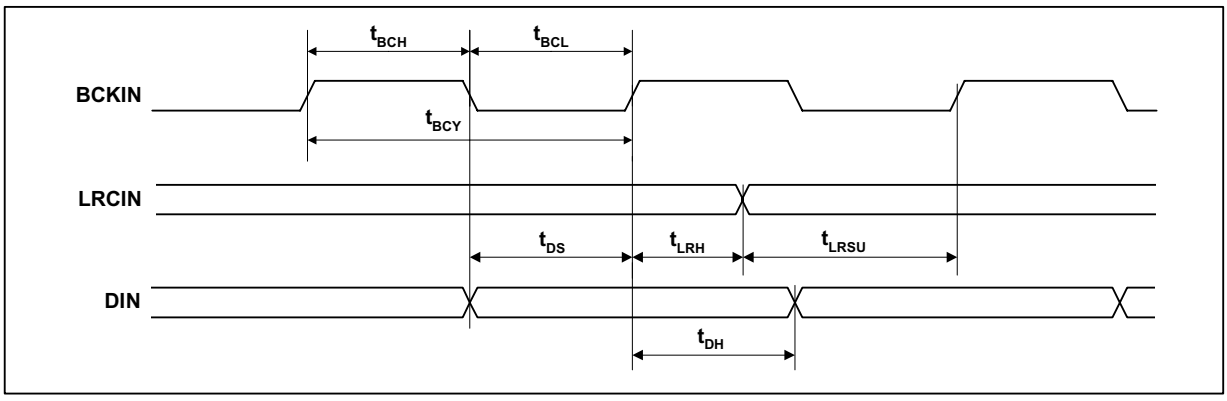


Figure 2 Digital Audio Data Timing

Test Conditions

VDD = 5V, GND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCKIN cycle time	t_{BCY}		40			ns
BCKIN pulse width high	t_{BCH}		16			ns
BCKIN pulse width low	t_{BCL}		16			ns
LRCIN set-up time to BCKIN rising edge	t_{LRSU}		8			ns
LRCIN hold time from BCKIN rising edge	t_{LRH}		8			ns
DIN set-up time to BCKIN rising edge	t_{DS}		8			ns
DIN hold time from BCKIN rising edge	t_{DH}		8			ns

DEVICE DESCRIPTION

GENERAL INTRODUCTION

The WM8759 is a high performance DAC with integrated headphone output buffer, designed for digital consumer audio applications. The range of features make it ideally suited for use in portable DVD players, MP3 players and other consumer audio equipment.

The WM8759 is a complete 2-channel stereo audio digital-to-analogue converter, including digital interpolation filter, multi-bit sigma delta with dither, and switched capacitor multi-bit stereo DAC and output smoothing filters. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs. A novel multi bit sigma-delta DAC design is used, utilising a 128x oversampling rate, to optimise signal to noise performance and offer increased clock jitter tolerance. (In 'high-rate' operation, the oversampling ratio is 64x for system clocks of 128fs or 192fs)

Control of the internal functionality of the device is provided by hardware control (pin programmed).

Operation using master clocks of 256fs, 384fs, 512fs or 768fs is provided, selection between clock rates being automatically controlled. Sample rates (fs) from less than 8kHz to 96kHz are allowed, provided the appropriate system clock is input. Support is also provided for up to 192kHz using a master clock of 128fs or 192fs.

The audio data interface supports 16-bit right justified or 16-24-bit I^2S (Philips left justified, one bit delayed) interface formats. A DSP interface is also supported, enhancing the interface options for the user.

Split analog and digital 2.7-5.5V supply may be used, the output amplitude scaling with absolute analog supply level. Low supply voltage operation and low current consumption combined with the low pin count small package make the WM8759 attractive for many consumer applications. A power down mode is provided, allowing power consumption to be minimised.

The device is packaged in a small 14-pin SOIC.

DAC CIRCUIT DESCRIPTION

The WM8759 DAC is designed to allow playback of 24-bit PCM audio or similar data with high resolution and low noise and distortion. Sample rates up to 192kHz may be used, with much lower sample rates being acceptable provided that the ratio of sample rate (LRCIN) to master clock (MCLK) is maintained at one of the required rates.

The two DACs on the WM8759 are implemented using sigma-delta oversampled conversion techniques. These require that the PCM samples are digitally filtered and interpolated to generate a set of samples at a much higher rate than the up to 192kHz input rate. This sample stream is then digitally modulated to generate a digital pulse stream that is then converted to analogue signals in a switched capacitor DAC.

The advantage of this technique is that the DAC is linearised using noise shaping techniques, allowing the 24-bit resolution to be met using non-critical analogue components. A further advantage is that the high sample rate at the DAC output means that smoothing filters on the output of the DAC need only have fairly crude characteristics in order to remove the characteristic steps, or images on the output of the DAC. To prevent the generation of unwanted tones dithering is used in the digital modulator along with a higher order modulator.

The multi-bit switched capacitor technique used in the DAC reduces sensitivity to clock jitter, and dramatically reduces out of band noise compared to switched current or single bit techniques used in other implementations.

The voltage on the CAP pin is used as the reference for the DACs. Therefore the amplitude of the signals at the DAC outputs will scale with the amplitude of the voltage at the CAP pin. An external reference could be used to drive into the CAP pin if desired, with a value typically of about midrail ideal for optimum performance.

The outputs of the 2 DACs are buffered out of the device by buffer amplifiers capable of driving loads of either line level or headphone level impedance. The advanced multi-bit DAC used in WM8759 produces far less out of band noise than single bit traditional sigma delta DACs, and so in most applications where line level output is required, no post DAC filter is required. Typically an AC coupling capacitor and a DC setting resistor to ground are the only components required on the output of the chip.

CLOCKING SCHEMES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master clock can be applied directly through the MCLK input pin with no configuration necessary for sample rate selection.

Note that on the WM8759, MCLK is used to derive clocks for the DAC path. The DAC path consists of DAC sampling clock, DAC digital filter clock and DAC digital audio interface timing. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the DAC.

The device can be powered down by stopping MCLK. In this state the power consumption is substantially reduced.

DIGITAL AUDIO INTERFACE

Audio data is applied to the internal DAC filters via the Digital Audio Interface. Three interface formats are supported:

- Right Justified mode
- I^2S mode
- DSP mode

All formats send the MSB first. The data format is selected with the FORMAT pin. When FORMAT is LOW, right justified data format is selected and word lengths of 16-bits may be used. When the FORMAT pin is HIGH, I^2S format is selected and word length of any value up to 24-bits may be used. (If a word length shorter than 24-bits is used, the unused bits should be padded with zeros). If LRCIN is 4 BCKINs or less duration, the DSP compatible format is selected. Early and Late clock formats are supported, selected by the state of the FORMAT pin.

'Packed' mode (i.e. only 32 or 48 clocks per LRCIN period) operation is also supported in both I^2S (16-24 bits) and right justified formats, (16 bit). If a 'packed' format of 16-bit word length is applied (16 BCKINS per LRCIN half period), the device auto-detects this mode and switches to 16-bit data length.

I^2S MODE

The WM8759 supports word lengths of 16-24 bits in I^2S mode.

In I^2S mode, the digital audio interface receives data on the DIN input. Audio Data is time multiplexed with LRCIN indicating whether the left or right channel is present. LRCIN is also used as a timing reference to indicate the beginning or end of the data words.

In I^2S modes, the minimum number of BCKINs per LRCIN period is 2 times the selected word length. LRCIN must be high for a minimum of word length BCKINs and low for a minimum of word length BCKINs. Any mark to space ratio on LRCIN is acceptable provided the above requirements are met. In I^2S mode, the MSB is sampled on the second rising edge of BCKIN following a LRCIN transition. LRCIN is low during the left samples and high during the right samples.

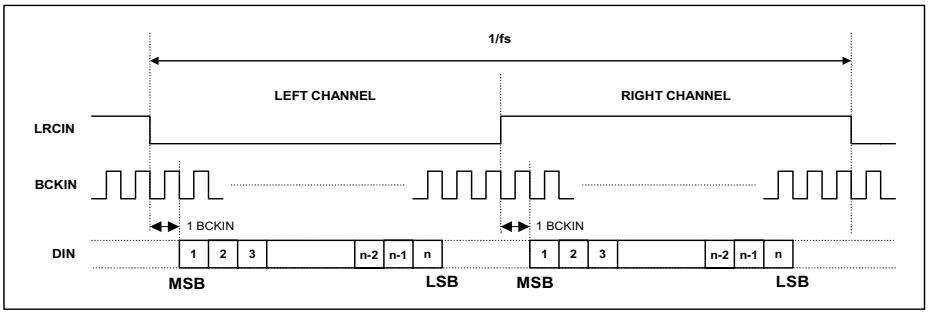


Figure 3 I²S Mode Timing Diagram

RIGHT JUSTIFIED MODE

The WM8759 supports word lengths of 16-bits in right justified mode.

In right justified mode, the digital audio interface receives data on the DIN input. Audio Data is time multiplexed with LRCIN indicating whether the left or right channel is present. LRCIN is also used as a timing reference to indicate the beginning or end of the data words.

In right justified mode, the minimum number of BCKINs per LRCIN period is 2 times the selected word length. LRCIN must be high for a minimum of word length BCKINs and low for a minimum of word length BCKINs. Any mark to space ratio on LRCIN is acceptable provided the above requirements are met.

In right justified mode, the LSB is sampled on the rising edge of BCKIN preceding a LRCIN transition. LRCIN is high during the left samples and low during the right samples.

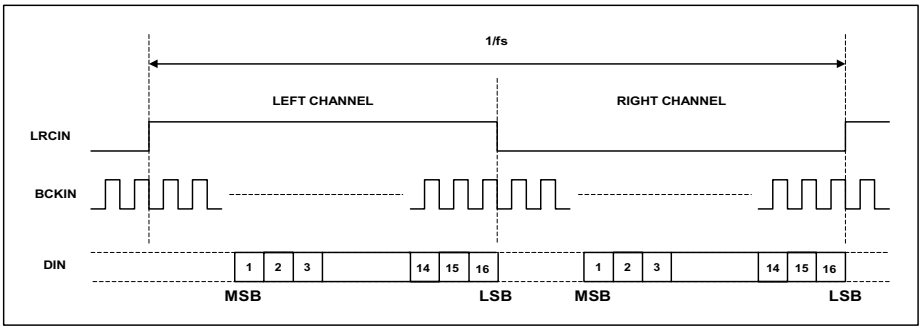


Figure 4 Right Justified Mode Timing Diagram

DSP MODE

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 5 and Figure 6. In device slave mode, Figure 7 and Figure 8, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

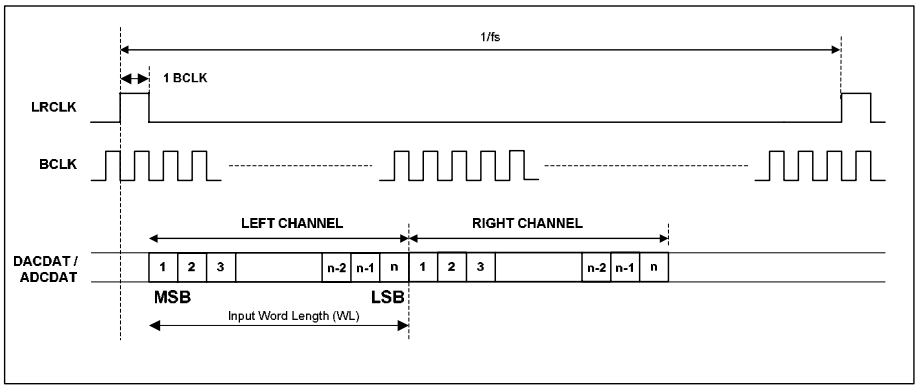


Figure 5 DSP/PCM Mode Audio Interface (mode A, LRP=0, Master)

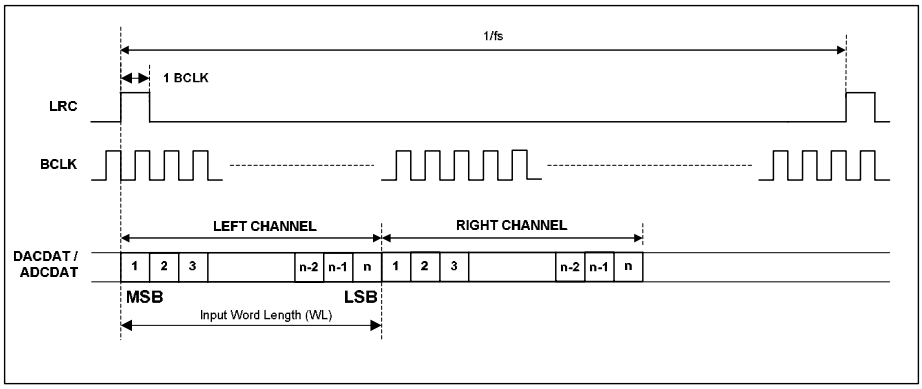


Figure 6 DSP/PCM Mode Audio Interface (mode B, LRP=1, Master)

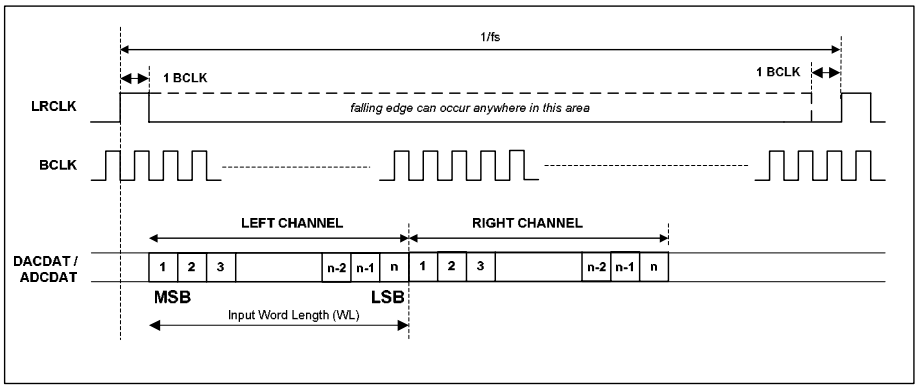


Figure 7 DSP/PCM Mode Audio Interface (mode A, LRP=0, Slave)

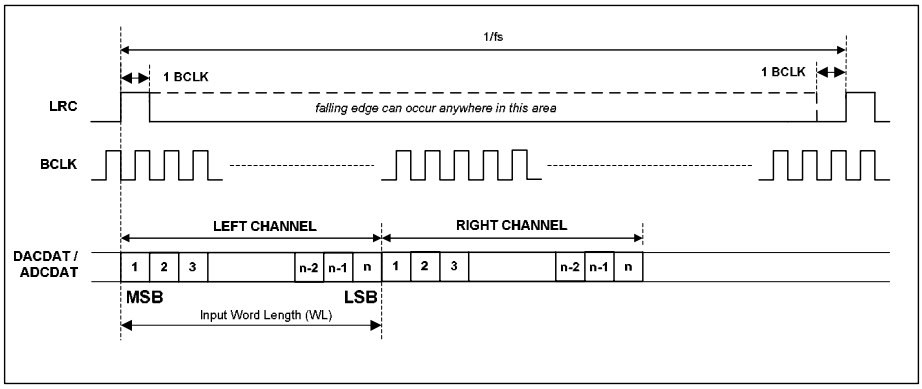


Figure 8 DSP/PCM Mode Audio Interface (mode B, LRP=0, Slave)

AUDIO DATA SAMPLING RATES

The master clock for WM8759 supports audio sampling rates from 128fs to 768fs, where fs is the audio sampling frequency (LRCIN) typically 32kHz, 44.1kHz, 48kHz, 96kHz or 192kHz. The master clock is used to operate the digital filters and the noise shaping circuits.

The WM8759 has a master clock detection circuit that automatically determines the relation between the master clock frequency and the sampling rate (to within +/- 8 master clocks). If there is a greater than 8 clocks error, the interface shuts down the DAC and mutes the output. The master clock should be synchronised with LRCIN, although the WM8759 is tolerant of phase differences or jitter on this clock.

SAMPLING RATE (LRCIN)	MASTER CLOCK FREQUENCY (MHZ) (MCLK)					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9344	22.5792	33.8688
48kHz	6.144	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 1 Master Clock Frequencies Versus Sampling Rate

HARDWARE CONTROL MODES

The WM8759 is hardware programmable providing the user with options to select input audio data format, de-emphasis and mute.

ENABLE OPERATION

Pin 4 (ENABLE) controls the operation of the chip. If ENABLE is low the device is held in a low power state. If this pin is held high the device is powered up.

To ensure correct operation it is essential that there is a low to high transition on the ENABLE pin after digital supplies have come on. This can be achieved by providing the ENABLE signal from an external controller chip or by means of a simple RC network on the ENABLE pin. See "Recommended External Components" in the "Application Information" section at the end of this datasheet.

Note that the ENABLE pin should not be used as a mute pin or to temporarily silence the DAC (between tracks of a CD for example). The ENABLE pin is not intended to be used as a mute control but to allow entry into low power mode. Disabling the device via the ENABLE pin has the effect of powering down the voltage on the CAP pin. Repeated enabling/disabling of the device can cause audible pops at the output.

HIGH PERFORMANCE MODE

On the rising edge of ENABLE, the DEEMPH pin is sampled. If it is low the device powers up normally. If it is high the device goes into a high performance and high power consumption state. Once ENABLE is high, DEEMPH controls the selection of the de-emphasis filter.

INPUT AUDIO FORMAT SELECTION

FORMAT (pin 13) controls the data input format.

FORMAT	INPUT DATA MODE
0	16 bit right justified
1	16–24 bit I^2S

Table 2 Input Audio Format Selection

Notes:

1. In 16-24 bit I^2S mode, any data from 16-24 bits or more is supported provided that LRCIN is high for a minimum of data width BCKINs and low for a minimum of data width BCKINs, unless Note 2. For data widths greater than 24 bits, the LSB's will be truncated and the most significant 24 bits will be used by the internal processing.
2. If exactly 16 BCKIN cycles occur in both the low and high period of LRCIN the WM8759 will assume the data is 16-bit and accept the data accordingly.

INPUT DSP FORMAT SELECTION

FORMAT	50% LRCIN DUTY CYCLE	LRCIN of 4 BCKIN or Less Duration
0	16 bit (MSB-first, right justified)	DSP format – 'late' mode
1	I^2S format up to 24 bit (Philips serial data protocol)	DSP format – 'early' mode

Table 3 DSP Interface Formats

DE-EMPHASIS CONTROL

DEEMPH (pin 12) is an input control for selection of de-emphasis filtering to be applied.

DEEMPH	DE-EMPHASIS
0	Off
1	On

Table 4 De-emphasis Control

DIGITAL FILTER CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband Edge		-3dB		0.487fs		
Passband Ripple		f < 0.444fs			±0.05	dB
Stopband Attenuation		f > 0.555fs	-60			dB

Table 5 Digital Filter Characteristics

DAC FILTER RESPONSES

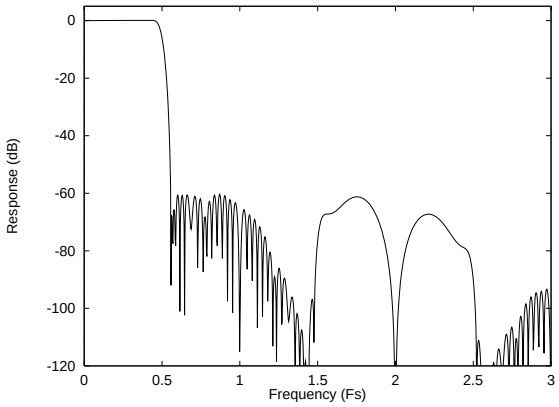


Figure 9 DAC Digital Filter Frequency Response -44.1, 48 and 96kHz

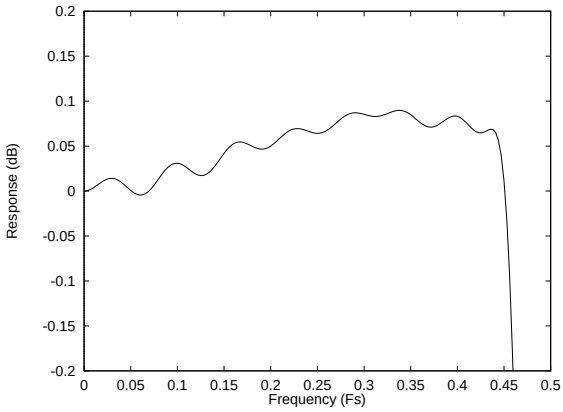


Figure 10 DAC Digital Filter Ripple -44.1, 48 and 96kHz

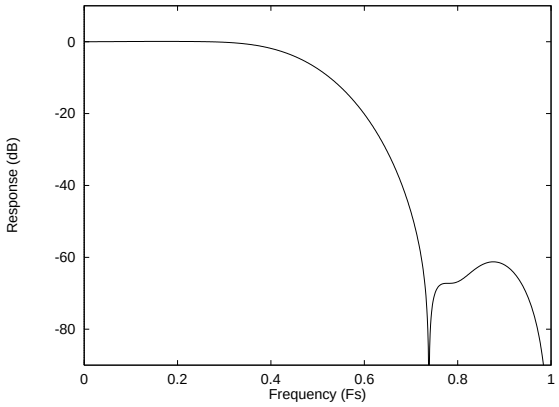


Figure 11 DAC Digital Filter Frequency Response -192kHz

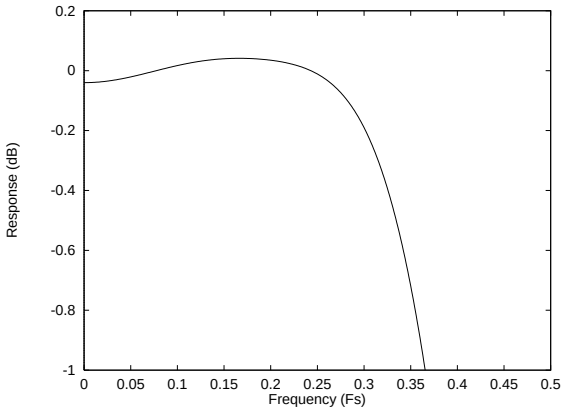


Figure 12 DAC Digital Filter Ripple -192kHz

DIGITAL DE-EMPHASIS CHARACTERISTICS

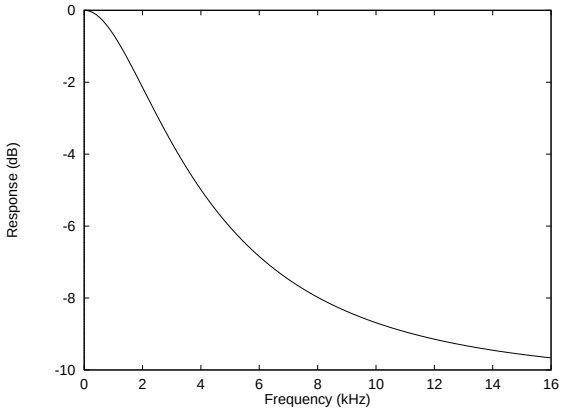


Figure 13 De-Emphasis Frequency Response (32kHz)

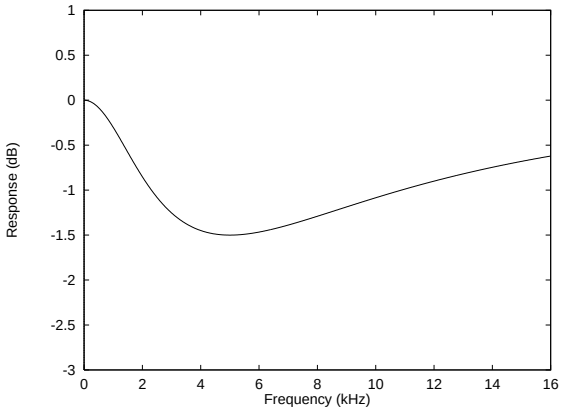


Figure 14 De-Emphasis Error (32kHz)

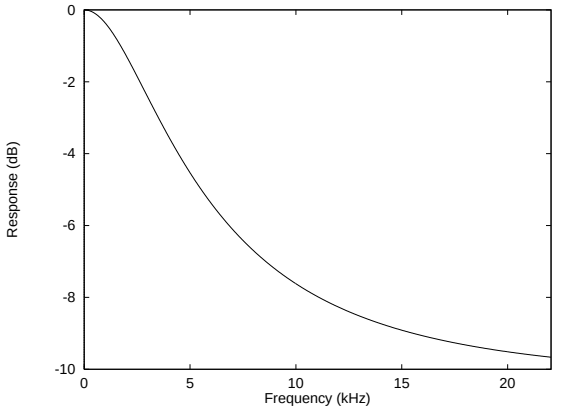


Figure 15 De-Emphasis Frequency Response (44.1kHz)

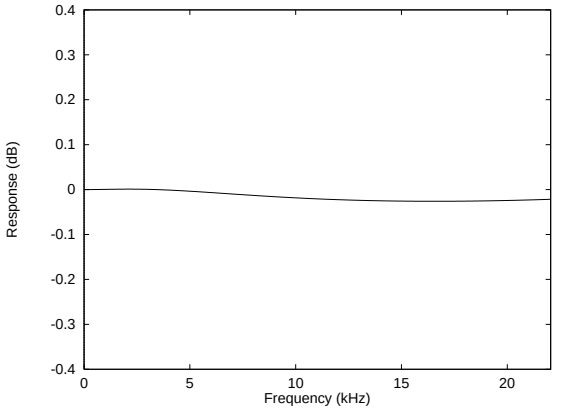


Figure 16 De-Emphasis Error (44.1kHz)

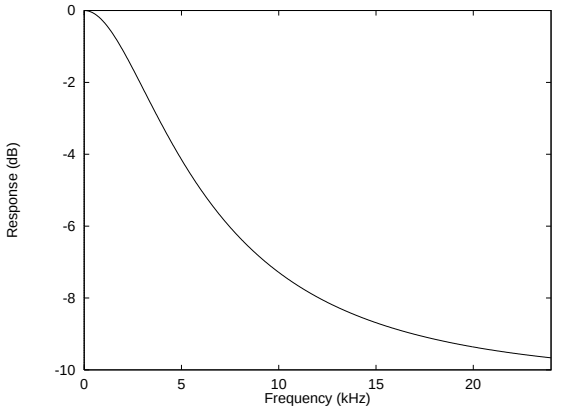


Figure 17 De-Emphasis Frequency Response (48kHz)

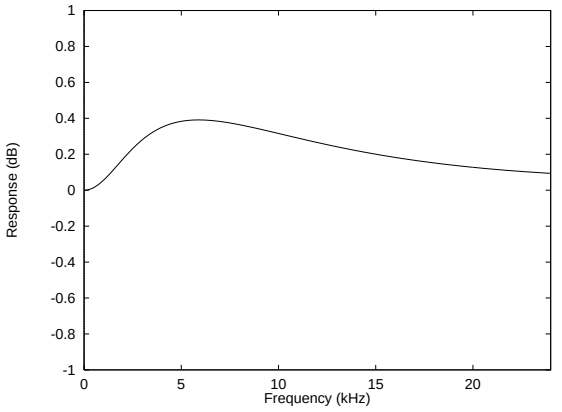


Figure 18 De-Emphasis Error (48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

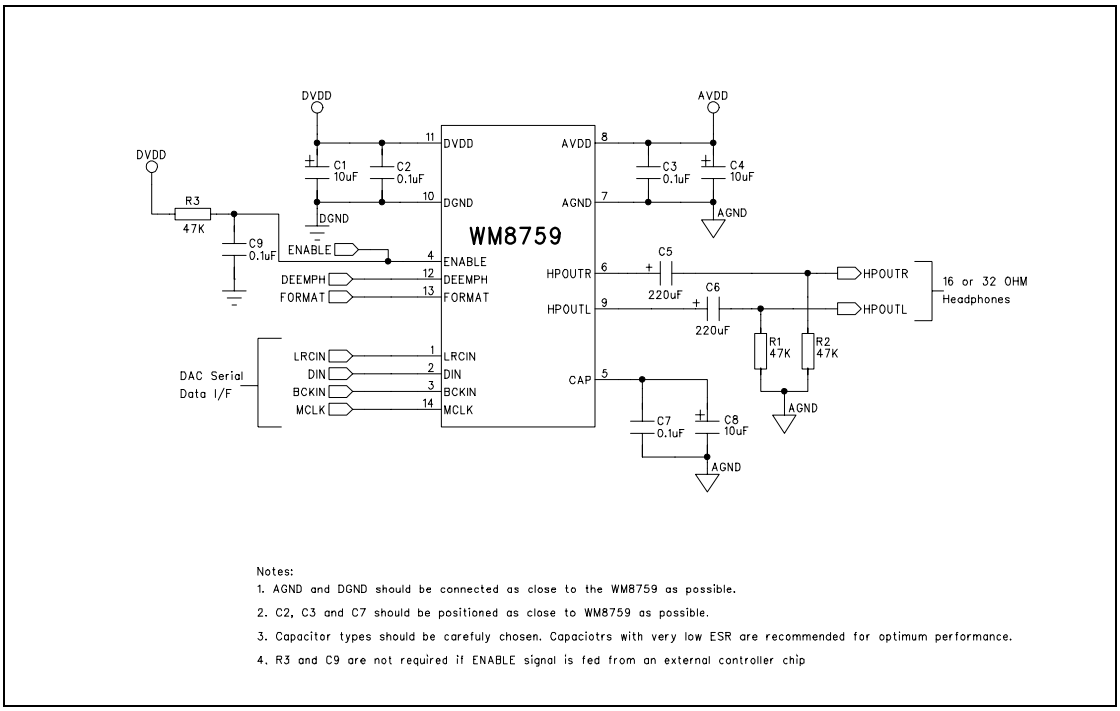


Figure 19 External Component Diagram

In an application where ENABLE is fed directly from VDD rather than a dedicated control line, resistor R3 and capacitor C9 are used on the ENABLE pin to introduce a short delay in the Low to High transition of ENABLE. This will ensure the pin goes high after power supplies have had time to settle (see “ENABLE Operation” in the “Hardware Control Modes” section of the datasheet).

However, if the ENABLE signal is being provided from an external controller chip rather than VDD directly, R3 and C9 will not be required.

POWER UP/DOWN SEQUENCE

POWER UP/DOWN SEQUENCE

For click free operation, the WM8759 should be powered up and down in a specific sequence.

Power-up:

1. Power up AVDD and DVDD and wait to settle
2. Turn on clocks and data (MCLK, BCLK, LRCLK, SDATA)
3. Switch ENABLE pin from low to high

Power-down:

1. Switch Enable from high to low
2. Remove clocks and data
3. Power down AVDD and DVDD

PCB LAYOUT RECOMMENDATIONS

Care should be taken in the layout of the PCB that the WM8759 is to be mounted to. The following notes will help in this respect:

1. **The VDD supply to the device should be as noise free as possible.** This can be accomplished to a large degree with a 10uF bulk capacitor placed locally to the device and a 0.1uF high frequency decoupling capacitor placed as close to the VDD pin as possible. It is best to place the 0.1uF capacitor directly between the VDD and GND pins of the device on the same layer to minimize track inductance and thus improve device decoupling effectiveness.

2. **The CAP pin should be as noise free as possible.** This pin provides the decoupling for the on chip reference circuits and thus any noise present on this pin will be directly coupled to the device outputs. In a similar manner to the VDD decoupling described above, this pin should be decoupled with a 10uF bulk capacitor local to the device and a 0.1uF capacitor as close to the CAP pin as possible.

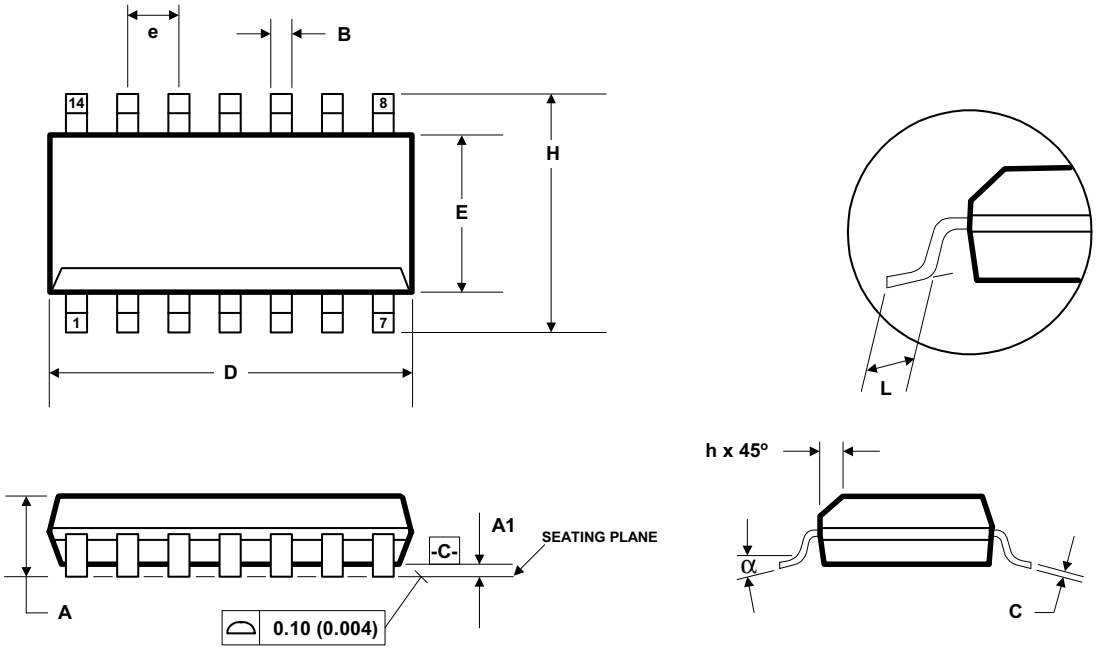
3. **Separate analogue and digital track routing from each other**. The device is split into analogue (pins 5 – 9) and digital (pins 1 – 4 and pins 10 – 14) sections that allow the routing of these signals to be easily separated. By physically separating analogue and digital signals, crosstalk from the PCB can be minimized.

4. **Use an unbroken solid GND plane**. To achieve best performance from the device, it is advisable to have either a GND plane layer on a multilayer PCB or to dedicate one side of a 2 layer PCB to be a GND plane. For double sided implementations it is best to route as many signals as possible on the device mounted side of the board, with the opposite side acting as a GND plane. The use of a GND plane greatly reduces any electrical emissions from the PCB and minimizes crosstalk between signals.

An evaluation board is available for the WM8759 that demonstrates the above techniques and the excellent performance achievable from the device. This can be ordered or the User manual downloaded from the Wolfson web site at www.wolfsonmicro.com

PACKAGE DRAWING

D: 14 PIN SOIC 3.9mm Wide Body **DM001.C**



Symbols	Dimensions (MM)		Dimensions (Inches)	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.0130	0.0200
C	0.19	0.25	0.0075	0.0098
D	8.55	8.75	0.3367	0.3444
E	3.80	4.00	0.1497	0.1574
e	1.27 BSC		0.05 BSC	
H	5.80	6.20	0.2284	0.2440
h	0.25	0.50	0.0099	0.0196
L	0.40	1.27	0.0160	0.0500
α	0^o	8^o	0^o	8^o
REF:	JEDEC.95, MS-012			

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).
D. MEETS JEDEC.95 MS-012, VARIATION = AB. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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