Data Sheet | March 4, 2005 | FN8187.0

# Dual Digitally Controlled Potentiometers (XDCPs™)

## FEATURES

- **Dual solid-state potentiometers**
- **Independent Up/Down interfaces**
- **32 wiper tap points per potentiometer**
  - **—Wiper position stored in nonvolatile memory and recalled on power-up**
- **31 resistive elements per potentiometer**
  - **—Temperature compensated**
  - **—Maximum resistance tolerance ± 25%**
  - **—Terminal voltage, 0 to $V_{CC}$**
- **Low power CMOS**
  - **—$V_{CC}$ = 5V ± 10%**
  - **—Active current, 200µA typ.**
  - **—Standby current, 4µA max**
- **High reliability**
  - **—Endurance 200,000 data changes per bit**
  - **—Register data retention, 100 years**
- **$R_{TOTAL}$ value = 50kΩ**
- **Packages**
  - **—14-lead TSSOP**

## DESCRIPTION

The Intersil X93255 is a dual digitally controlled potentiometer (XDCP). The device consists of two resistor arrays, wiper switches, a control section, and nonvolatile memory. The wiper positions are controlled by individual Up/Down interfaces.

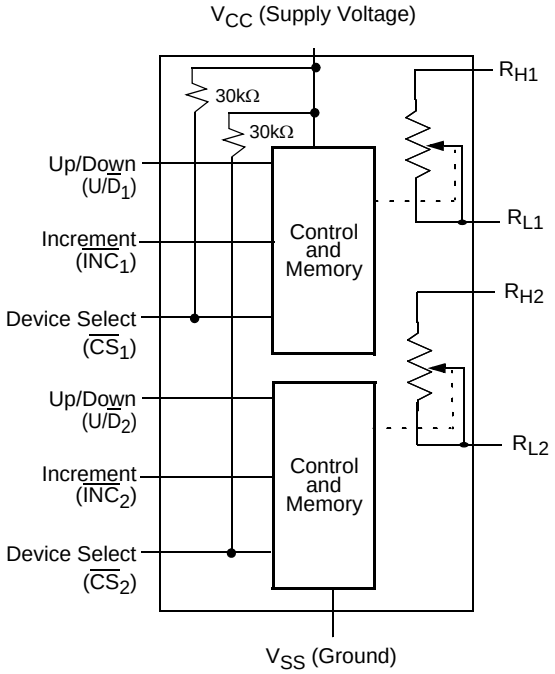
A potentiometer is implemented by a resistor array composed of 31 resistive elements and a wiper switching network. The position of each wiper element is controlled by a set of independent $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon a subsequent power-up operation.

Each potentiometer is connected as a two-terminal variable resistor and can be used in a wide variety of applications including:

– bias and gain control

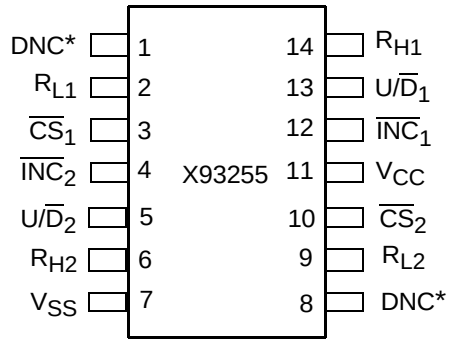
– LCD Contrast Adjustment

## BLOCK DIAGRAM



## PIN CONFIGURATION

**TSSOP**




*Do not connect.

## X93255 ORDERING CODES

| Ordering Number | RTOTAL | Package | Temperature Range |
|---|---|---|---|
| X93255UV14I | 50kΩ | 14-lead TSSOP package | -40°C to +85°C |

## PIN DESCRIPTIONS

| TSSOP | Symbol | Description |
|---|---|---|
| 1 | DNC | Do Not Connect. |
| 2 | $R_{L1}$ | Low Terminal 1. |
| 3 | $\overline{CS}_1$ | Chip Select 1. |
| 4 | $\overline{INC}_2$ | Increment 2. |
| 5 | $U/\overline{D}_2$ | Up/Down 2. |
| 6 | $R_{H2}$ | High Terminal 2. |
| 7 | $V_{SS}$ | Ground. |
| 8 | DNC | Do Not Connect. |
| 9 | $R_{L2}$ | Low Terminal 2. |
| 10 | $\overline{CS}_2$ | Chip Select 2. |
| 11 | $V_{CC}$ | Supply Voltage. |
| 12 | $\overline{INC}_1$ | Increment 1. |
| 13 | $U/\overline{D}_1$ | Up/Down 1. |
| 14 | $R_{H1}$ | High Terminal 1. |

## ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -65°C to +135°C
Storage temperature ..... -65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, $R_H$, $R_L$ and $V_{CC}$
with respect to $V_{SS}$ ..... -1V to +6.5V
Lead temperature (soldering 10 seconds)..... 300°C
Maximum reflow temperature (40 seconds) ..... 240°C
Maximum resistor current..... 2mA

## COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Temperature | Min. | Max. |
|---|---|---|
| Industrial | -40°C | +85°C |

| Supply Voltage ($V_{CC}$) | Limits |
|---|---|
| X93255 | 5V ± 10%(7) |

**POTENTIOMETER CHARACTERISTICS** (Over recommended operating conditions unless otherwise stated.)

| Symbol | Parameter | Limits | | | | Test Conditions/Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Unit | |
| $R_{TOT}$ | End to end resistance | 37.5 | 50 | 62.5 | kΩ | (5) |
| $V_R$ | $R_H$, $R_L$ terminal voltages | 0 | | $V_{CC}$ | V | (5) |
| | Power rating | | | 1 | mW(7) | $R_{TOTAL}$ = 50kΩ (5) (6) |
| | Noise | | -120 | | dBV(7) | Ref: 1kHz(5) (6) |
| $R_W$ | Wiper Resistance | | | 1000 | Ω | (5) (6) |
| $I_W$ | Wiper Current | | | 0.6 | mA | (5) (6) |
| | Resolution | | 3 | | % | (5) |
| | Absolute linearity(1) | | | ±1 | Ml(3) | $R_{H(n)(actual)} - R_{H(n)(expected)}$(5) |
| | Relative linearity(2) | | | ±0.5 | Ml(3) | $R_{H(n+1} - [R_{H(n)+Ml}]$ (5) |
| | $R_{TOTAL}$ temperature coefficient | | ±35 | | ppm/°C | (5) (6) |
| $C_H/C_L/C_W$ | Potentiometer capacitances | | 10/10/25 | | pF | See circuit #2(5) |

Notes: (1) Absolute linearity is utilized to determine actual wiper resistance versus expected resistance = ($R_{H(n)}$(actual) - $R_{H(n)}$(expected)) = ±1 Ml Maximum. n = 1 .. 29 only
(2) Relative linearity is a measure of the error in step size between taps = $R_{H(n+1)}$ - [$R_{H(n)}$ + Ml] = ±0.5 Ml, n = 1 .. 29 only.
(3) 1 Ml = Minimum Increment = $R_{TOT}$/31.
(4) Typical values are for $T_A$ = 25°C and nominal supply voltage.
(5) This parameter is only applies to a single potentiometer
(6) This parameter is guaranteed by characterization.
(7) When performing multiple write operations, $V_{CC}$ must not decrease by more than 150mV from its initial value.

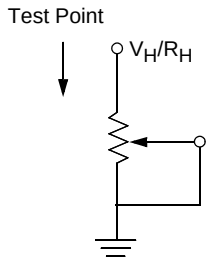
**D.C. OPERATING CHARACTERISTICS** (Over recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ.(4) | Max. | | |
| $I_{CC1}$ | $V_{CC}$ active current (Increment) per DCP | | 200 | 300 | µA | $\overline{CS}$ = $V_{IL}$, U/$\overline{D}$ = $V_{IL}$ or $V_{IH}$ and $\overline{INC}$ = 0.4V @ max. $t_{CYC}$(5) |
| $I_{CC2}$ | $V_{CC}$ active current (Store) (EEPROM Store) per DCP | | | 1400 | µA | $\overline{CS}$ = $V_{IH}$, U/$\overline{D}$ = $V_{IL}$ or $V_{IH}$ and $\overline{INC}$ = $V_{IH}$ @ max. $t_{WR}$(5) |
| $I_{SB}$ | Standby supply current | | | 4 | µA | $\overline{CS}$ = $V_{CC}$ - 0.3V, U/$\overline{D}$ and $\overline{INC}$ = $V_{SS}$ or $V_{CC}$ - 0.3V |
| $I_{LI}$ | CS | | | ±1 | µA | $V_{\overline{CS}}$ = $V_{CC}$(5) |
| $I_{LI}$ | CS | 120 | 200 | 250 | µA | $V_{CC}$ = 5V, $\overline{CS}$ = 0(5) |
| $I_{LI}$ | $\overline{INC}$, U/$\overline{D}$ input leakage current | | | ±1 | µA | $V_{IN}$ = $V_{SS}$ to $V_{CC}$(5) |
| $V_{IH}$ | $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input HIGH voltage | $V_{CC}$ x 0.7 | | $V_{CC}$ + 0.5 | V | (5) |
| $V_{IL}$ | $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input LOW voltage | -0.5 | | $V_{CC}$ x 0.1 | V | (5) |
| $C_{IN}$(5)(7) | $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ input capacitance | | | 10 | pF | $V_{CC}$ = 5V, $V_{IN}$ = $V_{SS}$, $T_A$ = 25°C, f = 1MHz(6) |

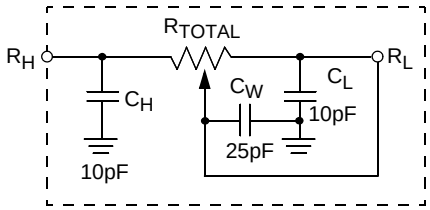
**ENDURANCE AND DATA RETENTION**

| Parameter | Min. | Unit |
|---|---|---|
| Minimum endurance | 200,000 | Data changes per bit |
| Data retention | 100 | Years |

**Test Circuit #1**




**Circuit #2 SPICE Macro Model**




**A.C. CONDITIONS OF TEST**

| | |
|---|---|
| Input pulse levels | 0V to 5V |
| Input rise and fall times | 10ns |
| Input reference levels | 1.5V |

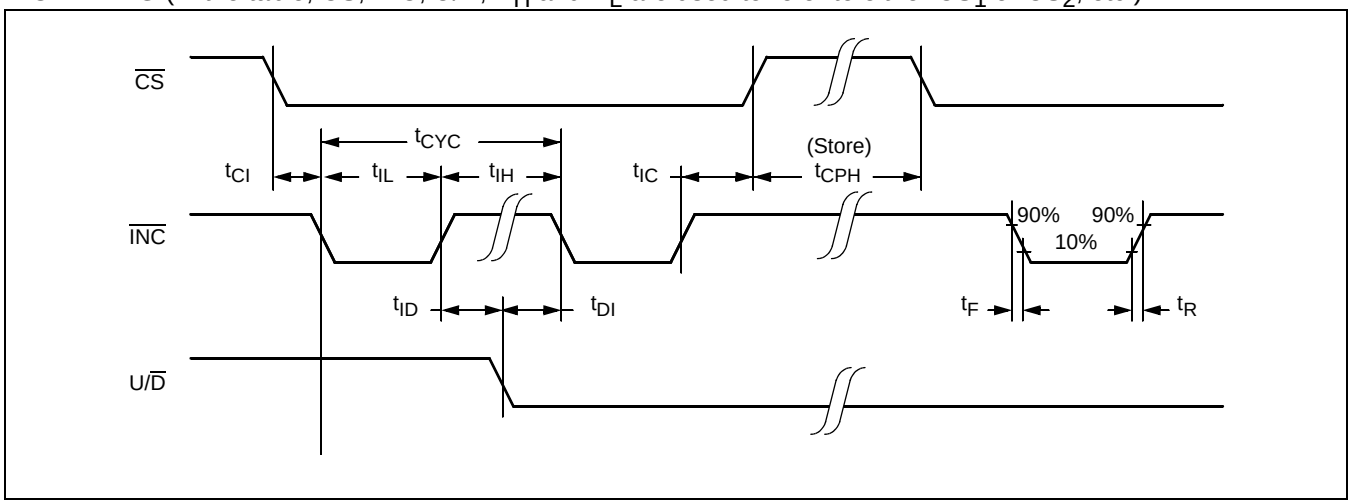
**A.C. OPERATING CHARACTERISTICS** (Over recommended operating conditions unless otherwise specified. In the table, $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, $R_H$ and $R_L$ are used to refer to either $\overline{CS}_1$ or $\overline{CS}_2$, etc.)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ.(6) | Max. | |
| $t_{CI}$ | $\overline{CS}$ to $\overline{INC}$ setup | 100 | | | ns |
| $t_{ID}$ | $\overline{INC}$ HIGH to U/$\overline{D}$ change | 100 | | | ns |
| $t_{DI}$ | U/$\overline{D}$ to $\overline{INC}$ setup | 100 | | | ns |
| $t_{IL}$ | $\overline{INC}$ LOW period | 1 | | | µs |
| $t_{IH}$ | $\overline{INC}$ HIGH period | 1 | | | µs |
| $t_{IC}$ | $\overline{INC}$ Inactive to $\overline{CS}$ inactive | 1 | | | µs |
| $t_{CPH}$ | $\overline{CS}$ Deselect time (NO STORE) | 250 | | | ns |
| $t_{CPH}$ | $\overline{CS}$ Deselect time (STORE) | 10 | | | ms |
| $t_{CYC}$ | $\overline{INC}$ cycle time | 2 | | | µs |
| $t_R$, $t_F$(6) | $\overline{INC}$ input rise and fall time | | | 500 | µs |
| $t_R$ $V_{CC}$(6) | $V_{CC}$ power-up rate | 1 | | 10,000 | V/ms |
| $t_{WR}$ | Store cycle | | 5 | 10 | ms |

**POWER-UP AND DOWN REQUIREMENTS**

There are no restrictions on the power-up or power-down conditions of $V_{CC}$ and the voltages applied to the potentiometer pins provided that $V_{CC}$ is always more positive than or equal to $V_H$ and $V_L$, i.e., $V_{CC} \geq V_H, V_L$. The $V_{CC}$ ramp rate spec is always in effect.

**A.C. TIMING** (In the table, $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, $R_H$ and $R_L$ are used to refer to either $\overline{CS}_1$ or $\overline{CS}_2$, etc.)



## PIN DESCRIPTIONS

### $R_H$ and $R_L$

The $R_H$ and $R_L$ pins of the X93255 are equivalent to the end terminals of a variable resistor. The minimum voltage is $V_{SS}$ and the maximum is $V_{CC}$. The terminology of $R_H$ and $R_L$ references the relative position of the terminal in relation to wiper movement direction selected by the U/$\overline{D}$ input per potentiometer.

### Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of a single potentiometer's wiper movement and whether the counter is incremented or decremented.

### Increment ($\overline{INC}$)

The $\overline{INC}$ input is negative-edge triggered. Toggling $\overline{INC}$ will move the wiper and either increment or decrement the pertatining potentiometer's counter in the direction indicated by the logic level on the pertaining potentiometer's U/$\overline{D}$ input.

### Chip Select ($\overline{CS}$)

A potentiometer is selected when the pertaining $\overline{CS}$ input is LOW. Its current counter value is stored in nonvolatile memory when the pertaining $\overline{CS}$ is returned HIGH while the pertaining $\overline{INC}$ input is also HIGH. After the store operation is complete the affected potentiometer will be placed in the low power standby mode until the potentiometer is selected once again.

## PRINCIPLES OF OPERATION

There are multiple sections for each potentiometer in the X93255: an input control, a counter and decode section; the nonvolatile memory; and a resistor array. Each input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. Each resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the connection at that point to the wiper. The wiper is connected to the $R_L$ terminal, forming a variable resistor from $R_H$ to $R_L$.

Each wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

If the wiper is moved several positions, multiple taps are connected to the wiper for up to 10µs. The 2-terminal resistance value for the device can temporarily change by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory for each potentiometer. When power is restored, the contents of the memory are recalled and each wiper is set to the value last stored.

## INSTRUCTIONS AND PROGRAMMING

The $\overline{INC}$, U/$\overline{D}$ and $\overline{CS}$ inputs control the movement of the pertaining wiper along the resistor array. With $\overline{CS}$ set LOW the pertaining potentiometer is selected and enabled to respond to the U/$\overline{D}$ and $\overline{INC}$ inputs. HIGH to LOW transitions on $\overline{INC}$ will increment or decrement (depending on the state of the U/$\overline{D}$ input) a five bit counter. The output of this counter is decoded to select one of thirty two wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever each $\overline{CS}$ transitions HIGH while the pertaining $\overline{INC}$ input is also HIGH. In order to avoid an accidental store during power-up, each $\overline{CS}$ must go HIGH with $V_{CC}$ during initial power-up. When left open, each $\overline{CS}$ pin is internally pulled up to $V_{CC}$ by an internal 30K resistor.

The system may select the X93255, move any wiper and deselect the device without having to store the latest wiper position in nonvolatile memory. After the wiper movement is performed as described above and once the new position is reached, the system must keep $\overline{INC}$ LOW while taking $\overline{CS}$ HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalled the previously stored data. In order to recall the stored position of the wiper on power-up, the $\overline{CS}$ pin must be held HIGH.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, or other system trim requirements.

The state of U/$\overline{D}$ may be changed while $\overline{CS}$ remains LOW. This allows the host system to enable the device and then move each wiper up and down until the proper trim is attained.

## MODE SELECTION

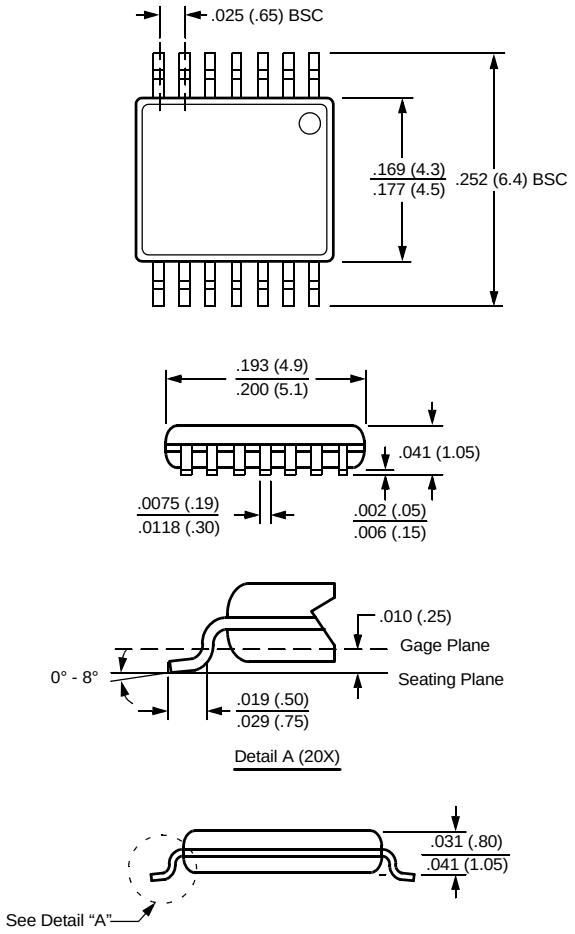
| $\overline{CS}$ | $\overline{INC}$ | U/$\overline{D}$ | Mode |
|---|---|---|---|
| L | ↘ | H | Wiper Up |
| L | ↘ | L | Wiper Down |
| ↗ | H | X | Store Wiper Position |
| H | X | X | Standby Current |
| ↗ | L | X | No Store, Return to Standby |
| ↘ | L | H | Wiper Up (not recommended) |
| ↘ | L | L | Wiper Down (not recommended) |

## SYMBOL TABLE

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| ——— | Must be steady | Will be steady |
| ⟋ | May change from Low to High | Will change from Low to High |
| ⟍ | May change from High to Low | Will change from High to Low |
| ⨯ | Don't Care: Changes Allowed | Changing: State Not Known |
| ⋈ | N/A | Center Line is High Impedance |

## TSSOP PACKAGING INFORMATION

**14-Lead Plastic, TSSOP, Package Code V14**




**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**