# XC6109 Series

***Voltage Detector with External Delay Type Capacitor***

◆CMOS
◆Highly Accurate : ±2%
◆Low Power Consumption : 0.9μA (TYP.) ($V_{DF}$=1.9V, $V_{IN}$ = 2.0V)
◆Built-In Delay Circuit, Delay Pin Available

## ■GENERAL DESCRIPTION

The XC6109 series is highly precise, low power consumption voltage detector, manufactured using CMOS and laser trimming technologies.
With the built-in delay circuit, connecting the delay capacitance pin to the capacitor enables the IC to provide an arbitrary release delay time.
Using an ultra small package (SSOT-24), the series is suited for high density mounting.
Both CMOS and N-channel open drain output configurations are available.

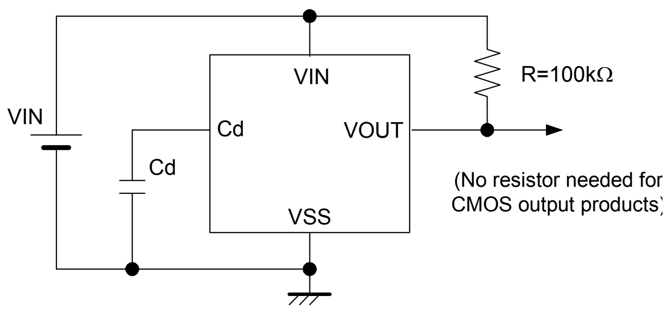
## ■APPLICATIONS

●Microprocessor reset circuitry
●Charge voltage monitors
●Memory battery back-up switch circuits
●Power failure detection circuits

## ■FEATURES

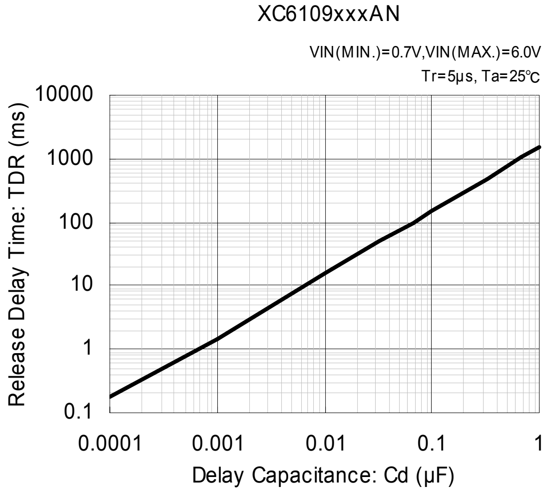
**Highly Accurate** : ±2% (Setting Voltage Accuracy≧1.5V)
: ±30mV (Setting Voltage Accuracy<1.5V)
**Low Power Consumption** : 0.9 μA (TYP., $V_{DF}$=1.9V, $V_{IN}$= 2.0V)
**Detect Voltage Range** : 0.8V ~ 5.0V in 100mV increments
**Operating Voltage Range** : 0.7V ~ 6.0V
**Detect Voltage Temperature Characteristics** : ±100ppm/°C (TYP.)
**Output Configuration** : CMOS or N-channel open drain
**Operating Temperature Range** : -40 °C ~ +85 °C
**Ultra Small Package** : SSOT-24

## ■TYPICAL APPLICATION CIRCUIT

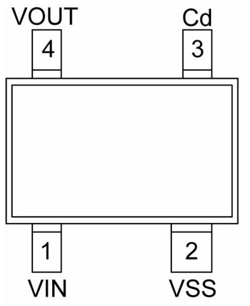



## ■TYPICAL PERFORMANCE CHARACTERISTICS

●Release Delay Time vs. Delay Capacitance



## ■PIN CONFIGURATION




SSOT-24 (TOP VIEW)

## ■PIN ASSIGNMENT

| PIN NUMBER | PIN NAME | FUNCTION |
|---|---|---|
| 1 | $V_{IN}$ | Input |
| 2 | $V_{SS}$ | Ground |
| 3 | Cd | Delay Capacitance |
| 4 | $V_{OUT}$ | Output (Detect "L") |

## ■PRODUCT CLASSIFICATION

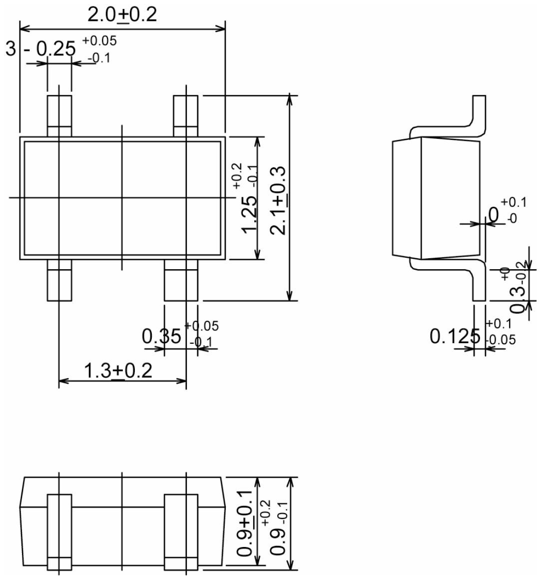
●Ordering Information

XC6109 ①②③④⑤⑥

| DESIGNATOR | DESCRIPTION | SYMBOL | DESCRIPTION |
|---|---|---|---|
| ① | Output Configuration | C | : CMOS output |
| | | N | : N-ch open drain output |
| ② ③ | Detect Voltage | 08 ~ 50 | : e.g. 18→1.8V |
| ④ | Output Delay & Hysteresis | A | : Built-in delay pin & hysteresis 5% (TYP.) |
| ⑤ | Package | N | : SSOT-24 |
| ⑥ | Device Orientation | R | : Embossed tape, standard feed |
| | | L | : Embossed tape, reverse feed |

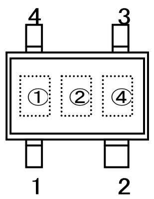
# ■PACKAGING INFORMATION

●SSOT-24




# ■MARKING RULE

●SSOT-24




SSOT-24
(TOP VIEW)

① Represents output configuration and integer number of detect voltage

CMOS output (XC6109C Series) N-ch Open Drain output (XC6109N Series)

| MARK | VOLTAGE (V) | PRODUCT SERIES | MARK | VOLTAGE (V) | PRODUCT SERIES |
|---|---|---|---|---|---|
| A | 0.x | XC6109C0xxNx | K | 0.x | XC6109N0xxNx |
| B | 1.x | XC6109C1xxNx | L | 1.x | XC6109N1xxNx |
| C | 2.x | XC6109C2xxNx | M | 2.x | XC6109N2xxNx |
| D | 3.x | XC6109C3xxNx | N | 3.x | XC6109N3xxNx |
| E | 4.x | XC6109C4xxNx | P | 4.x | XC6109N4xxNx |
| F | 5.x | XC6109C5xxNx | R | 5.x | XC6109N5xxNx |

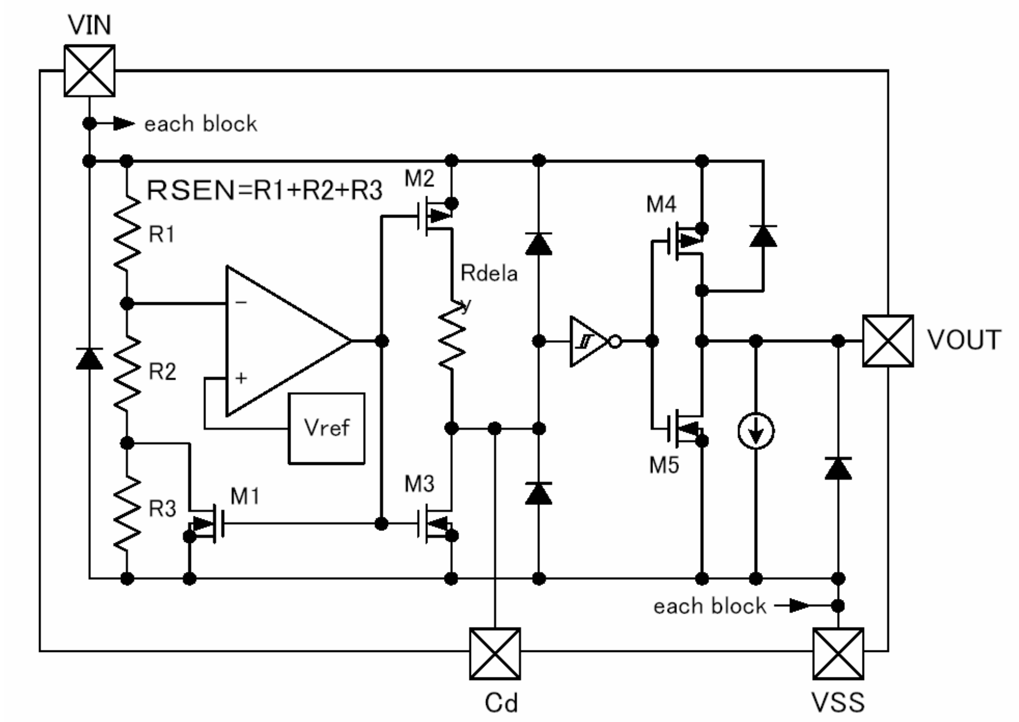
②Represents decimal number of detect voltage

| MARK | VOLTAGE (V) | PRODUCT SERIES |
|---|---|---|
| N | x.0 | XC6109xx0xNx |
| P | x.1 | XC6109xx1xNx |
| R | x.2 | XC6109xx2xNx |
| S | x.3 | XC6109xx3xNx |
| T | x.4 | XC6109xx4xNx |
| U | x.5 | XC6109xx5xNx |
| V | x.6 | XC6109xx6xNx |
| X | x.7 | XC6109xx7xNx |
| Y | x.8 | XC6109xx8xNx |
| Z | x.9 | XC6109xx9xNx |

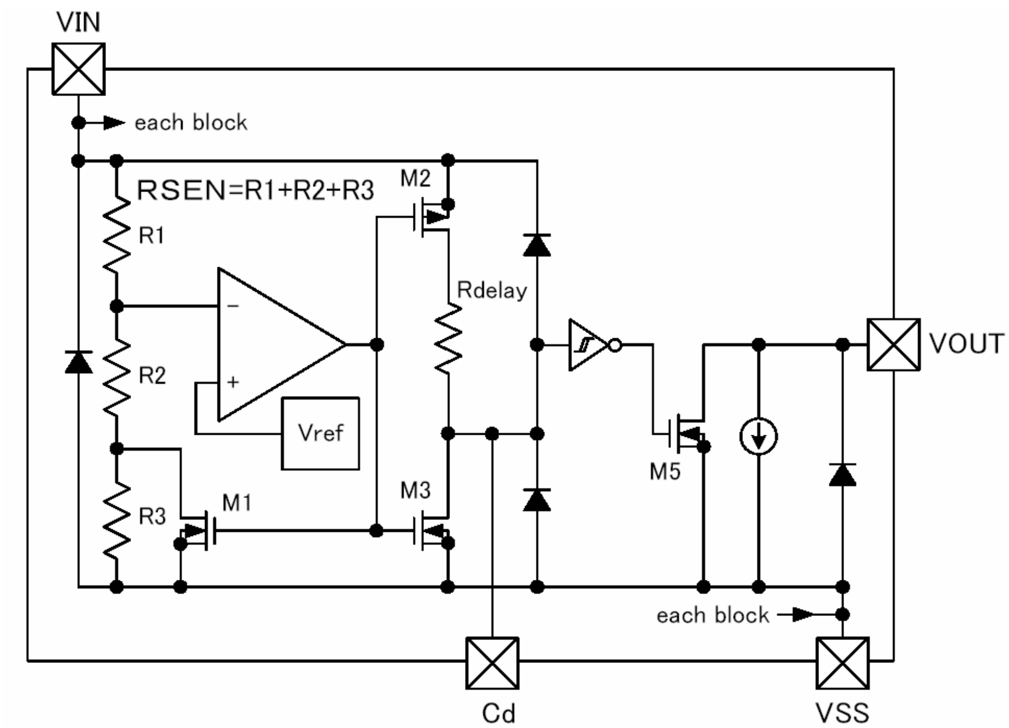
④Represents production lot number
0 to 9, A to Z or inverted characters of 0 to 9, A to Z repeated/
(G, I, J, O, Q, W excepted)

## ■BLOCK DIAGRAMS

(1) XC6109C (CMOS Output)




(2) XC6109N (N-ch Open Drain Output)



## ■ABSOLUTE MAXIMUM RATINGS

Ta = 25°C

| PARAMETER | | SYMBOL | RATINGS | UNITS |
|---|---|---|---|---|
| Input Voltage | | $V_{IN}$ | $V_{SS}$ - 0.3 ~ 7.0 | V |
| Output Current | | $I_{OUT}$ | 10 | mA |
| Output Voltage | XC6109C (*1) | $V_{OUT}$ | $V_{SS}$ - 0.3 ~ $V_{IN}$ + 0.3 | V |
| | XC6109N (*2) | | $V_{SS}$ - 0.3 ~ 7.0 | |
| Delay Pin Voltage | | $V_{CD}$ | $V_{SS}$-0.3 ~ $V_{IN}$ + 0.3 | V |
| Delay Pin Current | | $I_{CD}$ | 5.0 | mA |
| Power Dissipation | SSOT-24 | Pd | 150 | mW |
| Operating Temperature Range | | Ta | - 40 ~ + 85 | °C |
| Storage Temperature Range | | Tstg | - 40 ~ + 125 | °C |

NOTE:
*1: CMOS output
*2: N-ch open drain output

## ■ELECTRICAL CHARACTERISTICS

Ta = 25°C

| PARAMETER | SYMBOL | CONDITIONS | | MIN. | TYP. | MAX. | UNIT | CIRCUIT |
|---|---|---|---|---|---|---|---|---|
| Operating Voltage | $V_{IN}$ | $V_{DF(T)}$=0.8~5.0V (*1) | | 0.7 | - | 6.0 | V | - |
| Detect Voltage | $V_{DF}$ | $V_{DF(T)}$=0.8~5.0V | | E-1 | | | V | 1 |
| Hysteresis Range 1 | $V_{HYS1}$ | $V_{IN}$=1.0~6.0V | | $V_{DF}$ x 0.02 | $V_{DF}$ x 0.05 | $V_{DF}$ x 0.08 | V | 1 |
| Supply Current 1 | $I_{SS1}$ | $V_{IN}$=$V_{DF}$ x 0.9 | $V_{DF(T)}$=0.8~1.9V | - | 0.80 | 1.70 | μA | 2 |
| | | | $V_{DF(T)}$=2.0~3.9V | - | 0.90 | 1.90 | | |
| | | | $V_{DF(T)}$=4.0~5.0V | - | 1.00 | 2.00 | | |
| Supply Current 2 | $I_{SS2}$ | $V_{IN}$=$V_{DF}$ x 1.1 | $V_{DF(T)}$=0.8~1.9V | - | 0.90 | 1.80 | μA | 2 |
| | | | $V_{DF(T)}$=2.0~3.9V | - | 1.10 | 2.00 | | |
| | | | $V_{DF(T)}$=4.0~5.0V | - | 1.20 | 2.20 | | |
| Output Current | $I_{OUT1}$ | $V_{IN}$=$V_{DF}$x0.9<br>$V_{DS}$=0.5V (N-ch) | | E-2 | | | mA | 3 |
| | $I_{OUT2}$ (*2) | $V_{IN}$=$V_{DF}$x1.1<br>$V_{DS}$=0.5V (P-ch) | | E-3 | | | mA | 3 |
| Temperature Characteristics | $\frac{\triangle V_{DF}}{\triangle Ta \cdot V_{DF}}$ | -40°C≦Ta≦85°C | | - | ±100 | - | ppm/°C | 1 |
| Delay Resistance (*3) | Rdelay | $V_{IN}$=6.0V, $V_{CD}$=0V | | 1.6 | 2.0 | 2.4 | MΩ | 4 |
| Delay Pin Sink Current | $I_{CD}$ | $V_{DS}$=0.5V, $V_{IN}$=0.7V | | 8 | 60 | - | μA | 4 |
| Delay Capacitance Pin Threshold Voltage | $V_{TCD}$ | $V_{IN}$=1.0V | | 0.4 | 0.5 | 0.6 | V | 5 |
| | | $V_{IN}$=6.0V | | 2.9 | 3.0 | 3.1 | | |
| Unspecified Operating Voltage (*4) | $V_{UNS}$ | $V_{IN}$=0~0.7V | | - | 0.3 | 0.4 | V | 6 |
| Detect Delay Time (*5) | $T_{DF0}$ | $V_{IN}$=6.0 down to 0.7V<br>Cd: Open | | - | 30 | 230 | μs | 7 |
| Release Delay Time (*6) | $T_{DR0}$ | $V_{IN}$=0.7~6.0V<br>Cd: Open | | - | 30 | 200 | μs | 7 |

NOTE:
*1: $V_{DF(T)}$: Setting Detect Voltage
*2: This numerical value is applied only to the XC6109C series (CMOS output).
*3: Calculated from the voltage value and the current value of both ends of the resistor.
*4: The maximum voltage of the $V_{OUT}$ in the range of the $V_{IN}$ 0 to 0.7V. This numerical value is applied only to the XC6109C series (CMOS output).
*5: Time which ranges from the state of $V_{IN}$ =$V_{DF}$ to the $V_{OUT}$ reaching 0.6V when the $V_{IN}$ falls without connecting to the Cd pin.
*6: Time which ranges from the state of $V_{IN}$= $V_{DF}$ +$V_{HYS}$ to the $V_{OUT}$ reaching 5.4V when the $V_{IN}$ rises without connecting to the Cd pin.

## ■VOLTAGE CHART

| SYMBOL | E-1 | | | E-2 | | | E-3 | | |
|---|---|---|---|---|---|---|---|---|---|
| SETTING OUTPUT VOLTAGE (V) | DETECT VOLTAGE (*1) (V) | | | OUTPUT CURRENT (mA) | | | OUTPUT CURRENT (*2) (mA) | | |
| $V_{DF(T)}$ | $V_{DF}$ | | | $I_{OUT1}$ | | | $I_{OUT2}$ | | |
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| 0.8 | 0.770 | 0.800 | 0.830 | 0.01 | 0.36 | 0.70 | -0.40 | -0.20 | -0.01 |
| 0.9 | 0.870 | 0.900 | 0.930 | | | | | | |
| 1.0 | 0.970 | 1.000 | 1.030 | | | | | | |
| 1.1 | 1.070 | 1.100 | 1.130 | 0.10 | 0.70 | 1.30 | -0.60 | -0.30 | -0.08 |
| 1.2 | 1.170 | 1.200 | 1.230 | | | | | | |
| 1.3 | 1.270 | 1.300 | 1.330 | | | | | | |
| 1.4 | 1.370 | 1.400 | 1.430 | | | | | | |
| 1.5 | 1.470 | 1.500 | 1.530 | 0.30 | 1.00 | 1.80 | -0.80 | -0.40 | -0.14 |
| 1.6 | 1.568 | 1.600 | 1.632 | | | | | | |
| 1.7 | 1.666 | 1.700 | 1.734 | | | | | | |
| 1.8 | 1.764 | 1.800 | 1.836 | | | | | | |
| 1.9 | 1.862 | 1.900 | 1.938 | | | | | | |
| 2.0 | 1.960 | 2.000 | 2.040 | 0.60 | 1.60 | 2.60 | -1.00 | -0.50 | -0.20 |
| 2.1 | 2.058 | 2.100 | 2.142 | | | | | | |
| 2.2 | 2.156 | 2.200 | 2.244 | | | | | | |
| 2.3 | 2.254 | 2.300 | 2.346 | | | | | | |
| 2.4 | 2.352 | 2.400 | 2.448 | | | | | | |
| 2.5 | 2.450 | 2.500 | 2.550 | | | | | | |
| 2.6 | 2.548 | 2.600 | 2.652 | | | | | | |
| 2.7 | 2.646 | 2.700 | 2.754 | | | | | | |
| 2.8 | 2.744 | 2.800 | 2.856 | | | | | | |
| 2.9 | 2.842 | 2.900 | 2.958 | | | | | | |
| 3.0 | 2.940 | 3.000 | 3.060 | 1.00 | 2.00 | 3.10 | -1.20 | -0.60 | -0.40 |
| 3.1 | 3.038 | 3.100 | 3.162 | | | | | | |
| 3.2 | 3.136 | 3.200 | 3.264 | | | | | | |
| 3.3 | 3.234 | 3.300 | 3.366 | | | | | | |
| 3.4 | 3.332 | 3.400 | 3.468 | | | | | | |
| 3.5 | 3.430 | 3.500 | 3.570 | | | | | | |
| 3.6 | 3.528 | 3.600 | 3.672 | | | | | | |
| 3.7 | 3.626 | 3.700 | 3.774 | | | | | | |
| 3.8 | 3.724 | 3.800 | 3.876 | | | | | | |
| 3.9 | 3.822 | 3.900 | 3.978 | | | | | | |
| 4.0 | 3.920 | 4.000 | 4.080 | 1.30 | 2.30 | 3.30 | -1.30 | -0.65 | -0.60 |
| 4.1 | 4.018 | 4.100 | 4.182 | | | | | | |
| 4.2 | 4.116 | 4.200 | 4.284 | | | | | | |
| 4.3 | 4.214 | 4.300 | 4.386 | | | | | | |
| 4.4 | 4.321 | 4.400 | 4.488 | | | | | | |
| 4.5 | 4.410 | 4.500 | 4.590 | | | | | | |
| 4.6 | 4.508 | 4.600 | 4.692 | | | | | | |
| 4.7 | 4.606 | 4.700 | 4.794 | | | | | | |
| 4.8 | 4.704 | 4.800 | 4.896 | | | | | | |
| 4.9 | 4.802 | 4.900 | 4.998 | | | | | | |
| 5.0 | 4.900 | 5.000 | 5.100 | | | | | | |

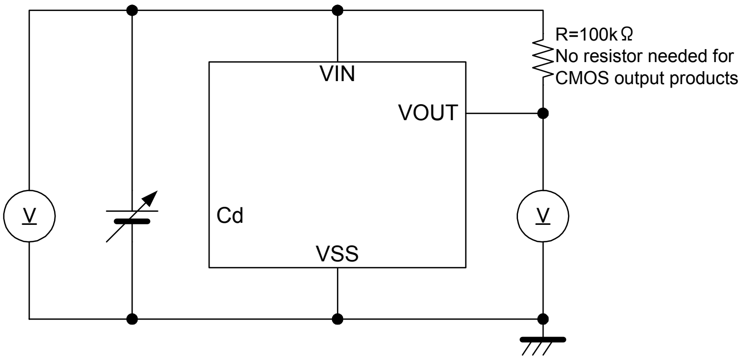
NOTE:

*1: When $V_{DF(T)} \leqq 1.4V$, the detection accuracy is ±30mV. When $V_{DF(T)} \geqq 1.5V$, the detection accuracy is ±2%.

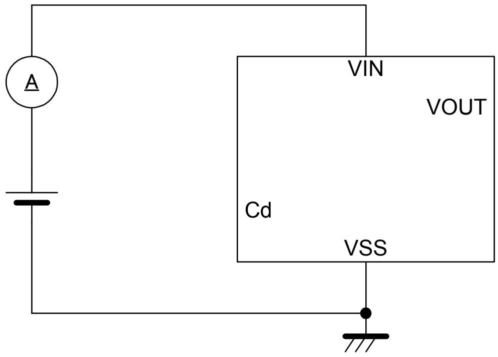
*2: This numerical value is applied only to the XC6109C series (CMOS output).

## ■TEST CIRCUITS

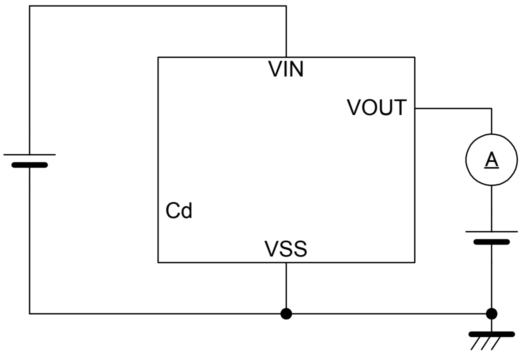
Circuit 1



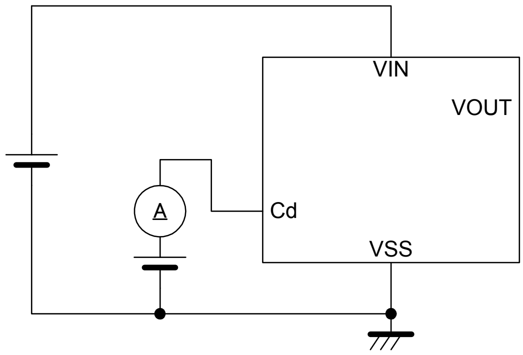

Circuit 2



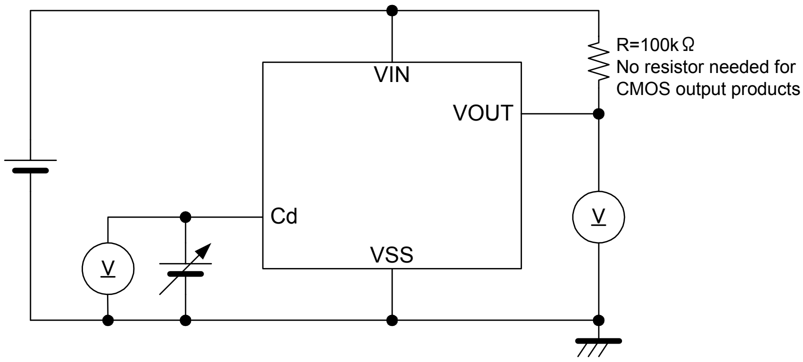

Circuit 3



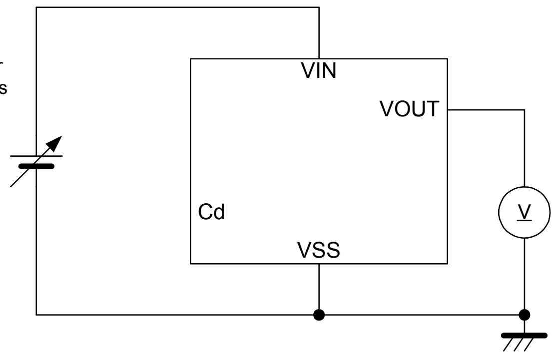

Circuit 4



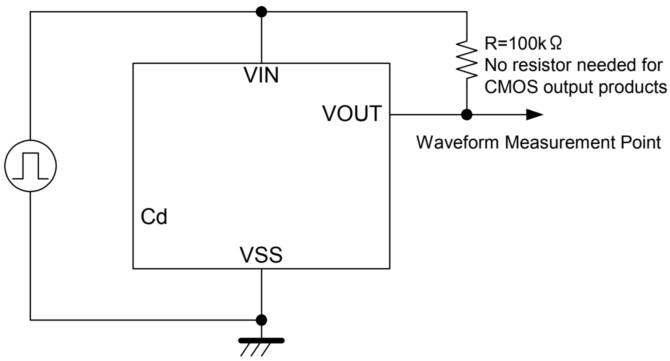

Circuit 5




Circuit 6




Circuit 7



## ■OPERATIONAL EXPLANATION

A typical circuit example is shown in Figure 1, and the timing chart of Figure 1 is shown in Figure 2 on the next page.

① As an early state, the input voltage pin is applied sufficiently high voltage to the release voltage and the delay capacitance (Cd) is charged to the input pin voltage. While the input pin voltage ($V_{IN}$) starts dropping to reach the detect voltage ($V_{DF}$) ($V_{IN} > V_{DF}$), the output voltage ($V_{OUT}$) keeps the “High” level (=$V_{IN}$).

② When the input pin voltage keeps dropping and becomes equal to the detect voltage ($V_{IN} = V_{DF}$), an N-ch transistor for the delay capacitance discharge is turned ON, and starts to discharge the delay capacitance. For the internal circuit, which uses the delay capacitance pin as power input, the reference voltage operates as a comparator of $V_{IN}$, and the output voltage changes into the “Low” level ($\leqq V_{IN} \times 0.1$). The detect delay time ($T_{DF}$) is defined as time which ranges from $V_{IN} = V_{DF}$ to the $V_{OUT}$ of “Low” level (especially, when the Cd pin is not connected: $T_{DF0}$).

③ While the input pin voltage keeps below the detect voltage, and 0.7V or more, the delay capacitance is discharged to the ground voltage (=$V_{SS}$) level. Then, the output voltage ($V_{OUT}$) maintains the “Low” level.

④ While the input pin voltage drops to 0.7V or less and it increases again to 0.7V or more, the output voltage may not be able to maintain the “Low” level. Such an operation is called “Unspecified Operation”, and voltage which occurs at the output pin voltage is defined as unstable operating voltage ($V_{UNS}$).

⑤ While the input pin voltage increases more than 0.7V and it reaches to the release voltage level ($V_{IN} < V_{DF} + V_{HYS}$), the output voltage ($V_{OUT}$) maintains the “Low” level.

⑥ When the input pin voltage continues to increase more than 0.7V up to the release voltage level (= $V_{DF} + V_{HYS}$), the N-ch transistor for the delay capacitance discharge will be turned OFF, and the delay capacitance will be started discharging via a delay resistor (Rdelay). The internal circuit, which uses the delay capacitance pin as power input, will operate as a hysteresis comparator (Rise Logic Threshold: $V_{TLH}=V_{TCD}$, Fall Logic Threshold: $V_{THL}=V_{SS}$) while the input pin voltage keeps higher than the detect voltage ($V_{IN} > V_{DF}$).

⑦ While the input pin voltage becomes equal to the release voltage or higher and keeps the detect voltage or higher, the delay capacitance (Cd) will be charged up to the input pin voltage. When the delay capacitance pin voltage ($V_{CD}$) reaches to the delay capacitance pin threshold voltage ($V_{TCD}$), the output voltage changes into the “High” (=$V_{IN}$) level. $T_{DR}$ is defined as time which ranges from $V_{IN} = V_{DF} + V_{HYS}$ to the $V_{OUT}$ of “High” level (especially when the Cd pin is not connected: $T_{DR0}$). $T_{DR}$ can be given by the formula (1).

$$T_{DR} = -Rdelay \times Cd \times \ln(1 - V_{TCD} / V_{IN}) + T_{DR0} \quad \cdots(1)$$

* ln = a natural logarithm

The release delay time can also be briefly calculated with the formula (2) because the delay resistance is 2.0MΩ (TYP.) and the delay capacitance pin threshold voltage is $V_{IN}/2$ (TYP.)

$$T_{DR} = 2.0e6 \times Cd \times 0.69 \cdots(2)$$

As an example, presuming that the delay capacitance is 0.68μF, TDR is :

$$2.0e6 \times 0.68e{-6} \times 0.69 = 938 \text{ (ms)}$$

* Note that the release delay time may remarkably be short when the delay capacitance is not discharged to the ground (=$V_{SS}$) level because time described in ③ is short.

⑧ While the input pin voltage is higher than the detect voltage ($V_{IN} > V_{DF}$), therefore, the output voltage maintains the “High”(=$V_{IN}$) level.

●Release Delay Time Chart

| Delay Capacitance [Cd] (μF) | Release Delay Time [$T_{DR}$] (TYP.) (ms) | Release Delay Time [$T_{DR}$] (MIN. ~ MAX.) (ms) |
|---|---|---|
| 0.01 | 13.8 | 11.0 ~ 16.6 |
| 0.022 | 30.4 | 24.3 ~ 36.4 |
| 0.047 | 64.9 | 51.9 ~ 77.8 |
| 0.1 | 138 | 110 ~ 166 |
| 0.22 | 304 | 243~ 364 |
| 0.47 | 649 | 519 ~ 778 |
| 1 | 1380 | 1100 ~ 1660 |

## ■OPERATIONAL EXPLANATION (Continued)

Figure 1: Typical application circuit example

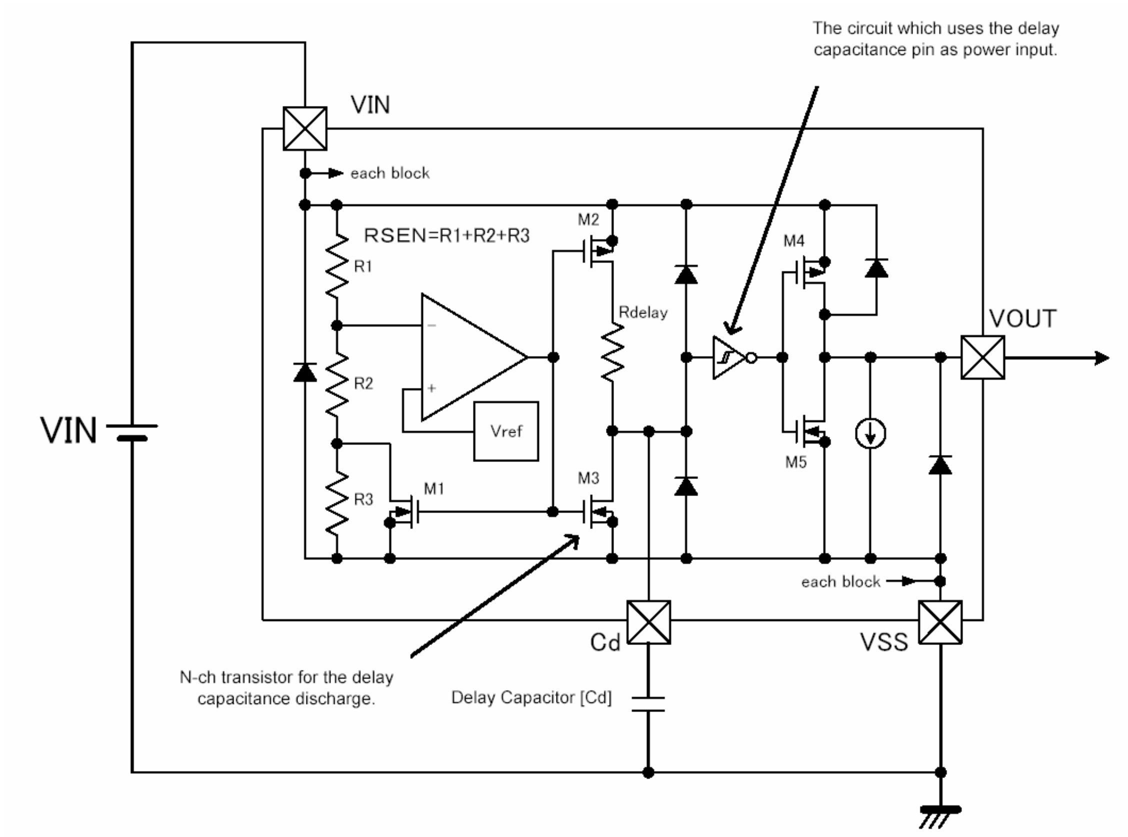
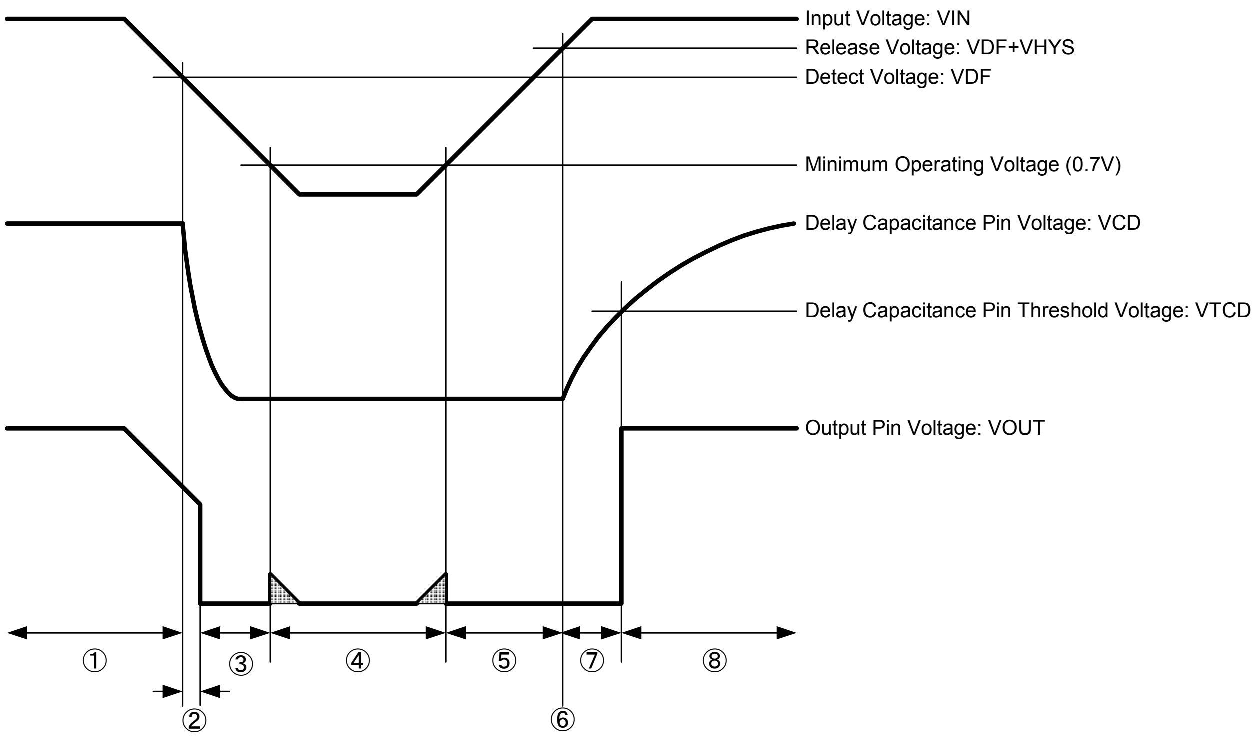


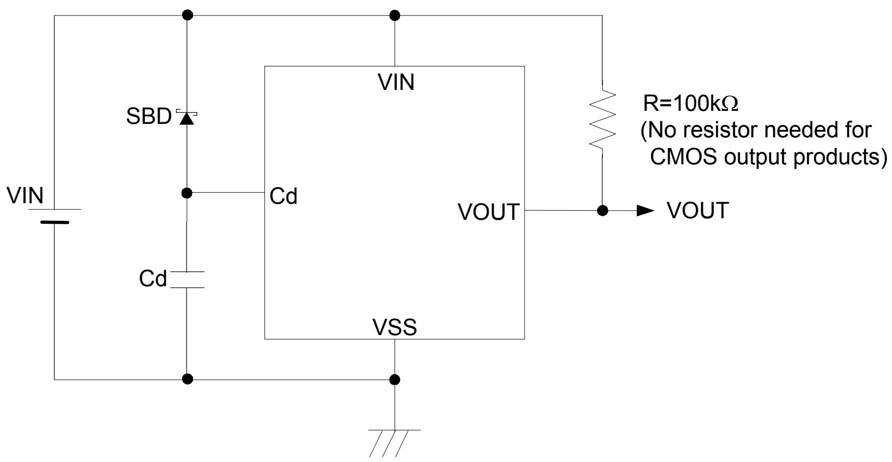

Figure 2: The timing chart of Figure 1



## ■NOTES ON USE

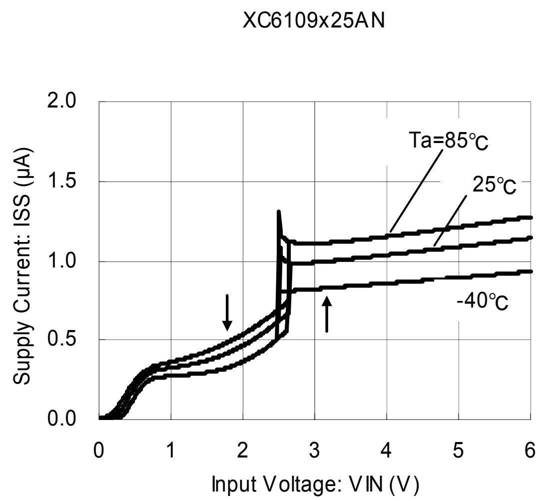
1. Use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.
2. The input pin voltage drops by the resistance between power supply and the $V_{IN}$ pin, and by through current at operation of the IC. At this time, the operation may be wrong if the input pin voltage falls below the minimum operating voltage range. In CMOS output, for output current, drops in the input pin voltage similarly occur. Oscillation of the circuit may occur if the drops in voltage, which caused by through current at operation of the IC, exceed the hysteresis voltage. Note it especially when you use the IC with the $V_{IN}$ pin connected to a resistor.
3. Note that a rapid and high fluctuation of the input pin voltage may cause a wrong operation.
4. When there is a possibility of which the input pin voltage falls rapidly (e.g.: 6.0V to 0V) at release operation with the delay capacitance pin (Cd) connected to a capacitor, use a schottky barrier diode connected between the $V_{IN}$ pin and the Cd pin as the Figure 3 shown below.

Figure 3: Circuit example with the delay capacitance pin (Cd) connected to a schottky barrier diode

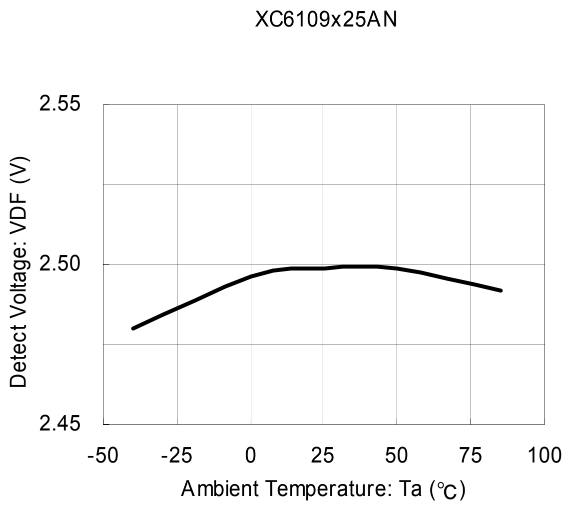


## ■TYPICAL PERFORMANCE CHARACTERISTICS

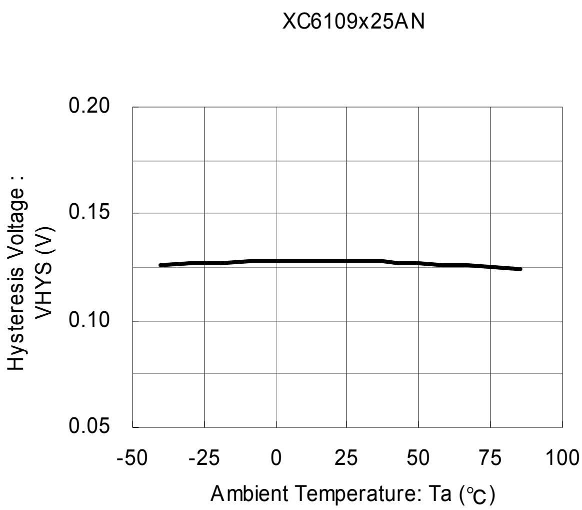
(1) Supply Current vs. Input Voltage



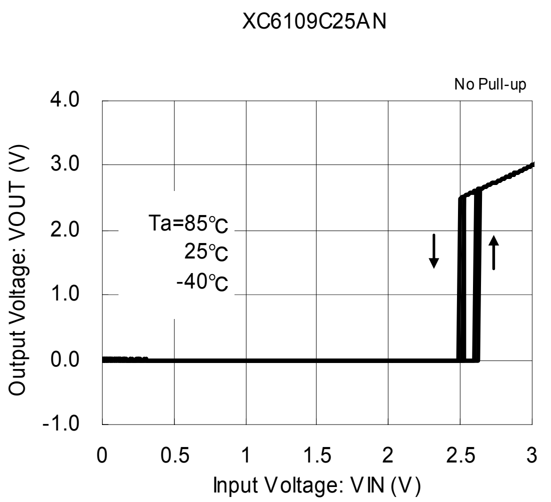

(2) Detect Voltage vs. Ambient Temperature

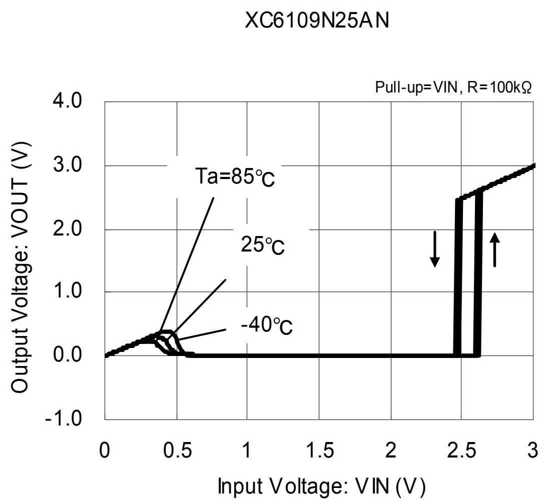



(3) Hysteresis Voltage vs. Ambient Temperature




(4) Output Voltage vs. Input Voltage

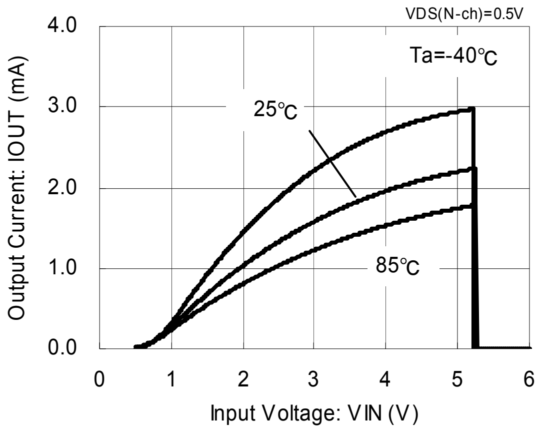


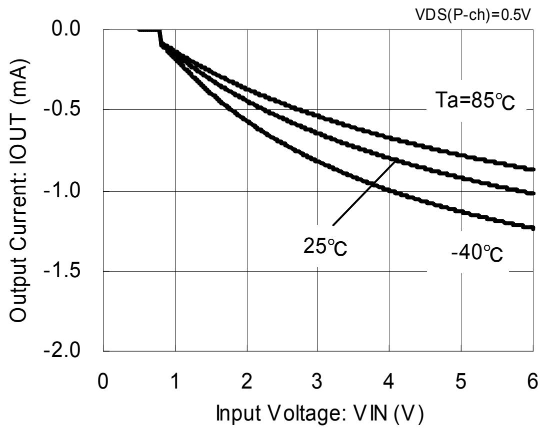
## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(5) Output Current vs. Input Voltage

XC6109x50AN

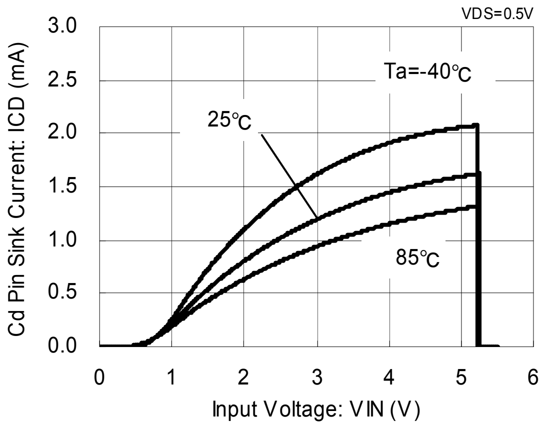



XC6109C08AN



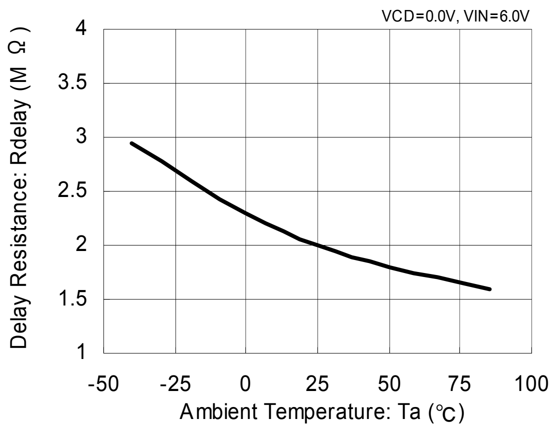

(6) Cd Pin Sink Current vs. Input Voltage

XC6109x50AN



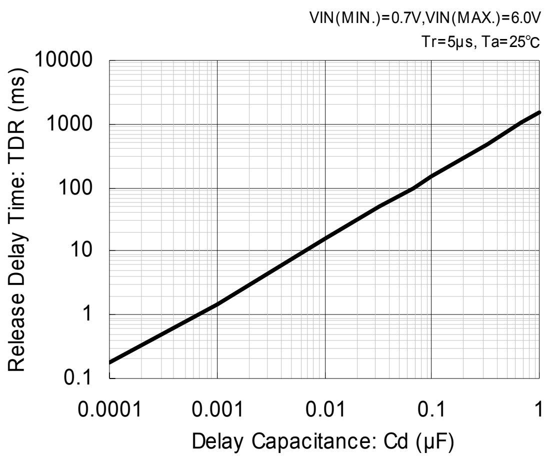

(7) Delay Resistance vs. Ambient Temperature

XC6109xxxAN



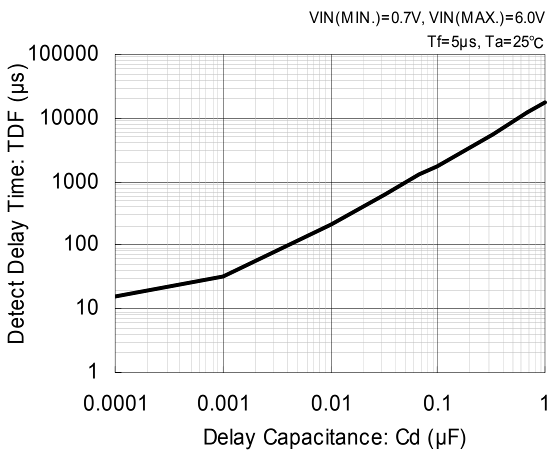

(8) Release Delay Time vs. Delay Capacitance

XC6109xxxAN




(9) Detect Delay Time vs. Delay Capacitance

XC6109xxxAN



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