XRD98L61

CCD Image Digitizers with CDS, PGA and 12-Bit A/D

May 2001-2

FEATURES

- 12-Bit Resolution ADC
- 20MHz Sampling Rate
- 10-Bit Programmable Gain: 0dB to 36dB PGA
- Digitally Controlled Offset-Calibration with Pixel Averager and Hot Pixel Clipper
- Widest Black Level Calibration Range at Maximum Gain
- DNS Filter Removes Black Level Digital Noise
- Manual Control of Offset DAC via Serial Port for use with High-speed Scanners
- 1ns/step Programmable Aperture Delay on SPIX, SBLK and ADCLK Sampling Clocks
- Single 2.7V to 3.6V Power Supply
- Optimized Power Consumption down to 125mW with External Resistor
- Low Power for Battery Operation
- Two Serially Controlled 8-Bit D/A Converters
- 0.1mA Stand-by Mode Current
- Three-state Digital Outputs
- 2,000V ESD Protection
- 48-Pin TQFP Package

APPLICATIONS

- Mega-pixel Digital Still Cameras
- Digital Camcorders
- 3-CCD Professional/Broadcast Camera
- Line Scan Cameras
- PC Video Cameras
- CCTV/Security Cameras
- Industrial/Medical Cameras
- 2D Bar Code Readers
- High Speed Scanners
- Digital Copiers

GENERAL DESCRIPTION

The XRD98L61 is a complete, low power CCD Image Digitizer for digital motion and still cameras. The product includes a high bandwidth differential Correlated Double Sampler (CDS), 10-bit digitally Programmable Gain Amplifier (PGA), 12-bit Analog-to-Digital Converter (ADC) and improved digitally controlled black level auto-calibration circuitry with programmable pixel averager, hot pixel clipper, and a DNS filter.

Two 8-bit serial controlled digital-to-analog converter (DACs) are provided to control external analog signals (Iris, Focus, Flash, etc.)

The Correlated Double Sampler (CDS) subtracts the CCD output signal black level from the video level. Common mode signal and power supply noise are rejected by the differential CDS input stage.

The PGA is digitally controlled with 10-bit resolution on a linear dB scale, resulting in a gain range of 0dB to 36dB with 0.047dB per LSB of the gain code.

The auto calibration circuit compensates for any internal offset of the XRD98L61 as well as black level offset from the CCD.

The PGA and black level auto-calibration are controlled through a simple 3-wire serial interface. The timing circuitry is designed to enable users to select a wide variety of available CCD and image sensors for their applications. Readback of the serial data registers is available from the digital output bus.

The XRD98L61 has direct access to the ADC and PGA inputs for digitizing other analog signals.

The XRD98L61 is packaged in 48-lead TQFP to reduce space and weight, and is suitable for hand-held and portable applications.

ORDERING INFORMATION

Part No.	Package	Temperature Range	Operating Power Supply	Maximum Sampling Rate
XRD98L61AIV	48-Pin TQFP	-40°C to 85°C	3.0V	20 MSPS

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 • (510) 668-7000 • FAX (510) 668-7017 • www.exar.com

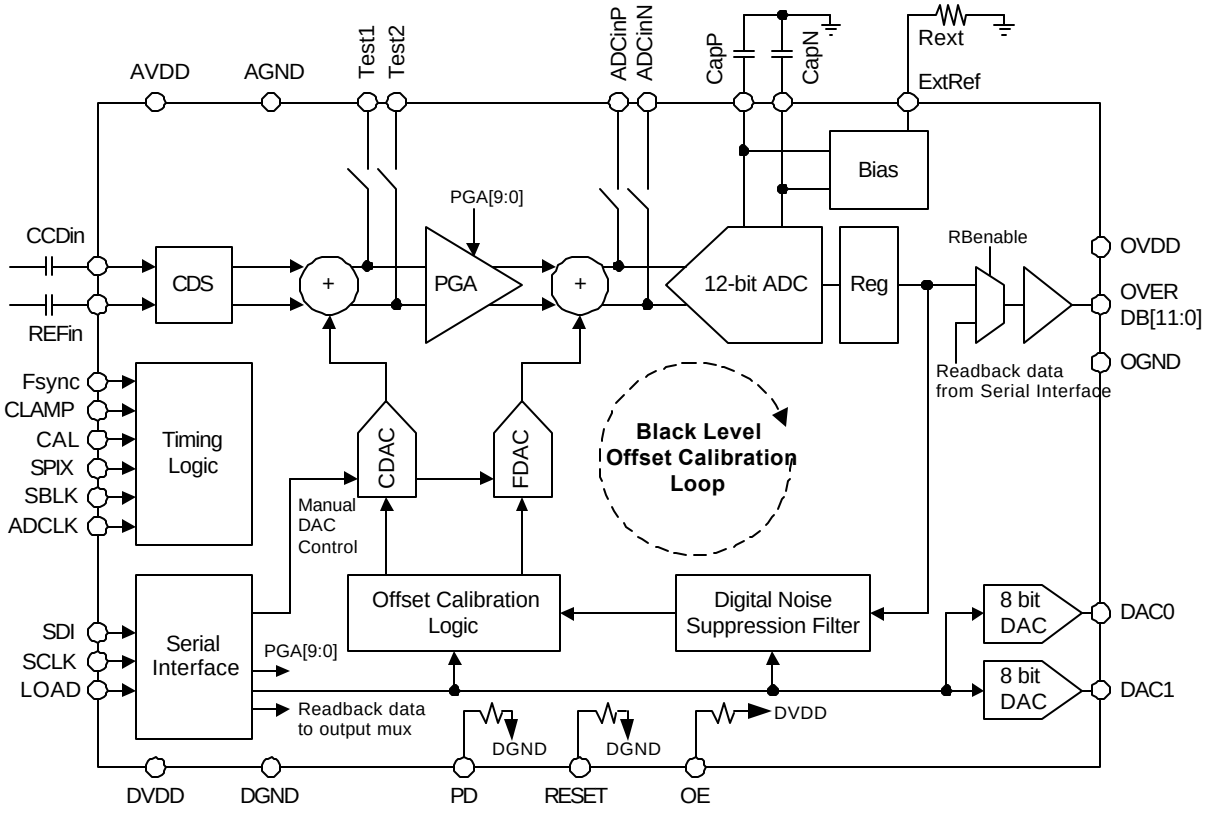


Figure 1. XRD98L61 Block Diagram

PIN CONFIGURATION

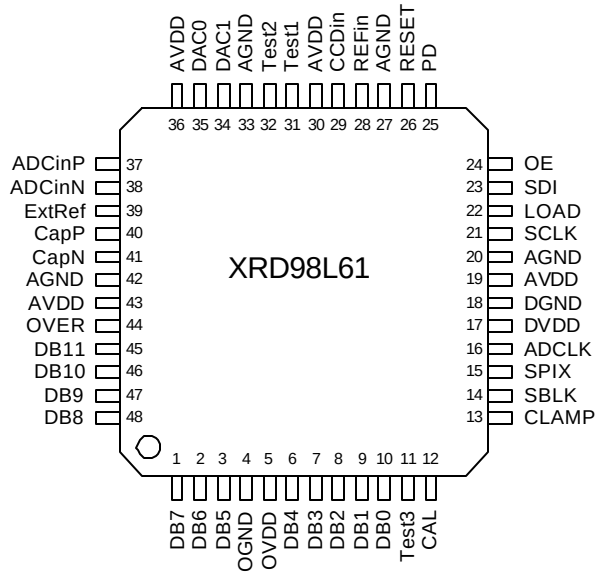


Figure 2. XRD98L61 Pinout

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	DB7	Digital Out	ADC Output
2	DB6	Digital Out	ADC Output
3	DB5	Digital Out	ADC Output
4	OGND	Ground	Digital Output Ground
5	OV_{DD}	Power	Digital Output Power Supply (must be < AV_{DD})
6	DB4	Digital Out	ADC Output
7	DB3	Digital Out	ADC Output
8	DB2	Digital Out	ADC Output
9	DB1	Digital Out	ADC Output
10	DB0	Digital Out	ADC Output (LSB)
11	Test3	Digital In	Test Pin. Connect to DV_{DD}.
12	CAL	Digital In	Calibration Control (clamp OB)
13	CLAMP	Digital In	DC-Restore Clamp Control
14	SBLK	Digital In	Sample Black CDS Clock
15	SPIX	Digital In	Sample Pixel CDS Clock
16	ADCLK	Digital In	ADC Clock
17	DV_{DD}	Power	On chip Logic Power Supply (must = AV_{DD})
18	DGND	Ground	On chip Logic Ground
19	AV_{DD}	Power	Analog Power Supply
20	AGND	Ground	Analog Ground
21	SCLK	Digital In	Serial Interface Shift Clock
22	LOAD	Digital In	Serial Interface Data Load
23	SDI	Digital In	Serial Interface Data Input
24	OE	Digital In	Output Enable Control 1=enable, 0=high-Z
25	PD	Digital In	Power Down Control 1=powerdown, 0=convert
26	RESET	Digital In	Reset Control 1=reset, 0=convert
27	AGND	Ground	Analog Ground
28	REFin	Analog	CCD Reference Signal
29	CCDin	Analog	CCD Input Signal
30	AV_{DD}	Power	Analog Power Supply
31	Test1	Analog	Direct PGA Input (inverting input)
32	Test2	Analog	Direct PGA Input (non-inverting input)
33	AGND	ground	Analog Ground
34	DAC1	Analog	Utility DAC 1 Output
35	DAC0	Analog	Utility DAC 0 Output
36	AV_{DD}	Power	Analog Power Supply
37	ADCinP	Analog	Direct ADC Input (non-inverting input)
38	ADCinN	Analog	Direct ADC Input (inverting input)
39	ExtRef	Analog	External Reference Resistor to Ground (R_{EXT})
40	CapP	Analog	ADC Reference By-Pass
41	CapN	Analog	ADC Reference By-Pass
42	AGND	Ground	Analog Ground
43	AV_{DD}	Power	Analog Power Supply
44	OVER	Digital Out	ADC Out of Range Bit
45	DB11	Digital Out	ADC Output (MSB)
46	DB10	Digital Out	ADC Output
47	DB9	Digital Out	ADC Output
48	DB8	Digital Out	ADC Output

DC ELECTRICAL CHARACTERISTICS – XRD98L61
Unless otherwise specified: OV_{DD} = DV_{DD} =AV_{DD} = 3.0V, Pixel Rate = 20MSPS, T_A = 25°C
Rext= 30 KOhm

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CDS Performance						
$CDSV_{IN}$	Input Range			800	mV_{PP}	Pixel (V_{BLK} - V_{VIDEO}), (See Figure 2)
V_{DARK}	Maximum Dark Voltage Offset		250		mV	At any gain. (See Figure 2)
Vrst	Reset Pulse			500	mV	
r_{CLAMP}	Clamp On Resistance		80		Ω	
PGA Parameters						
AV_{MIN}	Minimum Gain	-1.0	0	+1.0	dB	Gain Code = 0
AV_{MAX}	Maximum Gain	32.5	36	39.5	dB	GainCode ≥ 768
PGA n	Resolution		10		Bits	Transfer function is linear steps in dB
PGA Step	Gain Step Size		0.047		dB	
ADC Parameters (Measured in ADC Test Mode)SDI = 0010 001 0011 1000						
ADC n	Resolution	12			Bits	
f_S	Max Sample Rate	20			MSPS	
DNL	Differential Non-Linearity	-1.0	±0.75	+1.0	LSB	
V_{ID}	Full Scale Differential Input		±1.0		V	
ΔV_{REF}	ADC Reference Voltage		1		V	CapP - CapN = ΔV_{REF}
DAC Parameters						
DACn	Resolution	8			Bits	Guaranteed Monotonic
V_{MAX}	Vout Max		2.25		Volt	
V_{MIN}	Vout Min		0.25		Volt	
t_S	Settling Time		5		μs	
R_L	Output Load	20			KOhm	Buffer is needed for resistive load <20KΩ

DC ELECTRICAL CHARACTERISTICS - XRD98L61 (CONT'D)
Unless otherwise specified: OV_{DD} = DV_{DD} =AV_{DD} = 3.0V, Pixel Rate = 20MSPS, T_A = 25°C
Rext= 30KOhm

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
System Specifications						
DNL_S	System DNL	-1.0	±0.75	+1.0	LSB	No missing codes, monotonic
$e_{n\ MAXAV}$	Input Referred Noise, Max.Gain		180		μV_{rms}	Gain Code = 768 (36db)
$e_{n\ MINAV}$	Input Referred Noise, Min.Gain		800		μV_{rms}	Gain Code = 0 (0dB)
Latency	Pipeline Delay			7.5	cycles	
Digital Inputs (Digital Input Thresholds are Set by DV_{DD})						
V_{IH}	Digital Input High Voltage	2.5			V	
V_{IL}	Digital Input Low Voltage			0.5	V	
I_{IH}	Input Leakage, P/D & Reset	20	40	100	µA	Input = V_{DD}
I_{IH}	Input Leakage, OE	-.50	0	.50	µA	Input = V_{DD}
I_{IL}	Input Leakage, P/D & Reset	-.50	0	.50	µA	Input = GND
I_{IL}	Input Leakage, OE	-40	-5	0	µA	Input = GND
I_{IL} / I_{IH}	Input Leakage, All Other Inputs	-100	10	100	nA	Input = V_{DD} or GND
C_{IN}	Input Capacitance		5		pF	
Digital Outputs						
V_{OH}	Digital Output High Voltage	OV_{DD}-0.5			V	While sourcing 2mA
V_{OL}	Digital Output Low Voltage			0.5	V	While sinking 2mA
I_{OZ}	High–Z Leakage	-1		+1	µA	OE = 0 or PD = 1

DC ELECTRICAL CHARACTERISTICS - XRD98L61 (CONT'D)
Unless otherwise specified: OV_{DD} = DV_{DD} =AV_{DD} = 3.0V, Pixel Rate = 20MSPS, T_A = 25°C

Rext=30KOhm

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Digital I/O Timing						
t_{DL}	Data Valid Delay		12		ns	10 pF load
t_{PW1}	Pulse Width of SPIX	10			ns	
t_{PW2}	Pulse Width of SBLK	10			ns	
t_{PIX}	Pixel Period	50			ns	
t_{BK}	Sample Black (SBLK), Aperture Delay	4	7	10	ns	
t_{VD}	Sample Video (SPIX), Aperture Delay	4	7	10	ns	
t_{SCLK}	Shift Clock Period		100		ns	
t_{SET}	Shift Register Setup Time	10			ns	
t_{HOLD}	Shift Register Hold Time			0	ns	
t_{L1}	Load Set-up Time	10			ns	
t_{L2}	Load Hold Time			0	ns	
Power Supplies						
AV_{DD}	Analog Supply Voltage	2.7	3.0	3.6	V	
DV_{DD}	Digital Supply Voltage	2.7	3.0	3.6	V	Set DV_{DD} = AV_{DD}
OV_{DD}	Digital Output Supply Voltage	2.7	3.0	3.6	V	$OV_{DD} \leq AV_{DD}$
I_{DD}	Supply Current		42		mA	OV_{DD} = AV_{DD} = DV_{DD} =3.0V, Includes Reference Current.
I_{DDPD}	Power Down Supply Current		0.01	0.1	mA	PD = 1

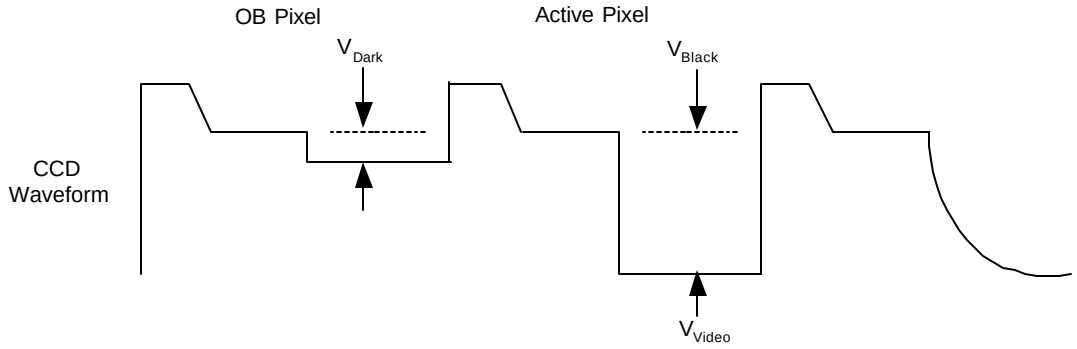


Figure 3. Definition of terms for V_{Out} of the CCD waveform: $CDSV_{IN} = (V_{Black} - V_{Video})$

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND ..... +6.6V
V_{RT} & V_{RB} ..... V_{DD} +0.5 to GND -0.5V
V_{IN} ..... V_{DD} +0.5 to GND -0.5V
All Inputs ..... V_{DD} +0.5 to GND -0.5V
All Outputs ..... V_{DD} +0.5 to GND -0.5V
Storage Temperature ..... -65°C to 150°C
Lead Temperature (Soldering 10 seconds) ..... 300°C
Maximum Junction Temperature ..... 150°C
Package Power Dissipation Ratings (T_A= +70°C)
TQFP ..... θ_{JA} = 105°C/W
ESD 2000V

Notes:

1 *Stresses above those listed as "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

2 *Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.*

3 *V_{DD} refers to AV_{DD}, OV_{DD} and DV_{DD}. GND refers to AGND, OGND and DGND.*

SERIAL INTERFACE

The XRD98L61 uses a three wire serial interface (LOAD, SDI & SCLK) to access the programmable features and controls of the chip. The serial interface uses a 16-bit shift register. The first 6 bits shifted in are the address bits; the next 10 bits are the data bits. The address bits select which of the internal registers will receive the 10 data bits. The interface will only load data from the shift register into the register array if there are exactly 16 rising edges of SCLK while LOAD is low. If more or less rising edges are present, the data is discarded. There is no checking of the address bits to ensure a valid register is written to. If the address bits select an undefined register, the data will be discarded. There is a readback function (see Serial Interface Readback section), which outputs the contents of a selected register on pins DB[11:2] of the digital output bus.

The following is the procedure for writing to the serial interface:

1) Force LOAD pin low to enable the shift register.
2) Shift in 16 bits, 6 address bits (msb first), followed by 10 data bits (msb first).
3) Force LOAD pin high to transfer data from the shift register to the serial interface register array.

Note: *There must be exactly 16 rising edges of SCLK while LOAD is low.*

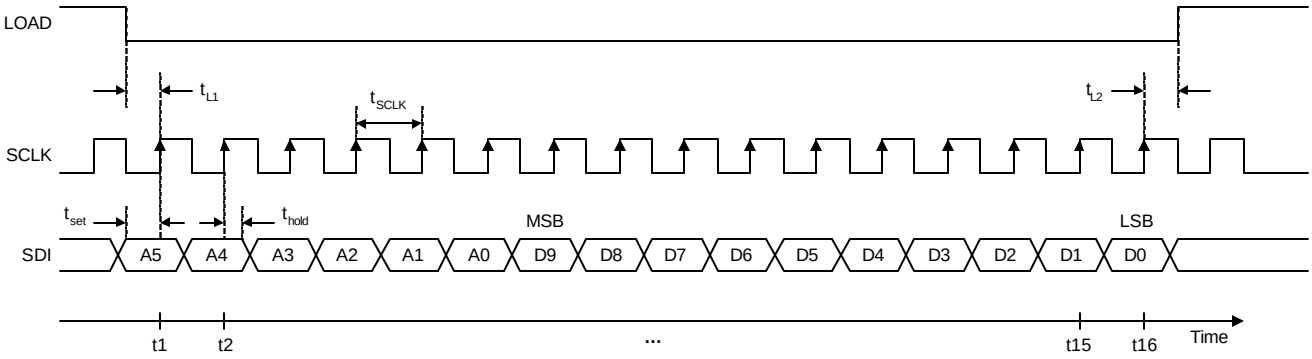


Figure 4. Serial Interface Timing Diagram

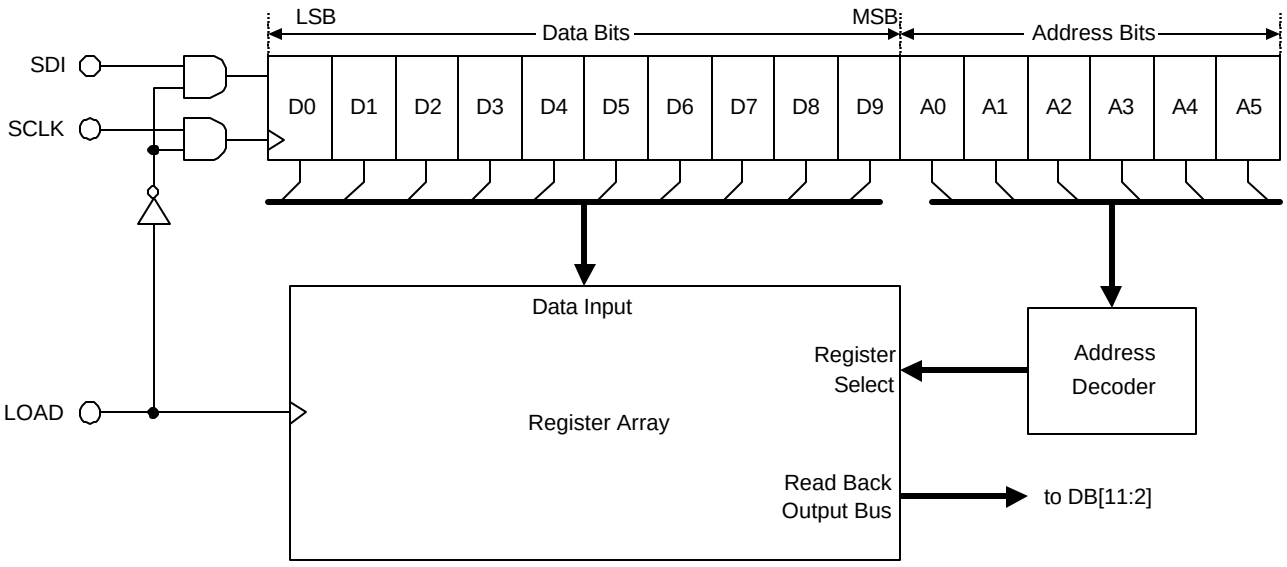


Figure 5. Serial Interface Block Diagram

	Address bits						Data bits									
Reg. Name	A5	A4	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Gain	0	0	0	0	0	0	PGA[9] 0	PGA[8] 0	PGA[7] 0	PGA[6] 0	PGA[5] 0	PGA[4] 0	PGA[3] 0	PGA[2] 0	PGA[1] 0	PGA[0] 0
Offset	0	0	0	0	0	1			OB[7] 1	OB[6] 0	OB[5] 0	OB[4] 0	OB[3] 0	OB[2] 0	OB[1] 0	OB[0] 0
Calibration	0	0	0	0	1	0	Avg[2] 1	Avg[1] 0	Avg[0] 1	Mode 0	LFrame 0	DNS[1] 1	DNS[0] 1	FastCal 1	Hold 0	ManCal 0
Wait A	0	0	0	0	1	1	WL[11] 0	WL[10] 0	WL[9] 0	WL[8] 0	WL[7] 0	WL[6] 0	WL[5] 0	WL[4] 0	WL[3] 0	WL[2] 0
Wait B	0	0	0	1	0	0									WL[1] 0	WL[0] 1
OB Lines	0	0	0	1	0	1			OBL[7] 0	OBL[6] 0	OBL[5] 0	OBL[4] 0	OBL[3] 0	OBL[2] 0	OBL[1] 1	OBL[0] 0
CDAC	0	0	0	1	1	0		CDAC[8] 0	CDAC[7] 0	CDAC[6] 0	CDAC[5] 0	CDAC[4] 0	CDAC[3] 0	CDAC[2] 0	CDAC[1] 0	CDAC[0] 0
FDAC	0	0	0	1	1	1	FDAC[9] 0	FDAC[8] 0	FDAC[7] 0	FDAC[6] 0	FDAC[5] 0	FDAC[4] 0	FDAC[3] 0	FDAC[2] 0	FDAC[1] 0	FDAC[0] 0
Control	0	0	1	0	0	0	DIGtest 0	ADCtest 0	NoCDS 0	LowPwr 0	OE 1	DAC1pd 1	DAC0pd 1	AFEpd 0	ADCpd 0	PwrDwn 0
Polarity	0	0	1	0	0	1					SBLKpol 0	SPIXpol 0	CALpol 0	CLAMPpol 0	*Reserved 0	ADCpol 0
Clock	0	0	1	0	1	0	CLKtest 0	Nullamp 0	CMtest 0	Fastclk 0	CLAMPopt 0	OneShot 0	ClampCal 0	SPIXopt 0	RSTreject 0	VSreject 0
Delay A	0	0	1	0	1	1		DelayA[8] 0	DelayA[7] 0	DelayA[6] 0	DelayA[5] 0	DelayA[4] 0	DelayA[3] 0	DelayA[2] 0	DelayA[1] 0	DelayA[0] 0
Delay B	0	0	1	1	0	0		DelayB[8] 0	DelayB[7] 0	DelayB[6] 0	DelayB[5] 0	DelayB[4] 0	DelayB[3] 0	DelayB[2] 0	DelayB[1] 0	DelayB[0] 0
DAC0	0	0	1	1	0	1			DAC0[7] 0	DAC0[6] 0	DAC0[5] 0	DAC0[4] 0	DAC0[3] 0	DAC0[2] 0	DAC0[1] 0	DAC0[0] 0
DAC1	0	0	1	1	1	0			DAC1[7] 0	DAC1[6] 0	DAC1[5] 0	DAC1[4] 0	DAC1[3] 0	DAC1[2] 0	DAC1[1] 0	DAC1[0] 0
ReadBack	1	1	1	1	1	0	RBenable 0	RBreg[8] 0	RBreg[7] 0	RBreg[6] 0	RBreg[5] 0	RBreg[4] 0	RBreg[3] 0	RBreg[2] 0	RBreg[1] 0	RBreg[0] 0
Reset	1	1	1	1	1	1										Reset 0

Table 1. Serial Interface Register Address Map & default values

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Gain	PGA[9]	PGA[8]	PGA[7]	PGA[6]	PGA[5]	PGA[4]	PGA[3]	PGA[2]	PGA[1]	PGA[0]
Default	0	0	0	0	0	0	0	0	0	0

Gain Register (Reg. 0, Address 000000)

The Gain register is used to set the gain of the Programmable Gain Amplifier (PGA).
Code 0000000000 is minimum gain (0 dB). Codes 1011111111 and greater are maximum gain (36 dB).
See the Programmable Gain Amplifier (PGA) section for more information.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Offset			OB[7]	OB[6]	OB[5]	OB[4]	OB[3]	OB[2]	OB[1]	OB[0]
Default	0	0	1	0	0	0	0	0	0	0

Offset Register (Reg. 1, Address 000001)

The Offset register is used to set the target ADC output code for Optical Black pixels.
See the Black Level Offset Calibration section for more information.

NOTE: *Reserved Test register bit. Used for factory test only. Please do not modify.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Calibration	Avg[2]	Avg[1]	Avg[0]	Mode	LFrame	DNS[1]	DNS[0]	FastCal	Hold	ManCal
Default	1	0	1	0	0	1	1	1	0	0

Calibration Register (Reg. 2, Address 000010)

The Calibration register is used to set various options for the Black Level Offset Calibration.
Avg[2:0] set the number of OB pixels to average:

000 = 4 pixels (not recommended) 100 = 64 pixels
001 = 8 pixels (not recommended) 101 = 128 pixels (default)
010 = 16 pixels (not recommended) 110 = 256 pixels
011 = 32 pixels 111 = 512 pixels

Mode=0, selects Line mode calibration (use OB pixels at start or end of each line).
Mode=1, do not use.
LFrame=0, selects Line mode calibration.
LFrame=1, do not use.
DNS[1:0] selects the Digital Noise Suppression filter setting:

00 = off, 10 = medium,
01 = narrow, 11 = wide.

FastCal=0, disables speedup convergence option of the calibration feedback loop.
FastCal=1, enables an option to speedup convergence of the calibration feedback loop.
Hold=0, normal operation of calibration feedback loop.
Hold=1, stops all updates to the Coarse and Fine offset DAC accumulators.
ManCal=0, normal operation of calibration feedback loop.
ManCal=1, enables manual calibration. The offset DACs are set to the values in the CDAC and FDAC registers.

See the Black Level Offset Calibration section for more information.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WaitA	WL[11]	WL[10]	WL[9]	WL[8]	WL[7]	WL[6]	WL[5]	WL[4]	WL[3]	WL[2]
Default	0	0	0	0	0	0	0	0	0	0

WaitA Register (Reg. 3, Address 000011)

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WaitB									WL[1]	WL[0]
Default	0	0	0	0	0	0	0	0	0	1

WaitB Register (Reg. 4, Address 000100)

The WaitA and WaitB registers are concatenated to make up the Wait register.
See OB Pixel calibration section for more information.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OB Lines			OBL[7]	OBL[6]	OBL[5]	OBL[4]	OBL[3]	OBL[2]	OBL[1]	OBL[0]
Default	0	0	0	0	0	0	0	0	1	0

OB Lines Register (Reg. 5, Address 000101)

The OB Lines register is used by the Offset Calibration Logic to set the number of Optical Black lines used for Calibration in the Frame Mode. Do not use.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CDAC		CDAC[8]	CDAC[7]	CDAC[6]	CDAC[5]	CDAC[4]	CDAC[3]	CDAC[2]	CDAC[1]	CDAC[0]
Default	0	0	0	0	0	0	0	0	0	0

CDAC Register (Reg. 6, Address 000110)

The CDAC register is used to set the Coarse Offset DAC in the Manual Calibration mode. See Calibration Option, in the Black Level Offset Calibration section for more information.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FDAC	FDAC[9]	FDAC[8]	FDAC[7]	FDAC[6]	FDAC[5]	FDAC[4]	FDAC[3]	FDAC[2]	FDAC[1]	FDAC[0]
Default	0	0	0	0	0	0	0	0	0	0

FDAC Register (Reg. 7, Address 000111)

The FDAC register is used to set the Fine Offset DAC in the Manual Calibration mode. See Calibration Option, in the Black Level Offset Calibration section for more information.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Control	DIGtest	ADCtest	NoCDS	LowPwr	OE	DAC1pd	DAC0pd	AFEpd	ADCpd	PwrDwn
Default	0	0	0	0	1	1	1	0	0	0

Control Register (Reg. 8, Address 001000)

The Control register is used to set various test and power-down modes.

DIGtest=0, normal operation.

DIGtest=1, Exar test mode - do not use.

ADCtest=0, connects PGA output to ADC input.

ADCtest=1, connects ADCinP & ADCinN pins to ADC input.

NoCDS=0, connects CDS output to PGA input.

NoCDS=1, connects Test1 & Test2 pins to PGA inputs (CDS by-pass mode).

Low Power=0, normal operation.

Low Power=1, Exar test mode - do not use.

OE=0, digital outputs in high-Z state.

OE=1, digital outputs enabled.

DAC1pd=1, Utility DAC1 is powered down.

DAC0pd=1, Utility DAC0 is powered down.

AFEpd=0, normal operation.

AFEpd=1, CDS & PGA are powered down, do not use.

ADCpd=0, normal operation.

ADCpd=1, ADC is powered down, do not use.

PwrDwn=0, normal operation.

PwrDwn=1, the whole chip is powered down.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Polarity					SBLKpol	SPIXpol	CALpol	CLAMPpol	*Reserved	ADCpol
Default	0	0	0	0	0	0	0	0	0	0

Polarity Register (Reg. 9, Address 001001)

The Polarity register is used to set the polarity for the 6 input clock signals.
For each clock: polarity bit=0 sets clock active low, polarity bit=1 sets clock active high.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Clock	CLKtest	Nullamp	CMtest	Fastclk	CLAMPopt	Oneshot	ClampCal	SPIXopt	RSTreject	VSreject
Default	0	0	0	0	0	0	0	0	0	0

Clock Register (Reg. 10, Address 001010)

The Clock register is used to set various clocking options.
CLKtest=0, Normal operation.
CLKtest=1, Exar test mode - Do not use.
Nullamp=0, Normal operation.
Nullamp=1, Exar test mode - Do not use.
CMtest=0, Normal operation.
CMtest=1, Exar test mode - Do not use.
Fastclk=0, Normal operation.
Fastclk=1, Exar test mode - Do not use.
CLAMPopt=0, DC Restore bias is on only during CLAMP.
CLAMPopt=1, DC Restore bias is always ON.
OneShot=0, CAL defines OB pixels. Clamp controls DC restore.
OneShot=1, CAL controls DC restore and defines OB pixels. CLAMP used for VS reject.
ClampCal=0, CLAMP at start of line, CAL at end of line (affects VS reject).
ClampCal=1, CAL at start of line, CLAMP at end of line (affects VS reject).
SPIXopt=0, ϕ2 starts DelayA[5:3] + DelayB[8:6] after SBLK trailing edge
SPIXopt=1, ϕ2 starts DelayB[2:0] after SPIX pin leading edge.
RSTreject=0, Reset reject switch (ϕ3) not clocked, always on.
RSTreject=1, Reset reject switch (ϕ3) clocked.
VSreject=0, Vertical Shift Reject is inactive.
VSreject=1, Vertical Shift Reject is active.

NOTE: *Reserved Test Register bit. Used for factory test only. Please do not modify.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Delay A		DelayA[8]	DelayA[7]	DelayA[6]	DelayA[5]	DelayA[4]	DelayA[3]	DelayA[2]	DelayA[1]	DelayA[0]
Default	0	0	0	0	0	0	0	0	0	0

Delay A Register (Reg. 11, Address 001011)

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Delay B		DelayB[8]	DelayB[7]	DelayB[6]	DelayB[5]	DelayB[4]	DelayB[3]	DelayB[2]	DelayB[1]	DelayB[0]
Default	0	0	0	0	0	0	0	0	0	0

DelayB Register (Reg. 12, Address 001100)

The DelayA & DelayB registers are used to add internal delay to the pixel rate clocks.
For each 3 bit delay parameter, 000 is minimum delay, 111 is maximum delay (~7ns).
DelayA[8:6]: ADC Clock delay.
DelayA[5:3]: ϕ1 trailing edge delay.
DelayA[2:0]: ϕ1 leading edge delay.
DelayB[8:6]: Delay for SPIX option.
DelayB[5:3]: ϕ2 trailing edge delay.
DelayB[2:0]: ϕ2 leading edge delay.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DAC0			DAC0[7]	DAC0[6]	DAC0[5]	DAC0[4]	DAC0[3]	DAC0[2]	DAC0[1]	DAC0[0]
Default	0	0	0	0	0	0	0	0	0	0

DAC0 Register (Reg. 13, Address 001101)

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DAC1			DAC1[7]	DAC1[6]	DAC1[5]	DAC1[4]	DAC1[3]	DAC1[2]	DAC1[1]	DAC1[0]
Default	0	0	0	0	0	0	0	0	0	0

DAC1 Register (Reg. 14, Address 001110)

The DAC1 & DAC0 registers are used to program the two 8-bit Utility DACs.

Code 00000000 is minimum output voltage.
Code 11111111 is maximum output voltage.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ReadBack	RBenable	RBreg[8]	RBreg[7]	RBreg[6]	RBreg[5]	RBreg[4]	RBreg[3]	RBreg[2]	RBreg[1]	RBreg[0]
Default	0	0	0	0	0	0	0	0	0	0

Readback Register (Reg. 62, Address 111110)

The readback register is used to enable the readback function and select a register for readback.

RBenable=0, Readback disabled.

RBenable=1, Readback enabled. Contents of selected register is output on DB[11:2] pins.

RBreg[8:0], select register to read from, see table in Serial Interface Read Back section.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Reset										Reset
Default	0	0	0	0	0	0	0	0	0	0

Reset Register (Reg. 63, Address 111111)

The Reset register is used to reset the entire chip.
Reset=0, Normal operation.
Reset=1, Resets the chip. The Reset bit will automatically reset after approximately 10 ns delay.

SERIAL INTERFACE READ BACK

The readback function is used to view the content of the serial interface registers as well as several key registers in the calibration logic. Readback is enabled by writing a 1 to the RBenable bit of the Readback register, bit D9 of register 62.

In the readback mode, the content of the selected register is output on the 10 MSBs of the ADC output bus pins DB[11:2]. As long as valid clocks and CCD signal are applied, the calibration will continue to function properly during readback (internally the ADC data is still sent to the calibration logic).

Registers are selected for readback by writing to the RBreg[8:0] bits in the Readback register, bits D8 to D0 of register 62. If RBreg[8:6]=000, then RBreg[5:0] are used to address the serial interface registers. Currently only register addresses 0 to 14, 62 and 63 are defined. If RBreg[8:6]≠000, then RBreg[5:0] are ignored and RBreg[8:6] are used to address registers in the calibration logic. Currently only three calibration registers are accessible.

RBenable	RBreg 8	RBreg 7	RBreg 6	RBreg 5	Rbreg 4	RBreg 3	RBreg 2	RBreg 1	RBreg 0	Selected Register
0	x	x	x	x	x	x	x	x	x	none (ADC data output)
1	0	0	0	0	0	0	0	0	0	Gain
1	0	0	0	0	0	0	0	0	1	Offset
1	0	0	0	0	0	0	0	1	0	Calibration
1	0	0	0	0	0	0	0	1	1	Wait A
1	0	0	0	0	0	0	1	0	0	Wait B
1	0	0	0	0	0	0	1	0	1	OB Lines
1	0	0	0	0	0	0	1	1	0	CDAC
1	0	0	0	0	0	0	1	1	1	FDAC
1	0	0	0	0	0	1	0	0	0	Control
1	0	0	0	0	0	1	0	0	1	Polarity
1	0	0	0	0	0	1	0	1	0	Clock
1	0	0	0	0	0	1	0	1	1	Delay A
1	0	0	0	0	0	1	1	0	0	Delay B
1	0	0	0	0	0	1	1	0	1	DAC0
1	0	0	0	0	0	1	1	1	0	DAC1
1	0	0	0	1	1	1	1	1	0	ReadBack
1	0	0	0	1	1	1	1	1	1	Reset
1	0	0	1	x	x	x	x	x	x	FDAC output from Cal. logic
1	0	1	0	x	x	x	x	x	x	CDAC output from Cal. logic
1	0	1	1	x	x	x	x	x	x	Avg. output from Cal logic

Table 2. Read-back Register Selection

CORRELATED DOUBLE SAMPLE/HOLD (CDS)

The function of the CDS block is to sense the voltage difference between the black level and video level for each pixel. The PGA then amplifies this difference to the desired level for the ADC. The CDS and PGA are fully differential. The CCDin pin should be connected, via a capacitor, to the CCD output signal. The REFin pin should be connected, via a capacitor, to the CCD "Common" voltage (typically the CCD ground is used as the "Common" voltage). These capacitors, C1 and C2, are typically 0.01µF ± 10% or better matching.

The timing for the switches shown in Figure 6 are determined by ϕ1, ϕ2, and ϕ3. ϕ1, ϕ2, and ϕ3 are internally generated from the timing signals SBLK and SPIX shown in Figures 17 & 18. ϕ3 (reset reject switches) are closed to simplify the operation described below.

At the beginning (or end) of every video line, the DC restore switch forces one side of the external capacitors to an internal bias level (Vbias1=1.2V). The DC restore switch is controlled by the combination of the CLAMP input signal ANDed with the ϕ2 clock.

During the black reference phase of each CCD pixel, the ϕ1 (Sample Black Reference) switches are turned on, shorting the PGA1 inputs to a second bias level (Vbias2). The Coarse Offset DAC adds an adjustment to the bias level (Vbias2) to cancel black level offset in the CCD signal. When the ϕ1 switches turn off, the pixel black reference level is sampled on the internal black sample capacitors, and the PGA is ready to gain up the CCD video signal.

During the video phase of each CCD pixel, the difference between the pixel black level and video level is transmitted through the internal black sample capacitors and converted to a fully differential signal by the PGA1 amplifier. At this time, the ϕ2 (Sample Pixel value) switches turn on, and the internal video sample capacitors track the amplified difference. The Fine Offset DAC adds offset adjustment to the PGA2 output (post gain).

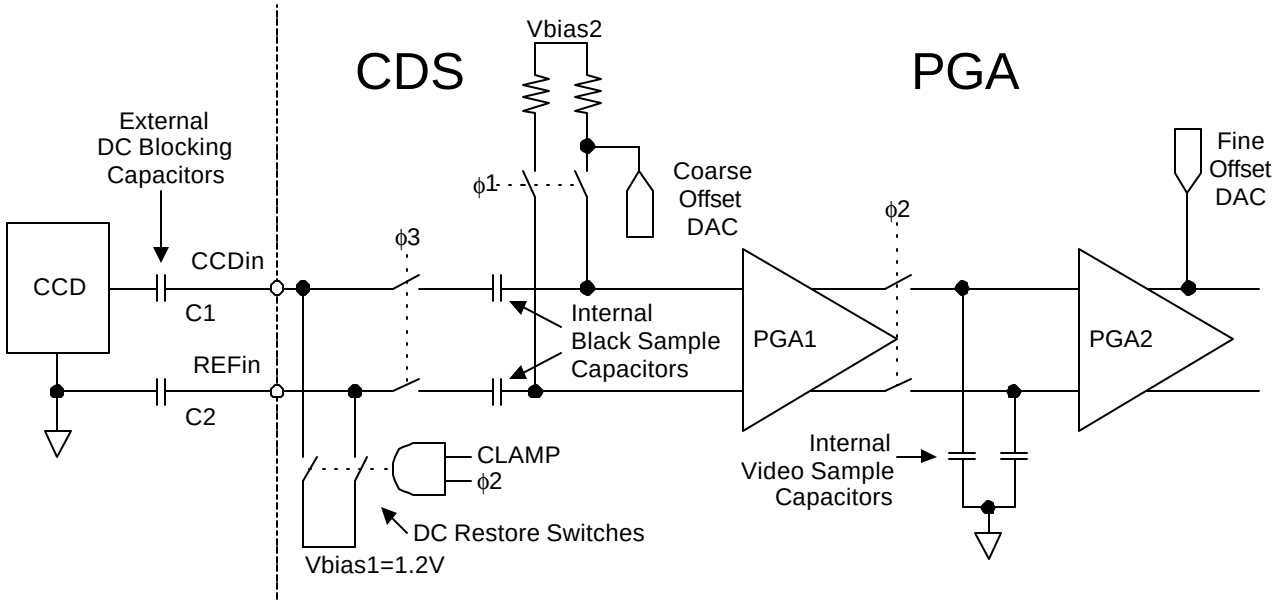


Figure 6. CDS and PGA Block Diagram

4.0 Programmable Gain Amplifier (PGA)

The PGA provides gains from 0dB to 36 dB in approximately 0.047 dB steps. The desired gain setting is programmed via the 10 bit gain register in the Serial Interface.

For gain codes between 0 and 767, the gain can be calculated by the following equation:

$$Gain[dB] = \left(\frac{Code}{768} \times 36 \right)$$

For gain codes ≥ 768, the gain is fixed at 36 dB. The gain doubles every 128 codes to simplify DSP algorithms and control.

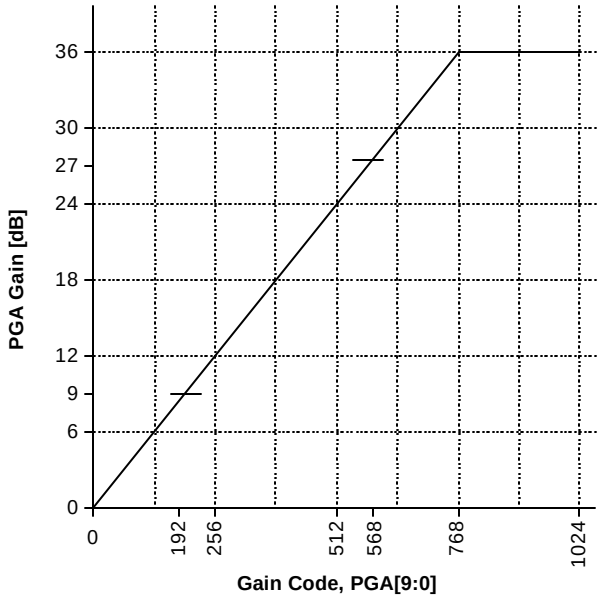


Figure 7. PGA Gain vs. Gain Code

An example of setting the gain is as follows: If the CCD input is limited by 800mVpp ($CDSV_{IN}$) and the ADC full scale differential input (VID) is 2Vpp, then a minimum gain is calculated by:

$$Gain = 20 \log \left(\frac{VID}{CDSV_{IN}} \right) = 20 \log \left(\frac{2}{0.8} \right) = 8dB$$

The gain code would be set to 170d for 8dB of PGA gain.

DIRECT PGA INPUT MODE

The inputs to the PGA can be accessed directly (bypassing the CDS) through the Test1 & Test2 pins (See Figure 1). The test inputs require Test2 set to a dc voltage of 1.2V and the Test1 input signal between 1.2V and 0.4V. ADC Zero Scale (000h) is at 1.2V input and Full Scale (FFFh)for a 0.4V input assuming a gain of 8dB. (ADC full scale input is 2Vpp.)

To enable the Direct PGA Input mode, write a "1" to the NoCDS bit in the Control register of the serial interface. This will disconnect the CDS from the PGA input and turn on the switches that connect the Test1 & Test2 pins to the PGA. Note that when the part is not in the NoCDS mode that Test1 and Test2 are grounded through an equivalent 10kohm switch resistance. To avoid shorting the input drive circuitry into Test1 and Test2 to ground, the NoCDS mode must be active before the input signal is driven.

In this mode, the SBLK and SPIX clocks must be clocked, due to the switched capacitor architecture of the second PGA stage. ADCLK must be provided to digitize the PGA output. The analog PGA output cannot be monitored; it does not come out to any pin.

The calibration logic should be put into the Hold mode, or into the ManCAL mode. The Coarse offset correction DAC (CDAC) is disconnected from the PGA inputs in this mode. The CDAC does not affect the Direct PGA inputs, but the Fine offset correction DAC (FDAC) does affect the PGA output. The FDAC range is +-128mV at the ADC input. FDAC can be used to adjust offset in the system when in the ManCal mode.

Note the calibration logic should not be in the automatic mode, because the FDAC circuitry is not "aware" that the Coarse DAC is not active, and thus could cause errors if left operating automatically. Therefore, it is recommended that either CAL Hold or Manual CAL mode be asserted.

The DNL in the Direct PGA Input Mode is shown in Figure 26.

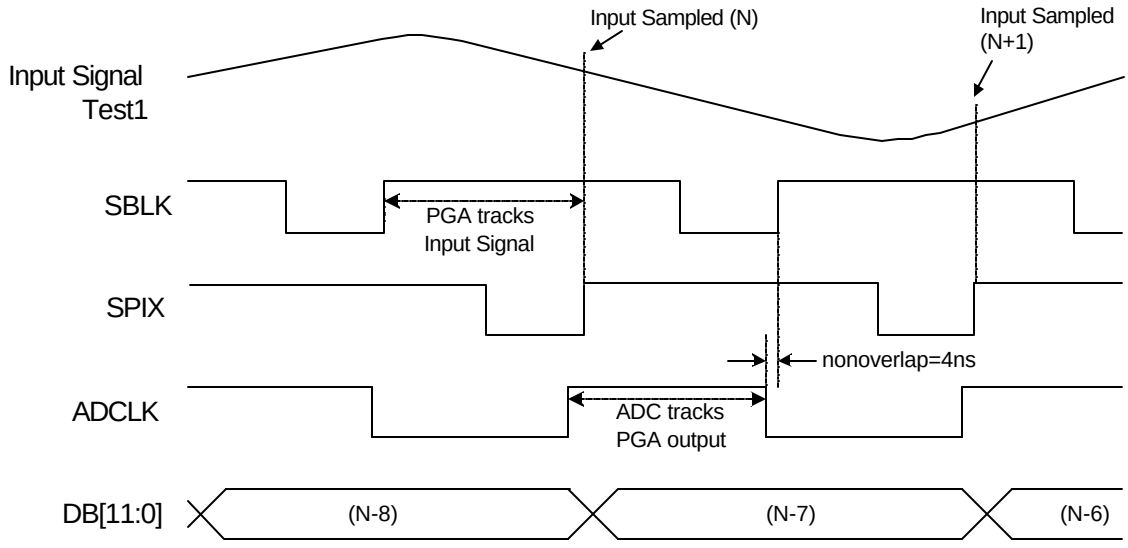


Figure 8. Direct PGA Input Timing (Default Polarities)

ANALOG TO DIGITAL CONVERTER (ADC)

The analog-to-digital converter is based on pipeline architecture with a built in track & hold input stage. The track & hold and ADC conversion are controlled by the externally supplied ADCLK.

The polarity of the ADCLK is programmable. If ADCpol = low, the track & hold circuit tracks the PGA output while ADCLK is high and holds while ADCLK is low. If ADCpol = high, the track & hold circuit tracks the PGA output while ADCLK is low and holds while ADCLK is high. ADCLK should be a 50% duty cycle clock, and should be synchronized with SBLK such that ADC tracking ends at the same time as the CDS sample black ends. (See Figure 13).

The ADC reference levels, CapP & CapN, are generated from an internal voltage reference. To minimize noise, these pins should have high frequency bypass capacitors to AGND. The value of these bypass capacitors will affect the time required for the reference to charge up and settle after power down mode.

The ADC output bus, DB[11:0] & OVER, has 3-state capability that is controlled by the OE bit of the Control register. The outputs are enabled when the OE bit is high. The outputs are high impedance when the OE bit is low.

Direct ADC Input Mode

The ADC inputs can be accessed directly via the ADCinP & ADCinN pins. To enable the Direct ADC Input mode, write a “1” to the ADCtest bit of the Control register. This will disable the CDS/PGS and connect the ADCinP & ADCinN pins directly to the ADC. The ADC data is valid 6.5 clock cycles after the sampling edge of ADCLK (default is falling edge).

POWER DOWN

The Power Down mode can be activated by forcing the PD pin high, or by writing a “1” to the PwrDwn bit in the Control register. For normal operation, the PD pin must be low and the PwrDwn bit must be “0”. In the Power Down mode, all analog circuits are turned off, the calibration is placed in the Hold mode, and the output bus, (DB[11:0] and OVER) is put in the high impedance mode. All the digital registers retain their values, so the PGA gain, offset, and calibration will return to their previous states. The serial interface pins remain active in the Power Down mode. The PD pin and the PwrDwn bit do not reset any internal registers.

In addition to the PwrDwn bit, there are 4 other power down bits which only turn off portions of the chip. DAC1pd and DAC0pd control the two 8 bit utility DACs. AFEpd controls the CDS & PGA circuits. ADCpd controls the ADC. AFEpd & ADCpd are included for factory test and characterization purposes; they are not intended for use in digital camera applications.

DIGITAL OUTPUT ENABLE CONTROL

The digital output bus, DB[11:0] and OVER, has 3-state capability. When the OE bit in the control register is high, and the OE Pin (#24) is high, the digital output drivers are enabled and active. When the OE bit is low, or the OE Pin is low, the digital output drivers are disabled and the bus is in the high impedance state.

The OE bit and OE Pin only control the digital output drivers; all other circuits on the chip will remain active. The black level calibration can still run properly when the outputs are in the high impedance state.

CHIP RESET

The chip includes a Power-On-Reset function (POR), so when the power supplies are turned on, the chip will always power up with default values in all registers.

There are two methods to force a chip reset. The first is to write a “1” to the RESET bit in the reset register. This will reset the chip, and after a delay of about 10 ns, the reset bit will automatically clear itself. The second reset method is to force the RESET pin high. This will reset the chip until the RESET pin goes low again. The RESET pin has an internal pull down.

BLACK LEVEL OFFSET CALIBRATION

To get the maximum color resolution and dynamic range, the XRD9861 uses a digitally controlled calibration circuit to correct for offset in the CCD signal as well as offset in the CDS, PGA & ADC signal path. This calibration is done while the CCD outputs Optical Black (OB) pixels. In the “Line” timing mode, the OB pixels at the start or end of each scan line are used for calibration.

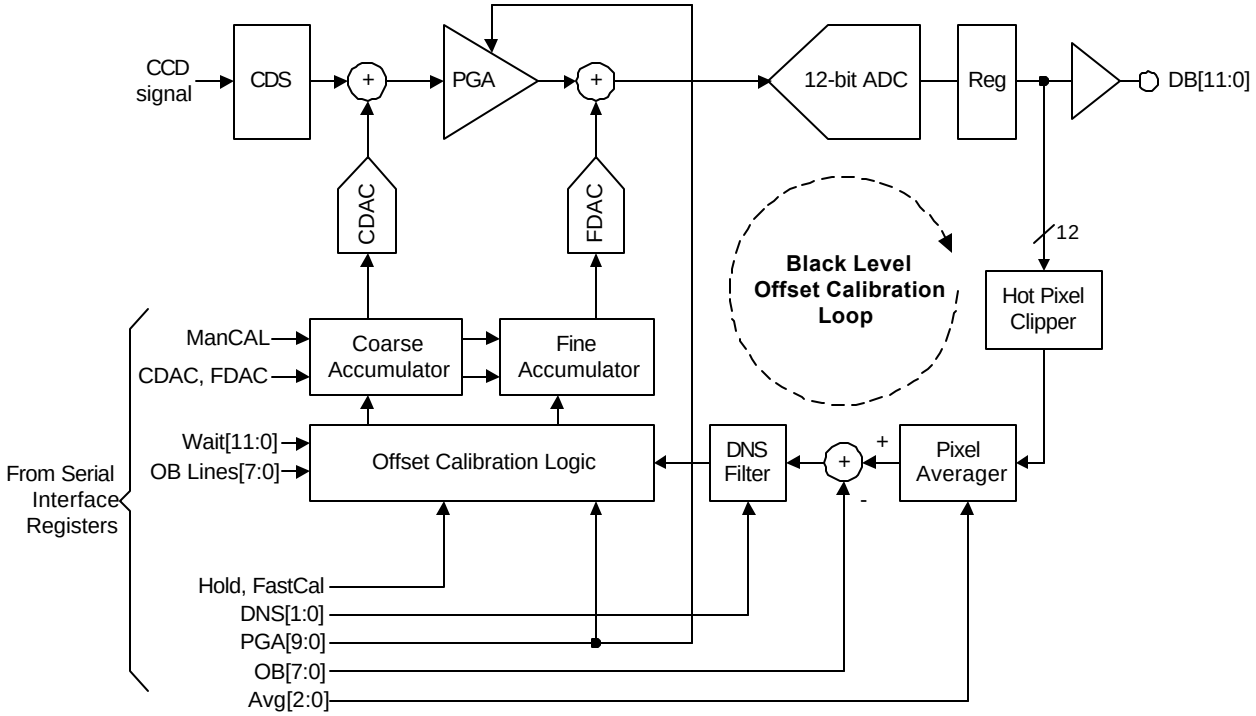


Figure 9. Black Level Offset Calibration Block Diagram

Offset Register										ADC Output
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Black Level (LSB)
X	X	0	0	0	0	0	0	0	0	Do Not Use
X	X	0	0	0	0	0	0	0	1	Do Not Use
X	X	0	0	0	0	0	0	1	0	2 (Minimum offset code)
					. . .					. . .
X	X	1	1	1	1	1	1	1	0	254
X	X	1	1	1	1	1	1	1	1	255

Table 3. Black Level Output Control

Hot Pixel Clipper

CCD's occasionally have hot pixels. These are defective pixels, which always output a bright level. To ensure the Black Level is not affected by hot pixels in the OB area, the Hot Pixel Clipper limits pixel data from the ADC to a maximum value of 511 (1FFh). This clipping only affects the data used by the internal calibration logic. Data on the ADC output bus, DB[11:0], is not clipped.

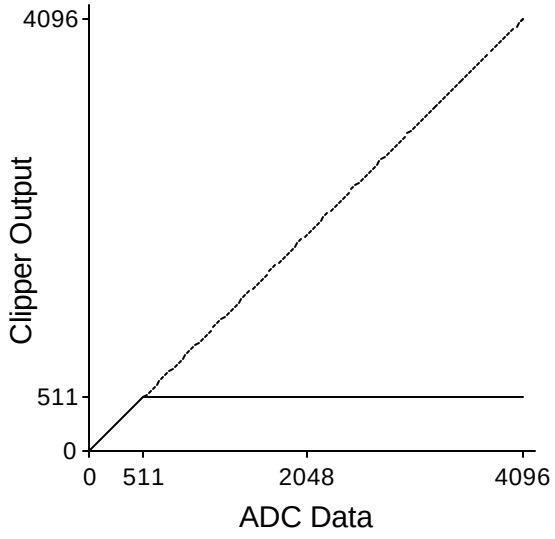


Figure 10. Hot Pixel Clipper

Pixel Averager

After the clipper, the logic takes an average of Optical Black pixels. The number of pixels to be averaged can be selected as one of the following: 4, 8, 16, 32, 64, 128, 256, or 512. The AVG[2:0] bits in the Calibration register are used to program the number of pixels to average. This averaging function filters out noise and prevents image artifacts. The calibration logic will average OB pixels over as many lines as required to get the programmed number of pixels to average.

AVG[2]	AVG[1]	AVG[0]	# of Pixels to Average
0	0	0	4 (Not recommended)
0	0	1	8 (Not recommended)
0	1	0	16 (Not recommended)
0	1	1	32
1	0	0	64
1	0	1	128 (default)
1	1	0	256
1	1	1	512

Table 4. Programming the Pixel Averager

Offset Difference

Next, the Offset register value, OB[7:0], is subtracted from the OB pixel average. If the difference is positive, the offset DACs are adjusted to reduce the effective ADC output code. If the difference is negative, the offset DACs are adjusted to increase the effective ADC output code. The FAST_CAL and DNS options will affect how the DAC adjustments are made.

Coarse & Fine Accumulators

The Coarse and Fine Accumulators are the registers which hold the digital codes for the Coarse and Fine Offset DACs. The Offset DAC adjustments are made by adding or subtracting to the value in the Fine accumulator. If there is an overflow or underflow in the Fine Accumulator, the Fine Accumulator is reset to its mid-scale value, and the Coarse Accumulator is incremented or decremented accordingly.

CALIBRATION OPTIONS

Fast Cal

The purpose of this option is to reduce the amount of time required for initial convergence of the calibration feedback system. The feedback system is designed to have a slow response time to avoid introducing image artifacts. The slow response time is achieved by averaging many OB pixels and by limiting the Fine accumulator changes to ± 1 count at a time (FDAC lsb = ½ ADC lsb). The FastCal option maintains this slow response while the difference between the averaged ADC data and the Offset Code is small, but when the difference is larger than ±128 lsb's, the coarse accumulator takes a step. The actual step size depends on the PGA Gain code, and is set such that the step will cause no more than a 128 LSB change in the ADC output.

To activate the FastCal mode ,write a "1" to the FastCal bit in the Calibration register. By default, the FastCal mode is active.

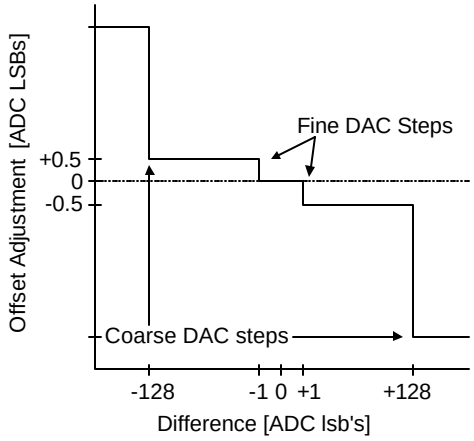


Figure 11. Calibration in FastCal (Speed Up) Mode

Digital Noise Suppression (DNS Filter)

The purpose of this option is to eliminate small changes in the Black Level offset by making the calibration system less sensitive to small changes in the measured offset. In this mode, the user has the option of selecting from three filter settings;see Table 5.

DNS[1]	DNS[0]	DNS Filter Width
0	0	OFF (default)
0	1	Narrow
1	0	Medium
1	1	Wide

Table 5. DNS Threshold Programming

To activate the Digital Noise Suppression mode, write to the DNS[1:0] bits in the Calibration register.By default, the Digital Noise Suppression is ON and set to the wide filter width.

Hold Mode

The purpose of this mode is to prevent any changes in the Fine or Coarse accumulators. This mode is intended to optimize digital still camera applications (DSC). The idea is to first run the calibration normally so the Fine and Coarse accumulators converge on the correct values to achieve the programmed Offset Code. Then, just before acquiring the final image data, activate the Hold mode. This will ensure the black level offset of the CDS/PGA does not change while the final image is being transferred out of the CCD. Once the image has been acquired from the CCD, turn off the Hold mode so the chip can continue to compensate for any changes in offset due to temperature drift or other effects.

To activate the Hold mode, write a "1" to the Hold bit in the Calibration register. By default, the Hold mode is not active.

Manual Mode

The purpose of this mode is to disable the automatic calibration feature. This allows manual adjustment of offset in applications such as digital copiers and high speed scanners. In Manual mode, the Coarse accumulator is programmed by writing to the CDAC register; the Fine accumulator is programmed by writing to the FDAC register. The Coarse accumulator is a 9 bit register. The Fine accumulator is a 10 bit register.

To activate the Manual mode, write a ”1” to the ManCal bit in the Calibration register. By default, the Manual mode is not active.

OB PIXEL CALIBRATION

Line Mode Calibration

In the Line mode, OB pixels are sampled when CAL is active. CAL can be programmed to be active high or active low. Please see the Timing section for more details about clock polarity. Averaging will span as many lines as needed to get the number of OB pixels programmed by AVG[2:0]. Updates to the offset DACs occur during the Optical Black pixel time after a complete iteration. A complete iteration includes the pixel clipping, averaging, calculation of the offset difference, and calculation of the DAC update values. After a complete iteration, the averager is reset, and the logic waits for the number of lines programmed in the “Wait A” & “Wait B” registers (WL[11:0]) before starting the next iteration.

CLOCK BASICS

There are five clock signals: SBLK, SPIX, ADCLK, CLAMP, and CAL.

The pixel rate clocks are SBLK, SPIX, and ADCLK. SBLK controls sampling of the Black reference level for each pixel. SPIX controls sampling of the Video level for each pixel. ADCLK controls the ADC sampling the PGA output.

The line rate clocks are CLAMP & CAL. CLAMP controls the DC restore function for the external AC coupling capacitors. CAL controls the Black level calibration by defining the OB pixels at the start or end of each line. In the One Shot mode (CAL only), CLAMP is used to define the vertical shift period between lines.

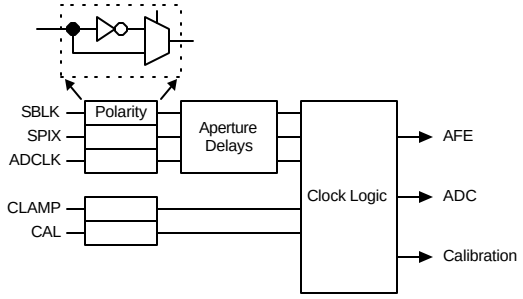
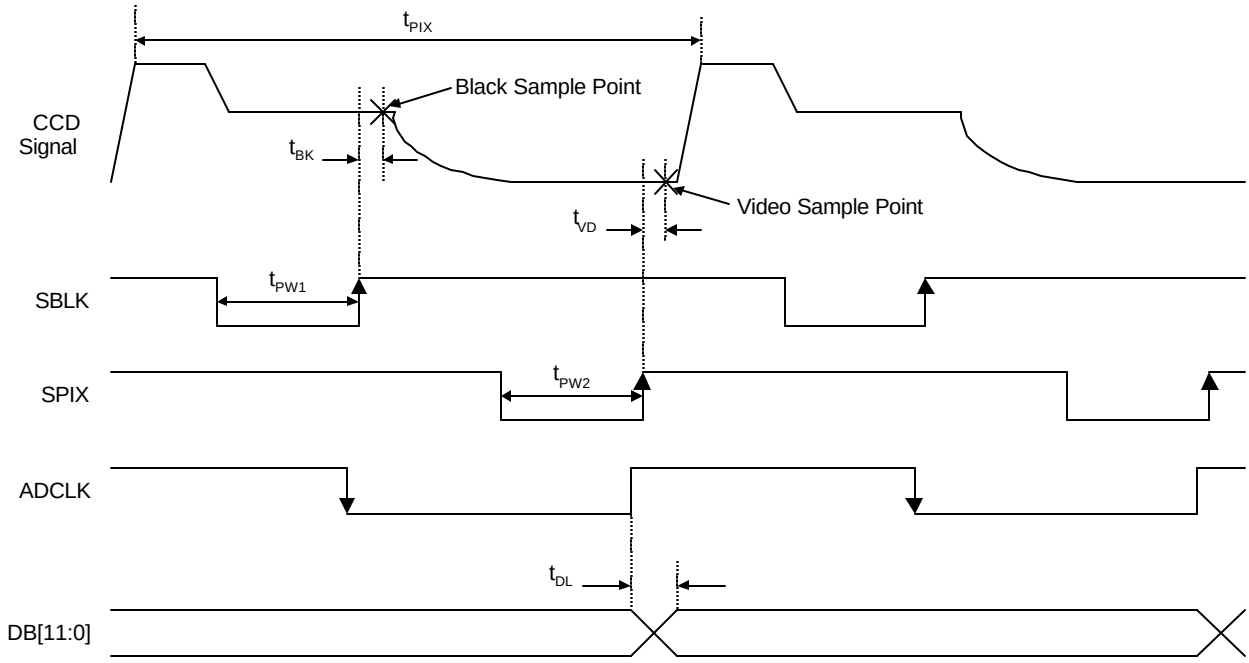


Figure 12. Clock Polarity and Aperture Delays

CLOCK POLARITY

Each of the five clocks has a separate polarity control bit in the Polarity register. If the polarity bit for a clock is low, then the clock is active low. If the polarity bit for a clock is high, then the clock is active high. After reset (by POR, reset bit or reset pin), all clocks default to active low.

PIXEL RATE CLOCKS



Note:

The timing descriptions in this section are correct for the default conditions:
All Polarity bits = 0,
RSTreject = 0 (switch always ON),
SPIXopt = 0

Figure 13. Detailed Pixel Rate Clock Timing for Default Register Settings

SBLK, SPIX & ADCLK

Sampling of the pixel Black Level is controlled by the SBLK pulse. When SBLK is low, the internal sample Black switches in the CDS are ON, sampling the pixel black level on the internal capacitors.

The AFE starts tracking the pixel Video Level, an internal delay, after the rising edge of SBLK. The internal delay is programmed by DelayB[8:6]. The AFE holds the pixel Video Level on the rising edge of SPIX.

The ADC will track the PGA output when ADCLK is high. The ADC will hold the PGA output and start a conversion when ADCLK goes low. The falling edge of ADCLK should happen coincident with, or just before, the rising edge of SBLK. ADCLK should be as close as possible to 50% duty cycle.

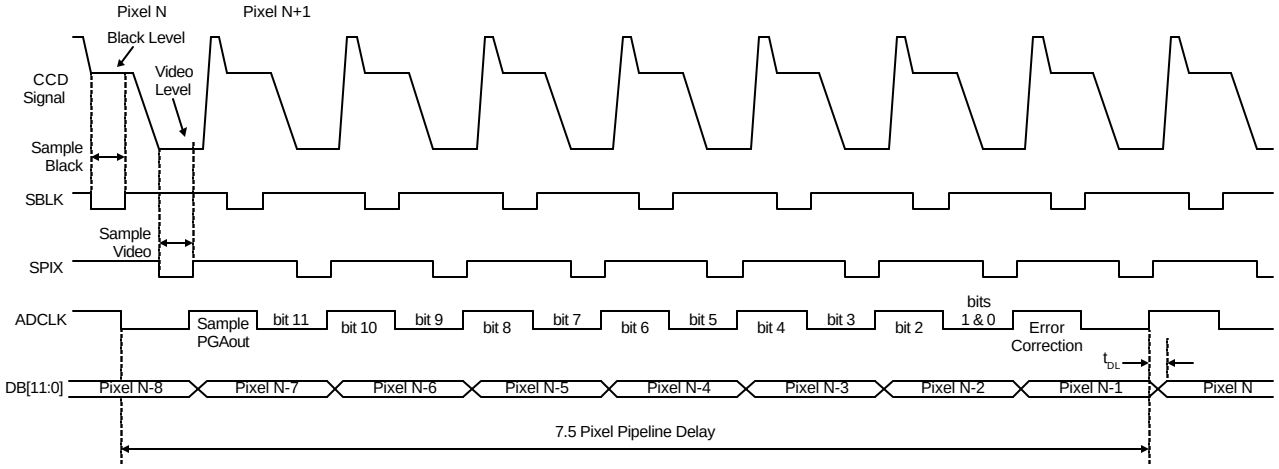


Figure 14. Pixel Timing Showing Pipeline Delay

Pipeline Delay

The digital outputs, DB[11:0] and OVER, are synchronized to ADCLK. When ADCLKpol=0 (default), the digital outputs change on the rising edge of ADCLK. Figure 14 shows the pipeline delay (latency) from sampling a pixel at the CDS input, until the coresponding data is available at the digital output.

SPIXopt

In the default case shown in Figure 15, SPIXopt=0, the internal sample video switches turn ON a programmed delay after the SBLK pulse ends, and turn OFF at the end of the SPIX pulse. The turn ON delay is programmed by DelayB[8:6].

When SPIXopt = 1, the internal SPIX switches are controlled only by the SPIX pulse. This mode is intended for camera systems where the designer has the ability to externally fine tune both the rising and falling edges of SPIX to achieve optimum performance (see Figure 16).

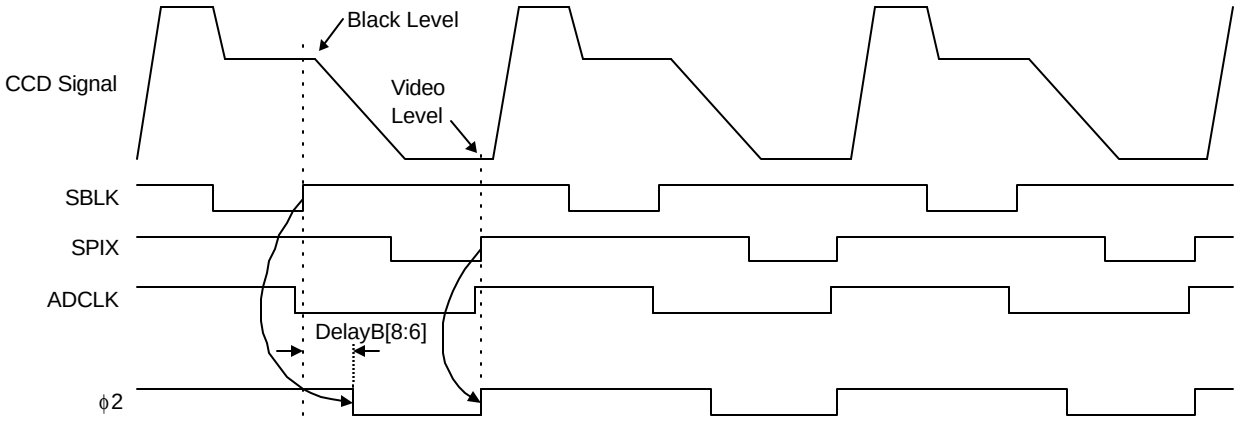


Figure 15. Pixel Rate Clock Timing with SPIXopt=0 (Default)

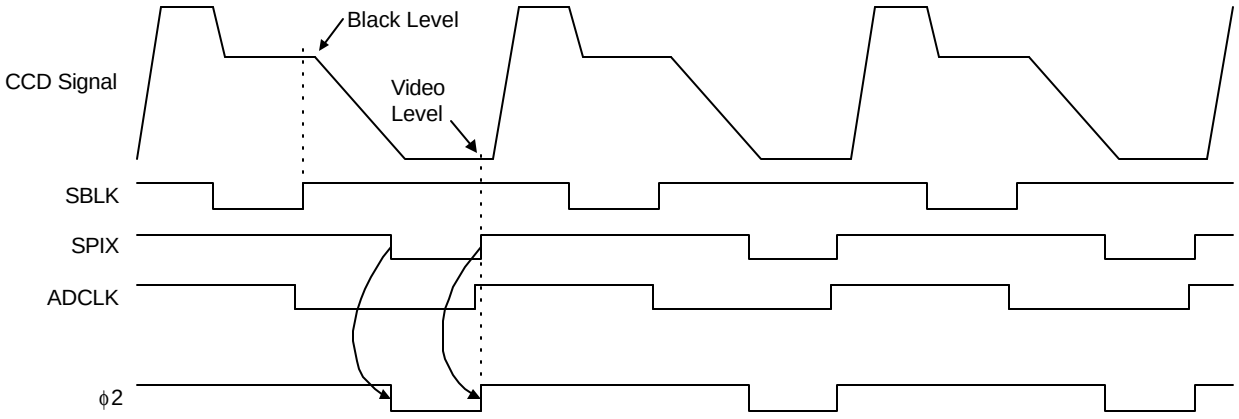


Figure 16. Pixel Rate Clock Timing with SPIXopt=1

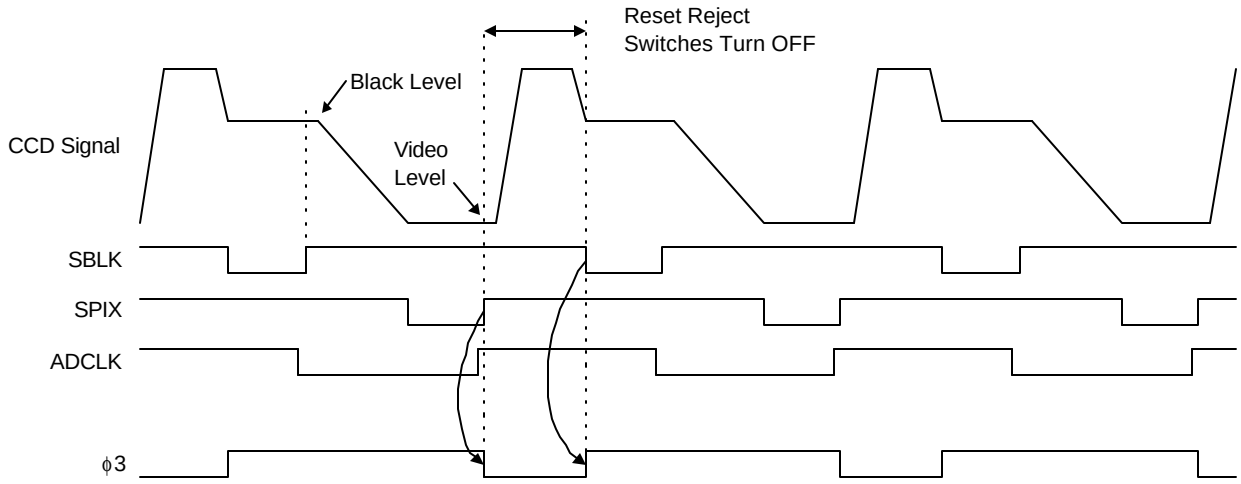


Figure 17. Pixel Rate Clock Timing with RSTreject=1

Reset Reject

In the default state, the reset reject switches (ϕ3) are always ON, they are not clocked. The reset pulse of each pixel is transmitted to the first stage of the PGA. Depending on the PGA gain and the actual voltage level of the reset pulse, this could cause the first stage of the PGA to rail. During the Black Level sampling, the PGA should have enough time to recuperate, but as a precaution, we have included the Reset Reject option.

When RSTreject = 1, the reset reject switches are turned OFF at the end of the SPIX pulse, and turned ON again at the start of the SBLK pulse. This will effectively reject the reset pulse and prevent it from railing the PGA.

Aperture Delays

One of the most difficult tasks in designing a digital camera is optimizing the pixel timing for the CCD, CDS and ADC. We have included the programmable aperture delay function to help simplify this job.

There are two serial interface registers, DelayA & DelayB, used to program the aperture delays. Each register is divided into 3 delay parameters. Each delay parameter is 3 bits wide. Each delay parameter can be set to add from 0ns to 7ns of delay.

The delays are added to the clock signals after the polarity control. This means the definition of leading edge and trailing edge depends on the polarity control bit for each clock. For the default case, SBLKpol=0 & SPIXpol=0, the leading edge is the falling edge and the trailing edge is the rising edge.

DelayA[2:0] controls the delay added to the leading edge of SBLK. This positions the falling edge of internal signal ϕ1.

DelayA[5:3] controls the delay added to the trailing edge of SBLK. This positions the rising edge of internal signal ϕ1.

DelayB[2:0] controls the delay added to the leading edge of ϕ2. This positions the falling edge of internal signal ϕ2.

DelayB[5:3] controls the delay added to the trailing edge of SPIX. This positions the rising edge of internal signal ϕ2.

DelayB[8:6] is only used when SPIXopt=0. It controls the delay from the trailing edge of SBLK to the start of the internal ϕ2 control. This delay is in addition to DelayA[5:3], the SBLK trailing edge delay.

DelayA[8:6] controls the delay added to ADCLK. This is a simple delay. It adds the same delay to both the rising and falling edges of ADCLK to create ϕ4.

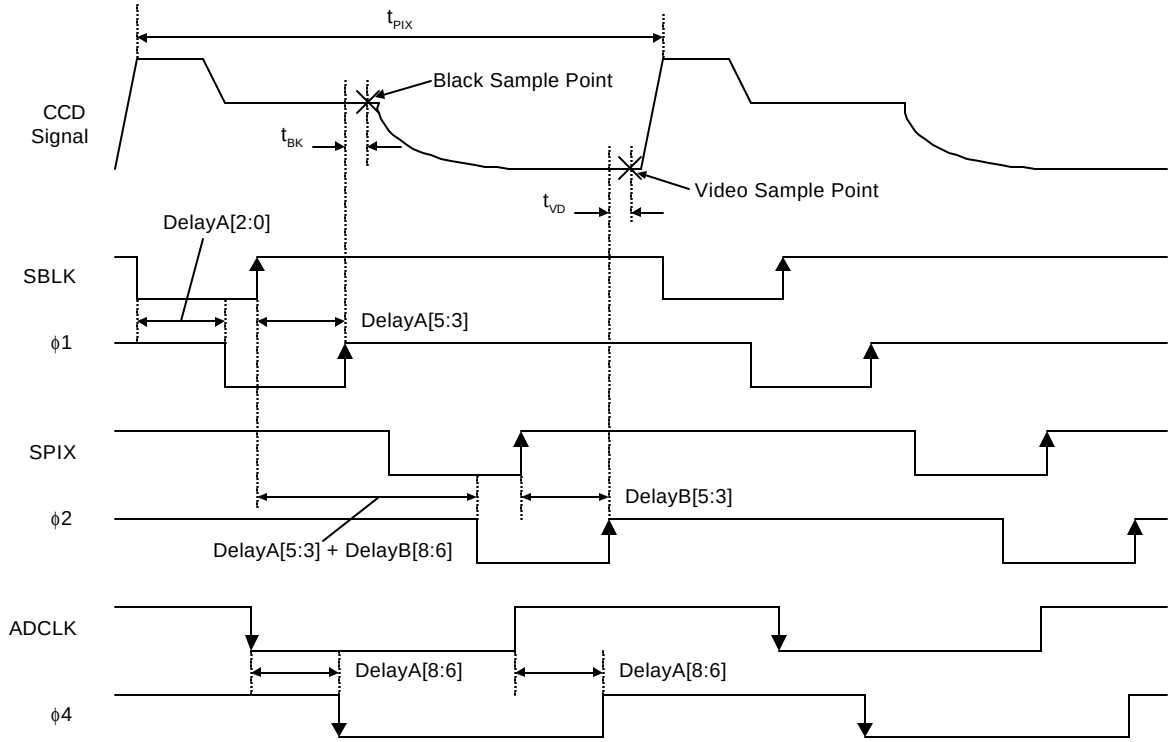


Figure 18. Effects of Aperture Delays with SPIXopt=0 (Default)

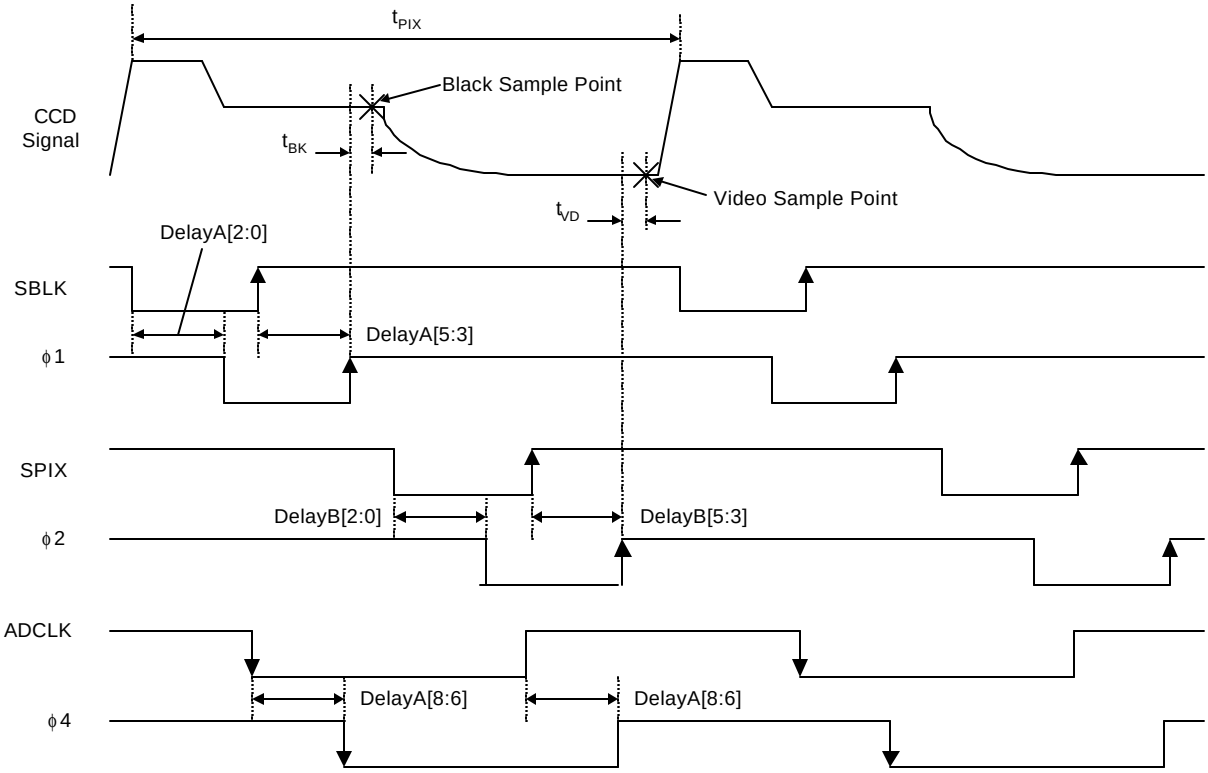


Figure 19. Effects of Aperture Delays with SPIXopt=1

LINE RATE CLOCKS

CLAMP & CAL are the two line rate clock signals. There are two modes of operation for these clocks.

CAL & CLAMP Mode

In this mode, the CLAMP signal is used to activate the DC restore Clamp at the CDS input, and the CAL signal is used to define the Optical Black pixels to be used for the Black Level calibration function. Typically the CLAMP pulse comes during the dummy or optical black pixels at the beginning of each scan line, and the CAL pulse comes during the longer string of optical black pixels at the end of each scan line. CLAMP & CAL must not be active at the same time.

VS Reject Option (CAL & CLAMP Mode)

In the CAL and CLAMP mode, there is an option to disconnect the CDS from the input pins during the Vertical Shift time. To enable this option, write a “1” to the VSreject bit in the Clock register. To properly define the Vertical Shift time, you must set the ClampCal bit properly.

In the typical case, the CCD has a few OB pixels at the beginning of a line (CLAMP time) and a larger number of OB pixels at the end of a scan line (CAL time). In this case set the ClampCal bit = 0. This will define the Vertical shift time as the time from the end of the CAL pulse to the beginning of the CLAMP pulse.

If a CCD has more OB pixels at the beginning of a line, then CAL should be active during these pixels and CLAMP should be active at the end of the line. In this case, set the ClampCal bit = 1. This will define the Vertical shift time as the time from the end of the CLAMP pulse to the beginning of the CAL pulse.

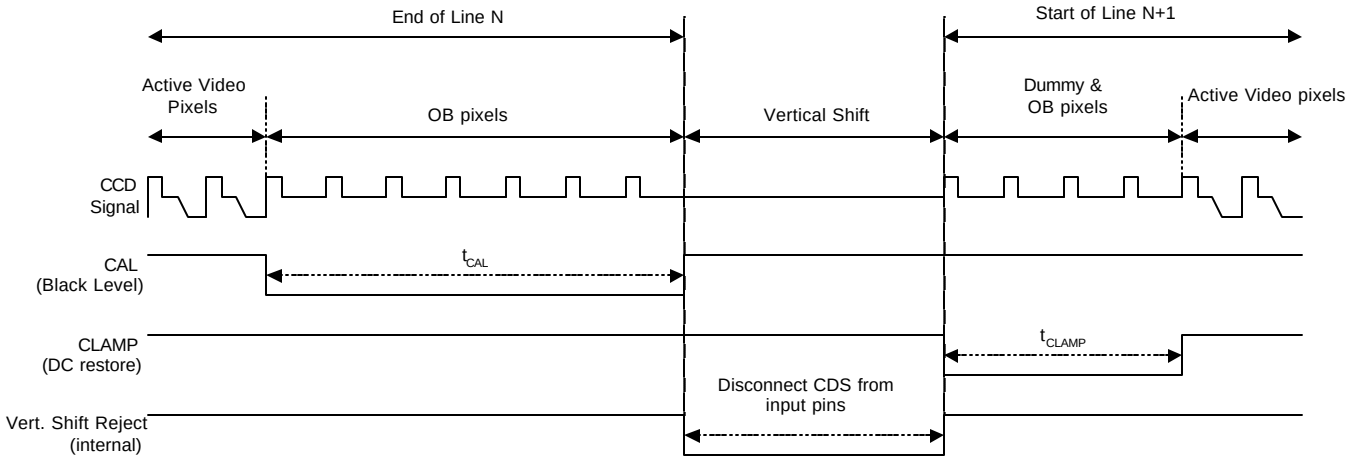


Figure 20. Line Rate Timing with OneShot=0, VSreject=1 & ClampCal=0

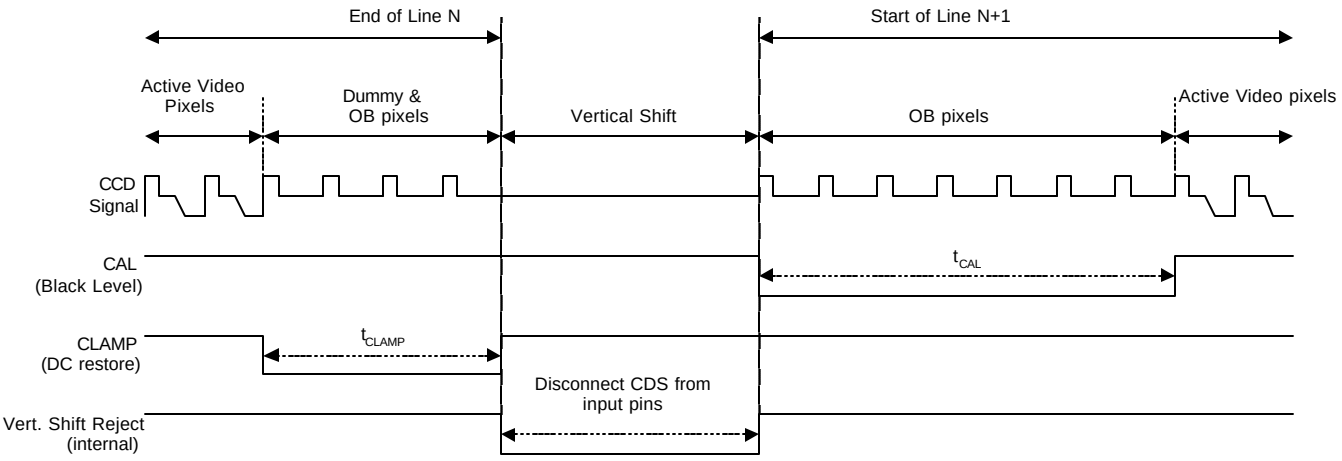


Figure 21. Line Rate Timing with OneShot=0, VSreject=1 & ClampCal=1

One Shot (CAL Only) Mode

In this mode, the CAL signal is used to activate the DC restore clamp and to define the optical black pixels for calibration. The CAL pulse should frame the longest group of OB pixels at either the end or beginning of each line. The DC restore Clamp switch is turned ON during the first four pixels of each CAL pulse. The remaining pixels under the CAL pulse are used for black level calibration.

VS Reject Option (One Shot mode)

The One Shot mode also has an option to disconnect the CDS from the input pins during the Vertical Shift time. To enable this option, write a “1” to the VSreject bit in the Clock register. The signal at the CLAMP pin is used to define the Vertical Shift period (i.e. the time when the CDS is disconnected from the input pins).

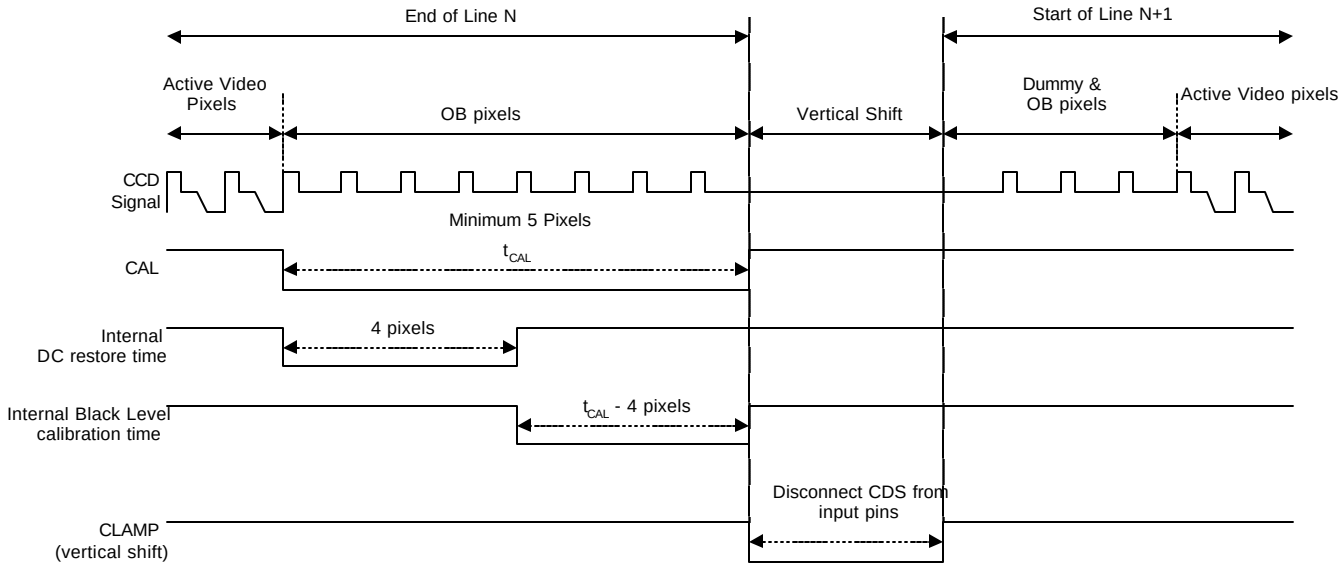


Figure 22. Line Rate Timing with OneShot=1 & VSreject=1

SETTING POWER AND PERFORMANCE WITH Rext

The power and performance levels of the XRD98L61 are set by the value of Rext. Rext sets the current bias level for the entire chip. Rext is connected between pin 39 (ExtRef) and analog ground (see Figure 23). This resistor should be placed as close as possible to the pin and routed directly to a ground plane in a PCB layout. A surface mount carbon resistor is recommended.

Increasing values of Rext decrease the power, linearity and noise performance of the XRD98L61. Lowering the value of Rext increases linearity and noise performance while increasing power. The tested default value for Rext is 30KOhms.

In order to match system to system performance and set consistent manufacturable performance levels between cameras, it is recommended that the Rext resistor have <1% tolerance.

Digital-to-Analog Converters

There are two voltage output, 8-bit resolution, Digital-to-Analog Converters (DACs) which can be used for a variety of purposes, and are controlled via the serial interface. On power up, these DACs are disabled. To activate them, you must write a "0" to the DAC0pd and DAC1pd bits in the Control register.

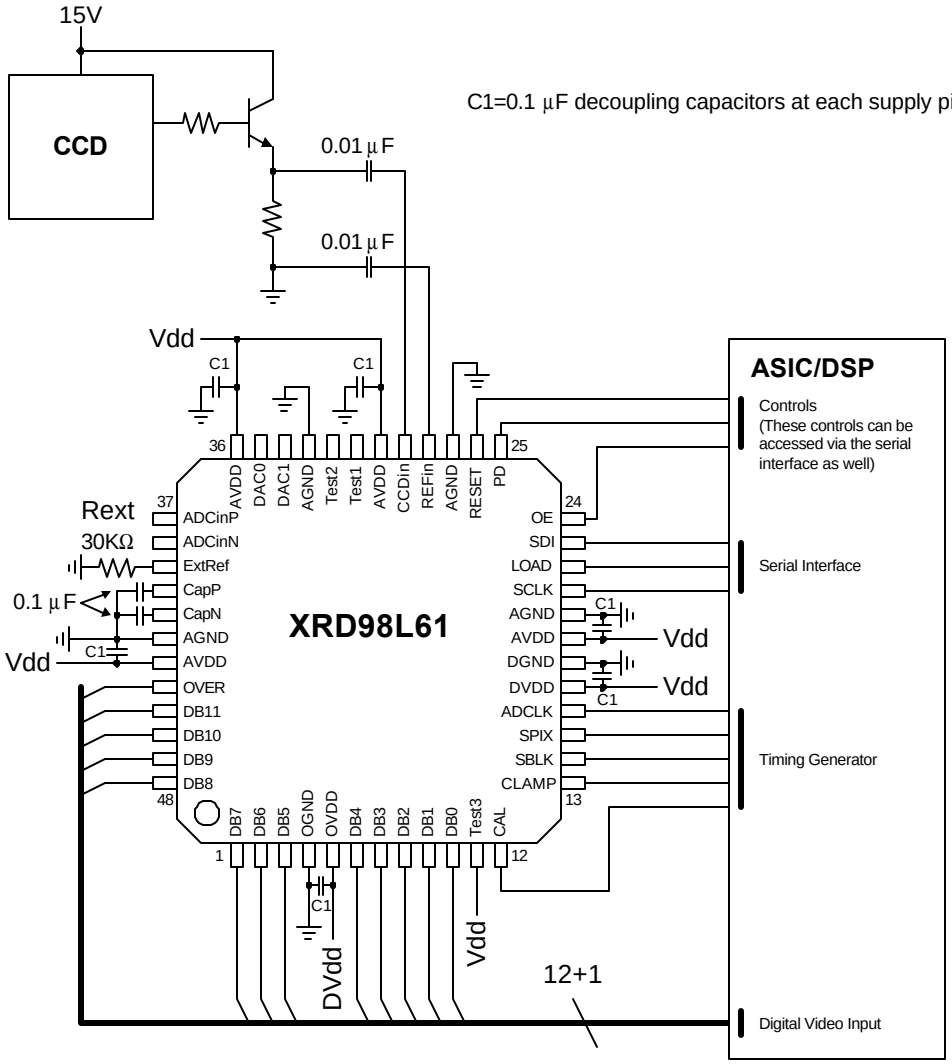


Figure 23. Typical Application Schematic

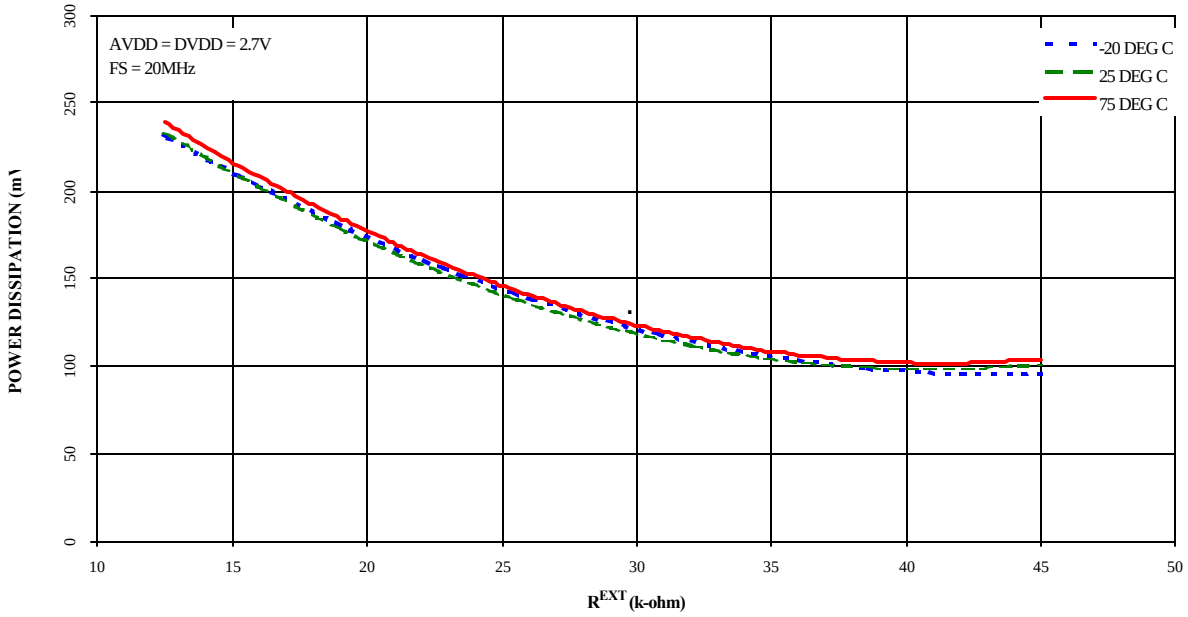


Figure 24. XRD98L61 Power Dissipation vs R_{EXT} @ 20MHz

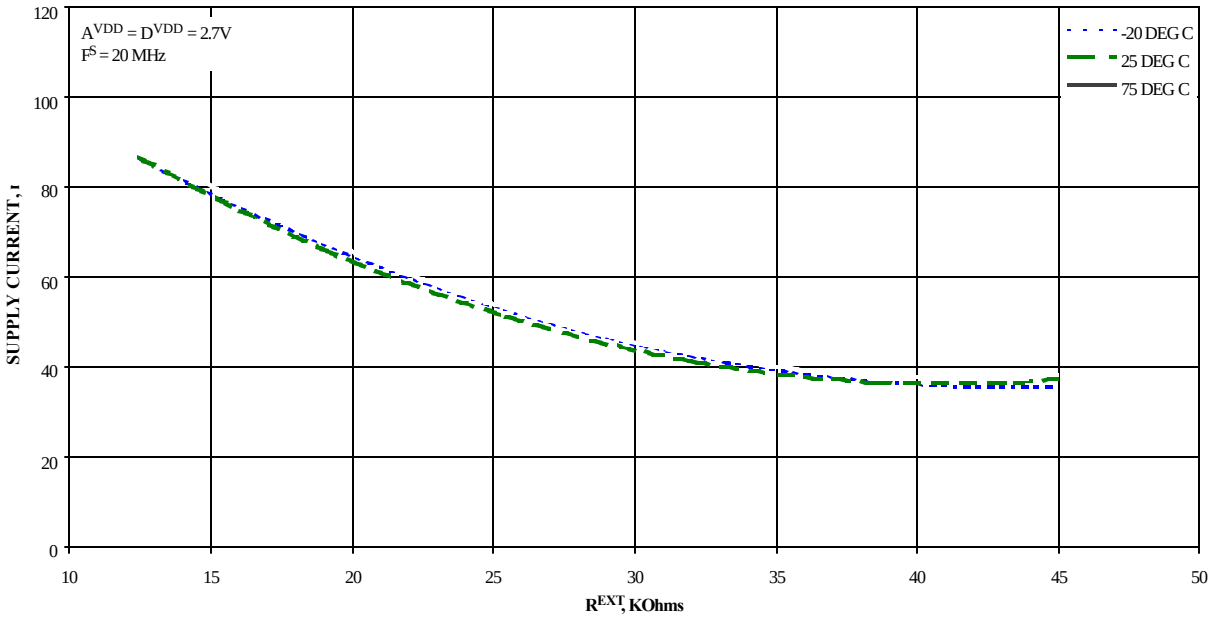


Figure 25. XRD98L61 Supply Current vs R_{EXT} @ 20MHz

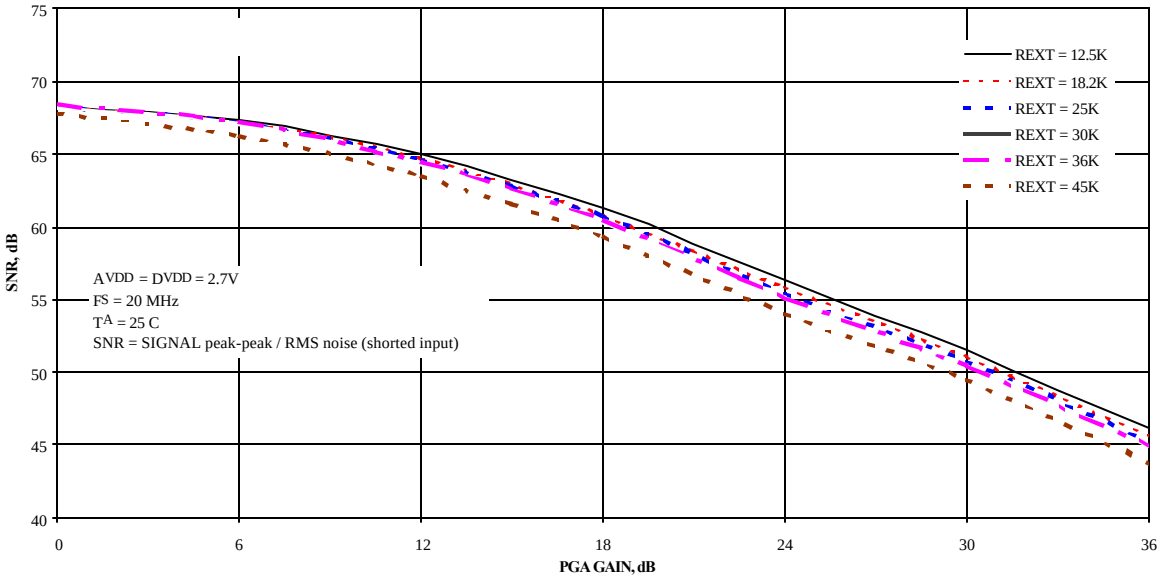


Figure 26. XRD98L61 SNR vs PGA Gain @ 20MHz with Different R_{EXT}

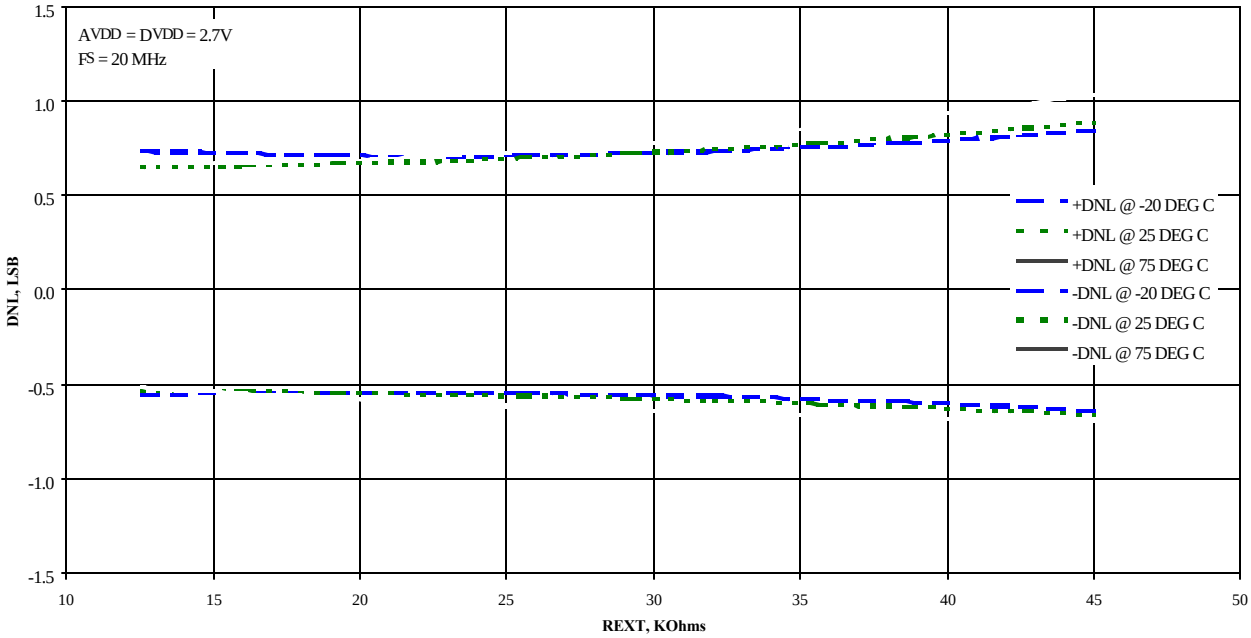


Figure 25. XRD98L61 System DNL vs R_{EXT} @ 20MHz

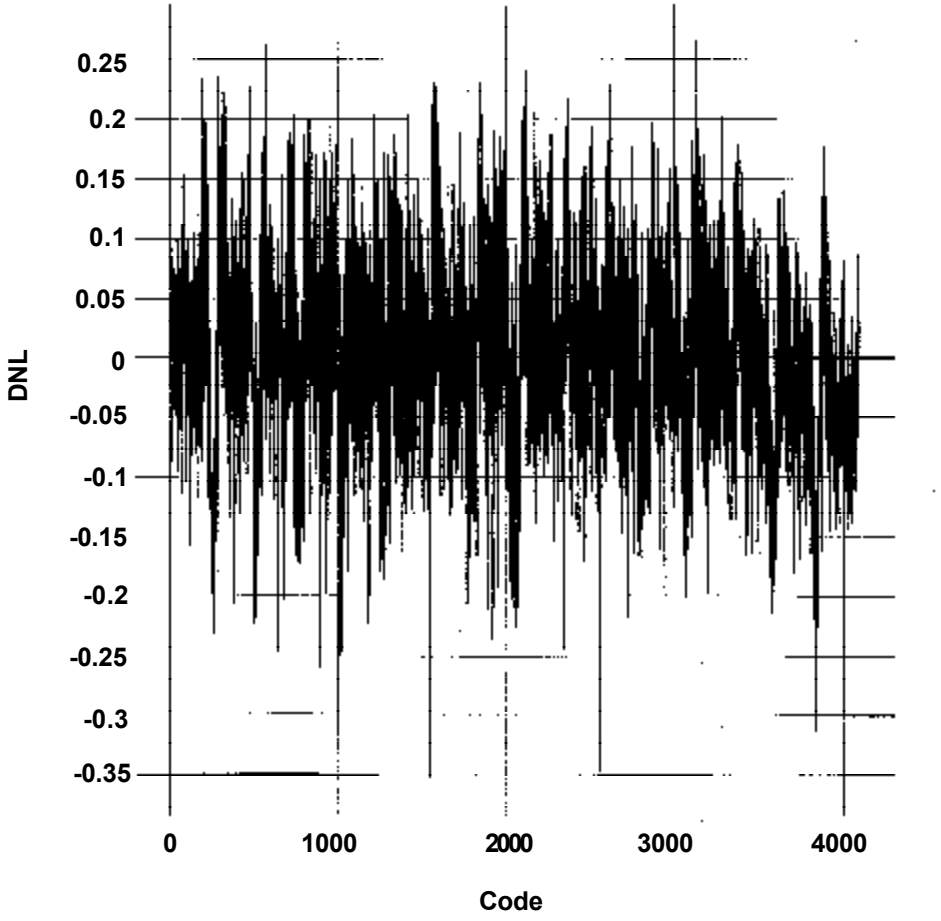
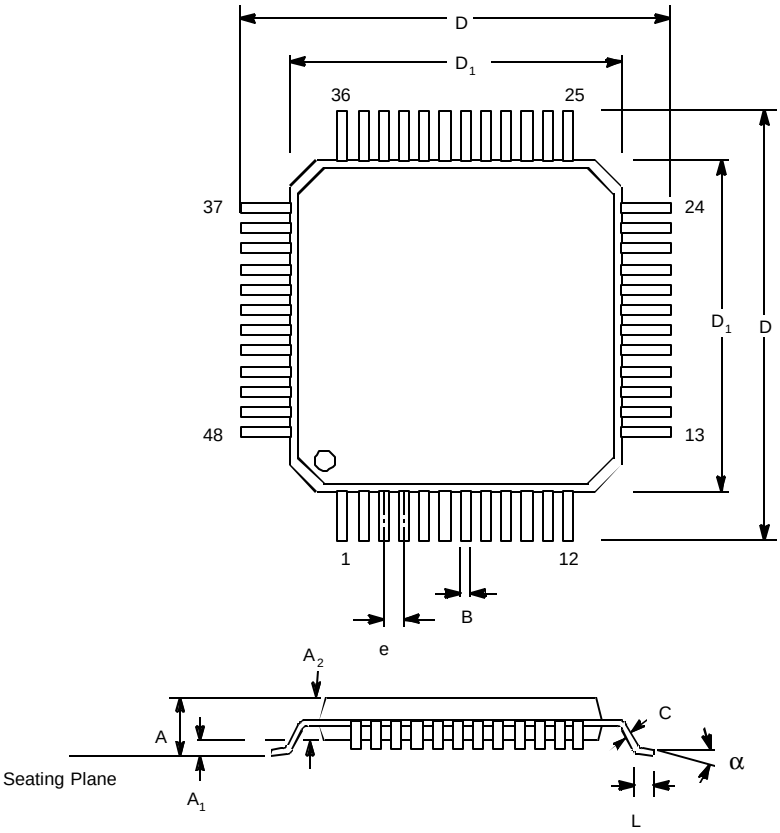


Figure 26. Direct PGA Input DNL

48 LEAD THIN QUAD FLAT PACK

(7 x 7 x 1.4 mm TQFP)

REV. 2.00



	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.055	0.063	1.4	1.6
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.2
D	0.346	0.362	8.8	9.2
D_1	0.272	0.28	6.9	7.1
e	0.020 BSC		0.50 BSC	
L	0.018	0.03	0.45	0.75
a	0°	7°	0°	7°

Note: *The control dimension is the millimeter column*

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