FUJITSU SEMICONDUCTOR
DATA SHEET

DS06-20211-1E

Semicustom

CMOS

Standard Cell

CS201 Series

■ DESCRIPTION

The CS201 series of 65 nm standard cells is a line of CMOS ASICs that satisfy demands for lower power consumption and higher integration. These cells offer the minimum level of leakage current in the semiconductor industry, and are able to implement a mixture of core transistors with three different threshold voltages, as appropriate for the applications ranging from handheld terminals to digital audiovisual equipment.

The integration level in this series is twice the previous series with lower power consumption.

■ FEATURES

- Technology : 65 nm Si gate CMOS
  : 6 to 12 layers of metal wiring.
  Ultra Low-K (low permittivity) material is used for dielectric inter-layers.
  Three different types of core transistors (low leak, standard and high speed) can be used on the same chip.
- Power supply voltage : Supports a wide range from + 0.9 V to + 1.3 V
- Operation junction temperature : − 40 °C to + 125 °C (standard)
- Gate delay time : 11 ps (1.2 V, Inverter, F/O = 1)
- Gate power consumption : 1.77 nW/gate (operating condition: 1.2 V, operating rate 0.5, 1 MHz)
- Reduced chip size achieved by creating the wire bonding pads within the I/O macro regions.
- Support various cell sets (from low power versions to high speed versions)
- Compiled cell (RAM, ROM, others)
- Support large capacity memory “1T-SRAM-Q®”*1
  “1T-SRAM-Q®” is the embedded memory which enable maximum 128Mbit.
- Support low-consumption technology “ CoolAdjust™ ”*2
- Support ultra high speed (up to 10 Gbps) interface macros
- Special interfaces (LVDS, SSTL, others)
- Short-term development using a physical prototyping tool
- One pass design using a physical synthesis tool
- Hierarchical design environment for supporting large-scale circuits
- Support Signal Integrity, EMI noise reduction
- Support static timing sign-off

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- Improve timing convergence by using Statistical Static Timing Analysis (SSTA)
- Design For Manufacturing (DFM) enables stable product-supply and reduced variation
- Optimum package range : FBGA, PBGA, TEBGA, FC-BGA

*1: To realize this memory, the "1T-SRAM-Q ®" technology by MoSys Inc. was used

*2: "CoolAdjust ™" is low power solution presented by Fujitsu.

Note : Some of the features are not available yet.

■ MACRO LIBRARIES (including macros currently being prepared)

1. Logic cells (about 400 types)

Library sets having three different threshold voltages of core transistors.

- Adder
- AND
- AND-OR
- AND-OR Inverter
- Buffer
- Clock Buffer
- Decoder
- Delay Buffer
- ENOR
- EOR
- Inverter
- Latch
- NAND
- NOR
- OR
- OR-AND
- OR-AND Inverter
- SCAN Flip flop
- Non-SCAN Flip Flop
- Multiplexer
- Others

2. IP macros

The following macros will be made available for the CS201 series.

CPU/DSP	ARM™* cores(ARM7/ARM9/ARM11),Peripherals IP
Mixed signal macro	ADC, DAC, OPAMP, others
Compiled macro	SRAM (1 Port, 2 Port), 1 ROM, product sum calculators
Large capacity memory	1T-SRAM-Q®
PLL	Analog PLL

* : ARM is the trademark of ARM Limited.

3. Special I/O interface macro

Interface macro (PHY)	LVDS, SSTL2, SSTL18, PCI, I^2C, others
Interface macro (controller)	USB2.0 Device/host, Serial ATA, PCI-Express, DDR2, HDMI, others

■ COMPILED CELL

Compiled cells are macro cells that can be automatically generated by specifying the bit/word configuration. The following compiled cells are available for the CS201 series (Note that the bit/word ranges for each macro vary depending on the column type).

1. Clock synchronous single-port RAM (1 address : 1 read/write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
2	16 to 160 K	16 to 1 K	1 to 160
4	32 to 640 K	32 to 8 K	1 to 80
8	64 to 640 K	64 to 16 K	1 to 40

2. Clock synchronous dual port RAM (2 address: 2 read/write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
4	64 to 72 K	32 to 1K	2 to 72

3. Clock synchronous ROM

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
16	256 to 1M	128 to 8 K	2 to 128
64	1K to 1M	512 to 32 K	2 to 32

4. Clock synchronous register file (2 address : 1 read, 1 write)

Column type	Memory capacity (bit)	Word range (word)	Bit range (bit)
1	16 to 1152	8	2 to 144
1	32 to 18 K	16 to 128	2 to 144

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{DD}	− 0.5	+ 1.8	V	*2
		− 0.5	+ 2.5 (TBD)		*3
		− 0.5	+ 3.6 (TBD)		*4
		− 0.5	+ 4.6		*5
Input voltage*1	V_I	− 0.5	V_{DD} + 0.5 (≤ 2.5 V)	V	*3
		− 0.5	V_{DD} + 0.5 (≤ 3.6 V)		*4
		− 0.5	V_{DD} + 0.5 (≤ 4.6 V)		*5
Output voltage*1	V_O	− 0.5	V_{DD} + 0.5 (≤ 2.5 V)	V	*3
		− 0.5	V_{DD} + 0.5 (≤ 3.6 V)		*4
		− 0.5	V_{DD} + 0.5 (≤ 4.6 V)		*5
Storage temperature	T_{ST}	− 55	+ 125	°C	
Operation junction temperature	Tj	− 40	+ 125	°C	
Output current*6	I_O	—	15	mA	
Power supply pin current	I_D	—	40	mA	

*1 : V_{SS} = 0 V

*2 : Internal gates

*3 : 1.8 V interface on dual-power supply system

*4 : 2.5 V interface on dual-power supply system

*5 : 3.3 V interface on dual-power supply system

*6 : The output current varies depending on the number of wiring layers in the chip and the wiring configuration of the I/O cells. Contact your Fujitsu representative for details.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

• Dual power supply (under planning)

(V_{DDE} = 1.8 V ± 0.15 V, V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V)

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DDE}	1.65	1.8	1.95	V
		V_{DDI}	0.9	1.0	1.1	V
			1.1	1.2	1.3	V
H level input voltage	1.8 V CMOS Normal	V_{IH}	$V_{DDE} \times 0.65$	—	$V_{DDE} + 0.3$	V
	1.8 V CMOS Schmitt		$V_{DDE} \times 0.70$	—	$V_{DDE} + 0.3$	V
L level input voltage	1.8 V CMOS Normal	V_{IL}	− 0.3	—	$V_{DDE} \times 0.35$	V
	1.8 V CMOS Schmitt		− 0.3	—	$V_{DDE} \times 0.30$	V
Schmitt hysteresis voltage		V_H	$V_{DDE} \times 0.10$	—	$V_{DDE} \times 0.40$	V
Operation junction temperature		Tj	− 40	—	+ 125	°C

• Dual power supply (under planning)

(V_{DDE} = 2.5 V ± 0.2 V, V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V)

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DDE}	2.3	2.5	2.7	V
		V_{DDI}	0.9	1.0	1.1	V
			1.1	1.2	1.3	V
H level input voltage	2.5 V CMOS Normal	V_{IH}	1.7	—	$V_{DDE} + 0.3$	V
	2.5 V CMOS Schmitt		1.7	—	$V_{DDE} + 0.3$	V
L level input voltage	2.5 V CMOS Normal	V_{IL}	− 0.3	—	+ 0.7	V
	2.5 V CMOS Schmitt		− 0.3	—	+ 0.7	V
Schmitt hysteresis voltage		V_H	0.2	—	1.0	V
Operation junction temperature		Tj	− 40	—	+ 125	°C

• **Dual power supply**

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V)

(V_{SS} = 0 V)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Power supply voltage		V_{DDE}	3.0	3.3	3.6	V
		V_{DDI}	0.9	1.0	1.1	V
			1.1	1.2	1.3	V
H level input voltage	3.3 V CMOS Normal	V_{IH}	2.0	—	V_{DDE} + 0.3	V
	3.3 V CMOS Schmitt		2.1	—	V_{DDE} + 0.3	V
L level input voltage	3.3 V CMOS Normal	V_{IL}	− 0.3	—	+ 0.8	V
	3.3 V CMOS Schmitt		− 0.3	—	+ 0.7	V
Schmitt hysteresis voltage		V_H	0.2	—	1.4	V
Operation junction temperature		Tj	− 40	—	+ 125	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

• Dual power supply (under planning)

(V_{DDE} = 1.8 V ± 0.15 V, V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V)

(V_{DDE} = 1.8 V ± 0.15 V, V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V, V_{SS} = 0 V, Tj = − 40 °C to + 125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
H level output voltage	V_{OH}	1.8 V output I_{OH} = − 100 µA	V_{DDE} − 0.2	—	V_{DDE}	V
L level output voltage	V_{OL}	1.8 V output I_{OL} = 100 µA	0	—	0.2	V
Input leakage current	I_L	—	—	—	—	µA
Pull-up/Pull-down resistor	Rp	Pull-up V_{IL} = 0 V Pull-down V_{IH} = V_{DDE}	—	18	—	kΩ

• Dual power supply (under planning)

(V_{DDE} = 2.5 V ± 0.2 V, V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V)

(V_{DDE} = 2.5 V ± 0.2 V, V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V, V_{SS} = 0 V, Tj = − 40 °C to + 125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
H level output voltage	V_{OH}	2.5 V output I_{OH} = − 100 µA	V_{DDE} − 0.2	—	V_{DDE}	V
L level output voltage	V_{OL}	2.5 V output I_{OL} = 100 µA	0	—	0.2	V
Input leakage current	I_L	—	—	—	—	µA
Pull-up/Pull-down resistor	Rp	Pull-up V_{IL} = 0 V/ Pull-down V_{IH} = V_{DDE}	—	25	—	kΩ

• Dual power supply

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V)

(V_{DDE} = 3.3 V ± 0.3 V, V_{DDI} = 1.0 V ± 0.1 V/V_{DDI} = 1.2 V ± 0.1 V, V_{SS} = 0 V, Tj = − 40 °C to + 125 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
H level output voltage	V_{OH}	3.3 V output I_{OH} = − 100 µA	V_{DDE} − 0.2	—	V_{DDE}	V
L level output voltage	V_{OL}	3.3 V output I_{OL} = 100 µA	0	—	0.2	V
Input leakage current	I_L	—	− 10	—	+ 10	µA
Pull-up/Pull-down resistor	Rp	Pull-up V_{IL} = 0 V/ Pull-down V_{IH} = V_{DDE}	15	33	70	kΩ

■ DESIGN METHODS

Fujitsu's Reference Design Flow provides the following functions that help reduce the development time of large scale, high quality LSIs.

- Statistical Static Timing Analysis (SSTA) improves timing convergence.
- Physical Prototyping enables more accurate estimation of highly reliable designs.
- Layout synthesis with optimized timing is realized by Physical Synthesis Tool.
- High accuracy design environment considers drop in power supply voltage, signal noise, delay penalty and crosstalk.
- I/O design environment (power line design, assignment and selection of I/Os, package selection) considers noise.

■ PACKAGES

The CS201 series can use the same packages that were available for the previous series, allowing a smooth transition from previously developed models.

For details of delivery time, contact Fujitsu.

- FBGA packages
- PBGA packages
- TEBGA packages
- FC-BGA packages

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