YAMAHA LSI

YAC520

HGVC1

High Grade Volume Control

■ Outline

YAC520(HGVC1) is a high grade stereophonic digital volume for high end audio system.
It provides wide dynamic range and low distortion as well, and can control individual channels in 256 steps with 0.5 dB per step. The use of 16 bit serial data interface allows daisy chain connection of several devices for multi channel system.
Zero Crossing Detection function suppresses audible noise at quick change of the volume.
YAC520 operates on a single 5 volt power supply, and it is possible to input signal of up to 7.9Vrms by using three types of connection methods.
Development evaluation board, DMB-HGVC1, equipped with PC interface is available.

■ Features

● Wide volume range	A: +32.0 to – 95.0dB	IN1=IN2	(Input < 2.0Vrms @V_{DD}=5V)
(can be used in three ways)	B: +29.5 to – 97.5dB	IN2=GND	(Input < 2.6Vrms @V_{DD}=5V)
	C: +20.0 to – 107.0dB	IN1=GND	(Input < 7.9Vrms @V_{DD}=5V)
● Adjustment step	adjustable in 256 steps, with 0.5dB per step		
● Gain Error	± 0.1dB		
● Low distortion factor	0.001% (input=150 mVrms, gain=+16dB)		
● Low residual noise	1 μVrms (gain=-∞)		

■ Others

Process	CMOS process
Package	20 SSOP (YAC520-E)
Power supply voltage	5 V
Operating temperature	0 to +70 ºC
Power consumption	100 mW @V_{DD}=5.0 V

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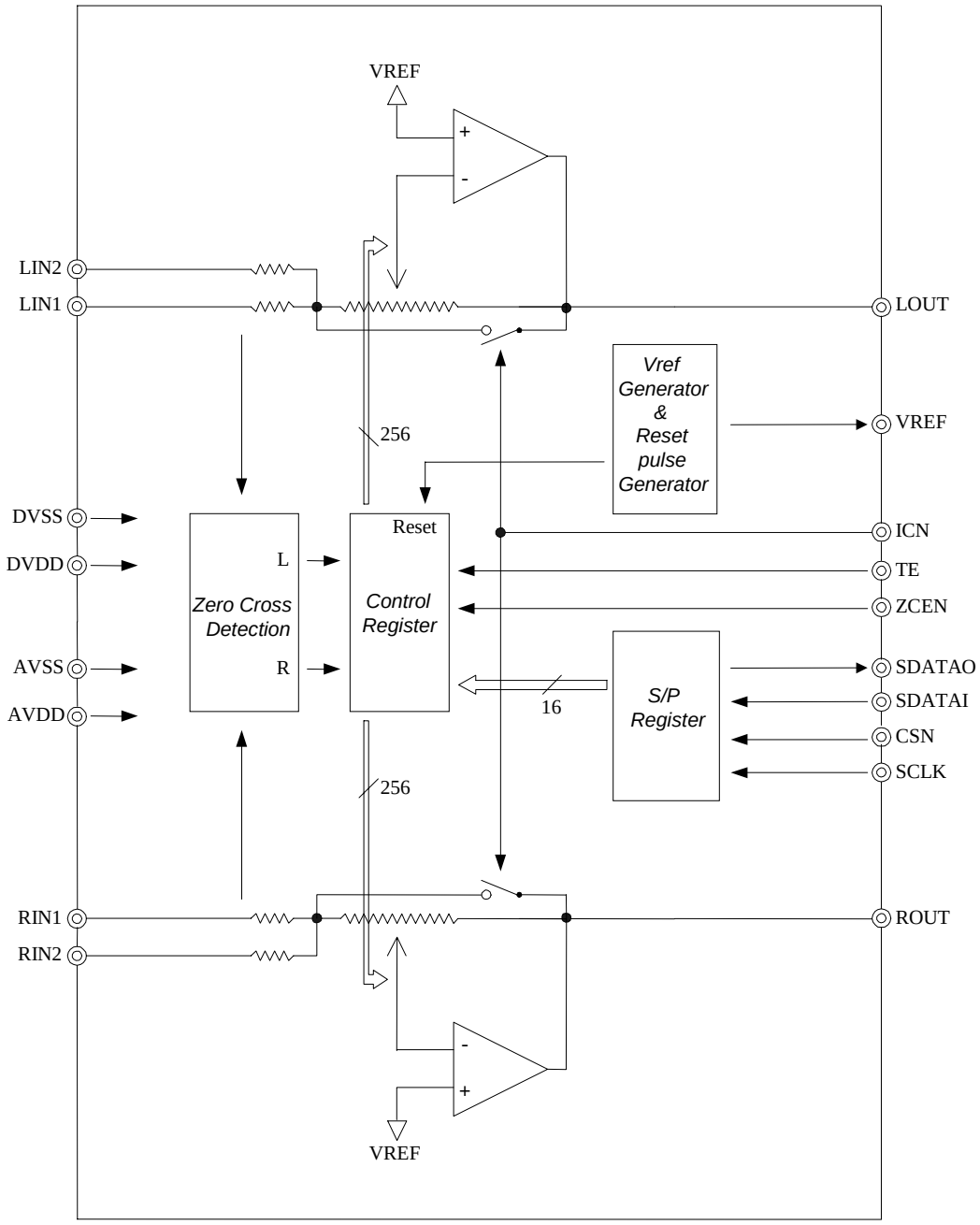
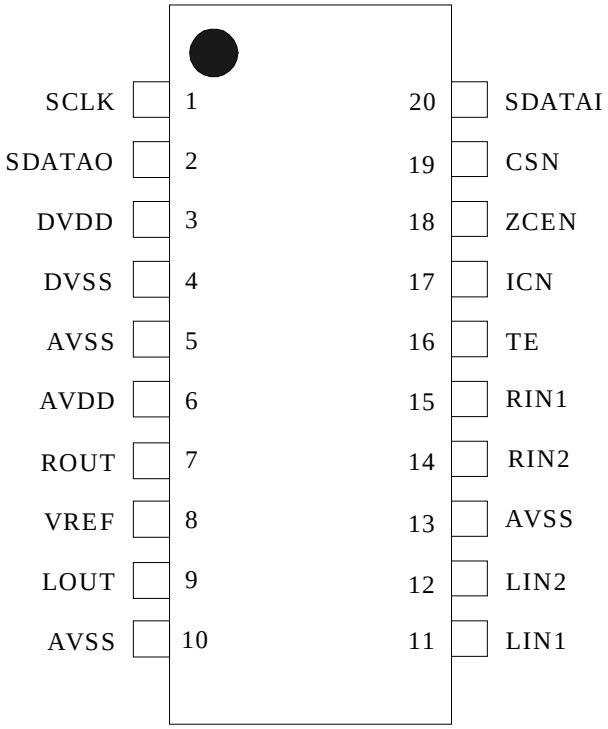
YAC520 CATALOG
CATALOG No.: LSI-4AC520A4
2001.12

■ Block Diagram



■ Pin Assignment



Top View

■ Pin Functions

- **Power supply pins**

AVDD – Analog power supply (+5.0 V)
AVSS – Analog ground
DVDD – Digital power supply (+5.0 V)
DVSS – Digital ground

- **Analog Pins**

LIN1 – Left Channel Analog input 1
Lch analog input pin 1
Gain setting ranges from +32 dB to – 95 dB when the signal inputted to LIN2 is inputted this pin, and gain setting ranges from +20.0 dB to – 107.0 dB when it is grounded through a capacitor.

LIN2 – Left Channel Analog input 2
Lch analog input pin 2
Gain setting ranges from +32 dB to – 95 dB when the signal inputted to LIN1 is inputted this pin, and gain setting ranges from +29.5 dB to – 97.5 dB when it is grounded through a capacitor.

RIN1 – Right Channel Analog input 1
Rch analog input pin 1
Gain setting ranges from +32 dB to – 95 dB when the signal inputted to RIN2 is inputted this pin, and gain setting ranges from +20.0 dB to – 107.0 dB when it is grounded through a capacitor.

RIN2 – Right Channel Analog input 2
Rch analog input pin 2
Gain setting ranges from +32 dB to – 95 dB when the signal inputted to RIN1 is inputted this pin, and gain setting ranges from +29.5 dB to – 97.5 dB when it is grounded through a capacitor.

LOUT – Left Channel Analog output
Lch analog output pin
Note this is an inverted output.

ROUT – Right Channel Analog output
Rch analog output pin
Note this is an inverted output.

VREF – Analog Reference Voltage (output)
Analog reference voltage output pin
Outputs 1/2VDD. Ground through a capacitor of 10 μF or more to attain stabilization.

- **Digital Pins**

SDATAI – Serial Data Input
Serial data input pin

SDATAO – Serial Data Output
Serial data putput pin
Outputs Serial data when CSN is “low”, or becomes high impedance state when it is “high”.

SCLK – Serial Clock (Input)
Serial clock input pin

CSN – Chip Select (Input)
Chip select input pin

ICN – DC Bias Initial Clear (Input)
DC bias initialization pin. DC bias is set to VREF (analog reference voltage) when this is “low”.
To stabilize the bias voltage at power on, determine the control time in accordance with the coupling capacitor that is connected to the inputs (LIN1, LIN2, RIN1 ,RIN2).
(Refer to “VREF stabilization time and DC bias initialization time” in the description of functions.)

ZCEN – Zero Crossing Enable (Input)
Zero crossing control pin. Making this pin “high” enables a mode where volume change is performed after detecting zero crossing.
The volume change immediately after writing data when this pin is “low”.

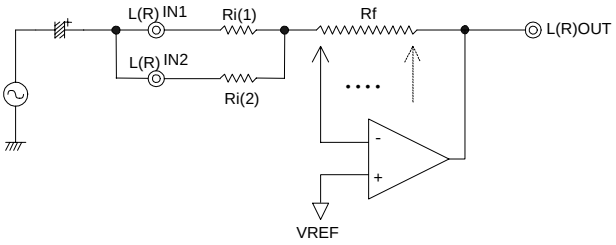
TE – Test Enable (Input)
Test mode control pin. Fix it to “low” or with NC when using.

■ Description of analog functions

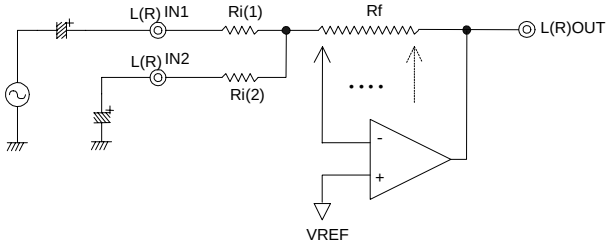
- Maximum input voltage

As described in the following figure, the maximum amplitude of signal that can be inputted varies according the method of the use of L(R) IN1 and 2 pins. The method A makes the maximum amplitude of the input signal approximately 2 Vrms, the method B makes it approximately 2.6 Vrms, and the method C makes it approximately 7.9 Vrms. The use of the method B or C allows to input signal exceeding the power supply voltage.

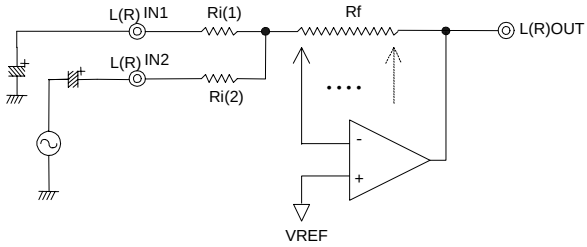
Note that the gain setting range for the method B is reduced by 2.5 dB from the one for the method A, and 12 dB for the method C.



MethodA: IN1=IN2 Gain range (+32 dB to –95 dB)
Maximum input voltage: 2 Vrms



MethodB: IN2=GND Gain range (+29.5 dB to –97.5 dB)
Maximum input voltage: 2.6 Vrms



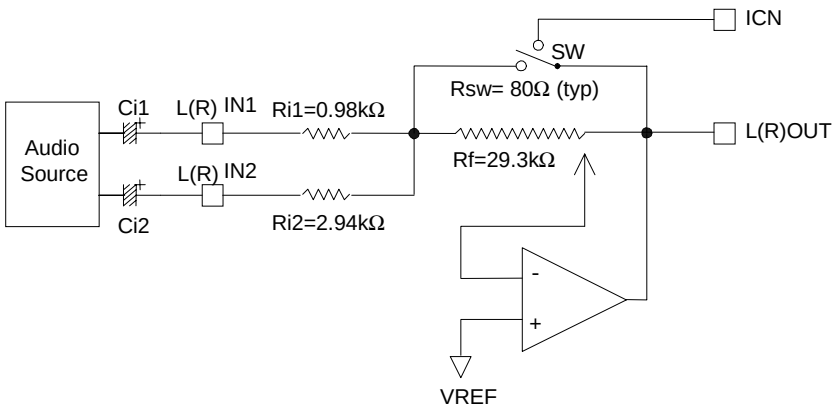
MethodC: IN1=GND Gain range (+20 dB to –107 dB)
Maximum input voltage: 7.9 Vrms

- VREF (analog reference voltage) stabilization time and DC bias initialization time

The time required for stabilization of VREF pin voltage after power on moment varies according to the capacitance of the capacitor connected to VREF pin. Connecting a capacitor of 10 µF makes the time constant 30 ms (typ.). Note that the serial interface becomes invalid in this period, t_{PUP}.

As shown in the following figure, making ICN terminal "low" sets the DC bias forcibly with SW in the LSI.

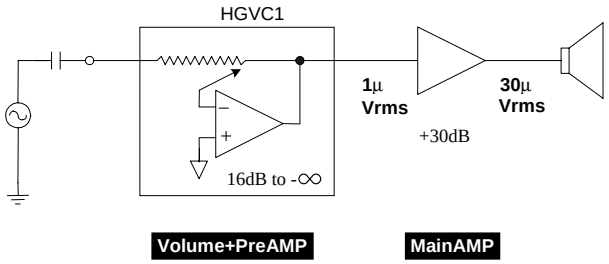
Since the time constant of L(R) IN1 and 2 pins becomes approximately 300 ms (typ.) when a capacitor of 100 µF is used as the coupling capacitors (Ci1, 2), control ICN according to the capacitor that is connected.



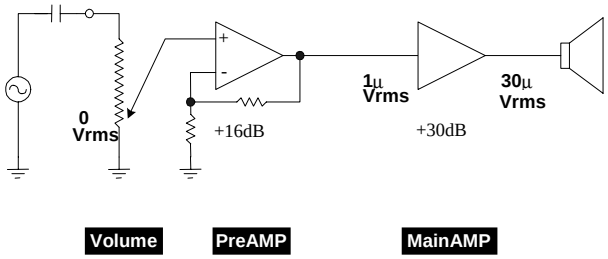
Gain setting after power on = -∞

■ Realization of system with low residual noise

– Configuration that uses HGVC1 –



– Conventional configuration –



General audio amplifiers are designed with the input sensitivity of approximately 150mV, and has gain of approximately 16 dB at PreAMP section, and approximately 30 dB at Power AMP section.

For passive volume, they are given configuration of “Volume”–”PreAMP”–”MainAMP” as shown in the above right figure. System with very small residual noise can be made by giving HGVC1 also the function of “PreAMP” because HGVC1 has the positive side gain (max : 32 dB).

Since the residual noise of HGVC1 (gain=-∞) is 1 μVrms(typ.), the noise level at the speaker end becomes 30 μVrms if the noise of MainAMP is neglected. On the other hand, when conventional configuration is used, the noise at the speaker end becomes very large because the noise produced by the initial stage of PreAMP is amplified approximately by 46 dB (200 times) even if the level of noise produced by the volume section during mute is zero.
To achieve the noise level at the speaker end that is equivalent to the one obtained with configuration using HGVC1, the level of the noise converted to that of input of PreAMP is required to be approximately 0.16 μVrms (-136 dBV), which is very difficult to achieve.

As described above, HGVC1 provides advantage of making the residual noise very small because it has built-in amplifiers.

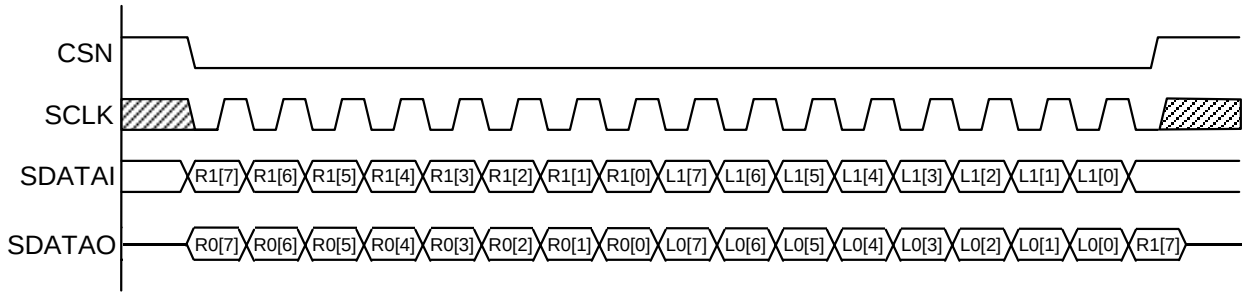
■ Description of digital functions

- Serial data interface

HGVC1 is a simple three wire serial interface. SDATAI is a serial data input pin, SCLK is a serial clock pin, and CSN is a chip select pin for writing volume value. 16 bit serial data is so formatted that SDATAI is inputted in synchronous with rise edge of SCLK when CSN is “low” (MSB first).

Data is latched with the rise edge of CSN, and volume values of both left channel and right channel are set into the register. Serial data is outputted from SDATAO in synchronous with fall edge of SCLK. This data allows control by using daisy chain connection or confirmation of present volume value easily.

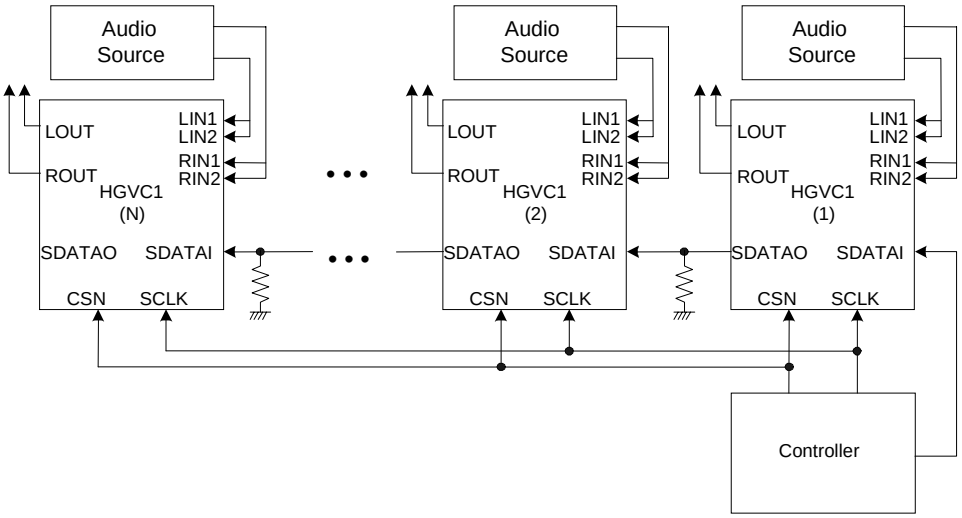
Note that the register value after power on is 0000h (muted state), and thus, the interface becomes valid after the time t_{PUP} elapses.

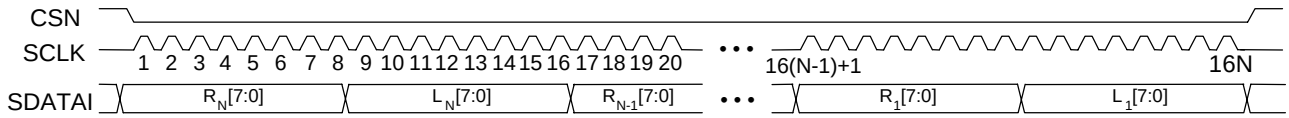


- Daisy Chaining

Since HGVC1 adopts multi channel system, multiple devices can be connected with daisy chain connection. When using the LSI in multi channel system, connection of the first SDATAO pin to the second SDATAI pin, and the second SDATAO pin to the third SDATAI pin allows control of multiple HGVC1s without requiring complex addressing. Volume data is inputted into the S/P(Serial/Parallel) register of the individual HGVC1 by holding CSN “low” for 16 clocks * N (N represents the number of HGVCs in the chain).
As the volume data inputted to the SDATAI of HGVC1(1) is shifted in the internal S/P register by 1 bit per SCLK clock, 16 * N clocks are required to input volume data into S/P registers of all HGVC1(1) to HGVC1(N). Note that the first 16-bit data is inputted to the S/P register of the HGVC1(N).

Finally, by setting CSN “High” after 16 clocks * N period, all data in the S/P registers are written into the Control registers simultaneously to activate new volume data of all HGVC1s in the daisy chain.





• Volume Setting

In zero crossing mode (ZCEN=H), the volume value is changed when one zero crossing is detected after the rise of CSN. The volume value is changed also when no zero crossing is detected for 20 ms. In normal mode (ZCEN=L), zero crossing detection is not performed and volume value is changed immediately after the rise of CSN.

The input codes and volumes values are related as described in the following table.

Input Code (Left/Right Channel)	L(R)IN1=L(R)IN2 Gain or Attenuation (dB)	L(R)IN2=GND Gain or Attenuation (dB)	L(R)IN1=GND Gain or Attenuation (dB)
11111111	+32.0	+29.5	+20.0
11111110	+31.5	+29.0	+19.5
•	•	•	•
•	•	•	•
11010111	+12.0	+9.5	0
•	•	•	•
11000100	+2.5	0	–9.5
•	•	•	•
10111111	0	–2.5	–12.0
•	•	•	•
•	•	•	•
00000010	–94.5	–97.0	–106.5
00000001	–95.0	–97.5	–107.0
00000000	MUTE	MUTE	MUTE

• MUTE

Writing 0000h into register enables mute. The time mute is enabled varies between zero crossing mode (ZCEN=H) and normal mode (ZCEN=L) as described above.

■ Electrical Characteristics

● Absolute maximum ratings

Parameter	Symbol	min.	max.	Unit
Analog Supply Voltage	AV_{DD}	– 0.3	7.0	V
Digital Supply Voltage	DV_{DD}	– 0.3	7.0	V
Analog Input Voltage (A: LIN1=LIN2, RIN1=RIN2) @AV_{DD}=DV_{DD}=5V (B: LIN2=GND, RIN2=GND) (C: LIN1=GND, RIN1=GND)	VIN_A	– – –	2.0 2.6 7.9	Vrms
Digital Input Voltage	VIN_D	– 0.3	DV_{DD}+0.3	V
Storage Temperature	T_{stg}	– 50	125	°C

Note) DVSS = AVSS = 0V

● Recommended operating conditions

Parameter	Symbol	min.	typ.	max.	Unit
Analog Operating Voltage	AV_{DD}	4.75	5.00	5.25	V
Digital Operating Voltage	DV_{DD}	4.75	5.00	5.25	V
Operating Ambient Temperature	T_{OP}	0	25	70	°C

● Analog Characteristics (Conditions: T_{OP} = 25°C, AV_{DD} = DV_{DD} = 5.0V)

Parameter	Symbol	min.	typ.	max.	Unit
Gain Range (A: LIN1=LIN2, RIN1=RIN2) (B: LIN2=GND, RIN2=GND) (C: LIN1=GND, RIN1=GND)	Gain A Gain B Gain C	– 95.0 – 97.5 – 107.0	–	+ 32.0 + 29.5 + 20.0	dB
Step Size		–	0.5	–	dB
Step Error		–	± 0.1	–	dB
Gain Matching Between Channel (1kHz)		–	± 0.1	–	dB
Input Resistance	R_I	0.5	–	40	kΩ
Input Capacitance	C_I	–	–	15	pF
Load Capacitance	C_L	–	–	100	pF
Output Impedance	R_O	–	50	–	Ω
Signal to Noise Ratio (input=150mVrms, gain=+16dB)	SN	–	100	–	dB
Total Harmonic Distortion (input=150mVrms, gain=+16dB)	THD	–	0.001	–	%
Residual Output Noise (-∞, IHF-A)	Vn	–	1	–	μVrms
Inter channel Isolation (1kHz)		–	– 110	–	dB
Output Clipping Voltage (THD < 0.1%, R_L = 10kΩ)		1.5	–	–	Vrms

● Power Supply

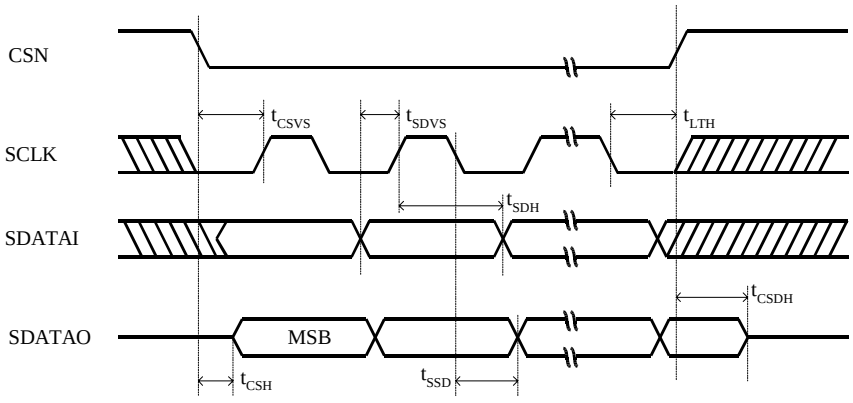
Parameter	Symbol	min.	typ.	max.	Unit
Power Consumption (AV_{DD},DV_{DD}=5V)	P_D	–	100	–	mW

● Digital DC Characteristics

Parameter	Symbol	min.	typ.	max.	Unit
High-Level Input voltage	V_{IH}	0.7xV_{DD}	–	–	V
Low-Level Input voltage	V_{IL}	–	–	0.3xV_{DD}	V
High-Level Output voltage(Io= – 0.2mA)	V_{OH}	V_{DD}–1	–	–	V
Low-Level Output voltage(Io=2mA)	V_{OL}	–	–	0.4	V
Input Leakage Current	I_{LI}	–	–	10	µA

● Digital AC Characteristics

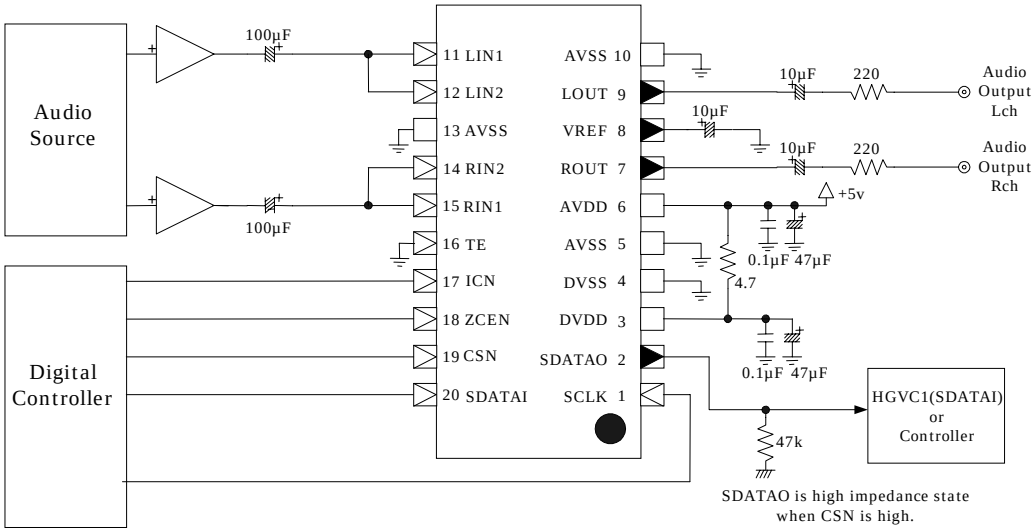
Parameter	Symbol	min.	typ.	max.	Unit
Serial Clock	SCLK	–	–	6.25	MHz
Serial Clock Pulse Width High	t_{PH}	80	–	–	ns
Serial Clock Pulse Width Low	t_{PL}	80	–	–	ns
SDATAI Set Up Time	t_{SDVS}	20	–	–	ns
SDATAI Hold Time	t_{SDH}	20	–	–	ns
CSN Valid to SCLK Rising	t_{CSVS}	30	–	–	ns
SCLK Falling to CSN High	t_{LTH}	35	–	–	ns
CSN low to Output Active (C_L=20 pF)	t_{CSH}	–	–	35	ns
SCLK Falling to Data Valid (C_L=20 pF)	t_{SSD}	–	–	60	ns
CSN High to SDATAO Inactive	t_{CSDH}	–	–	100	ns
Power-up to SPI Operation (C_{VREF}=10µF)	t_{PUP}	–	30	50	ms



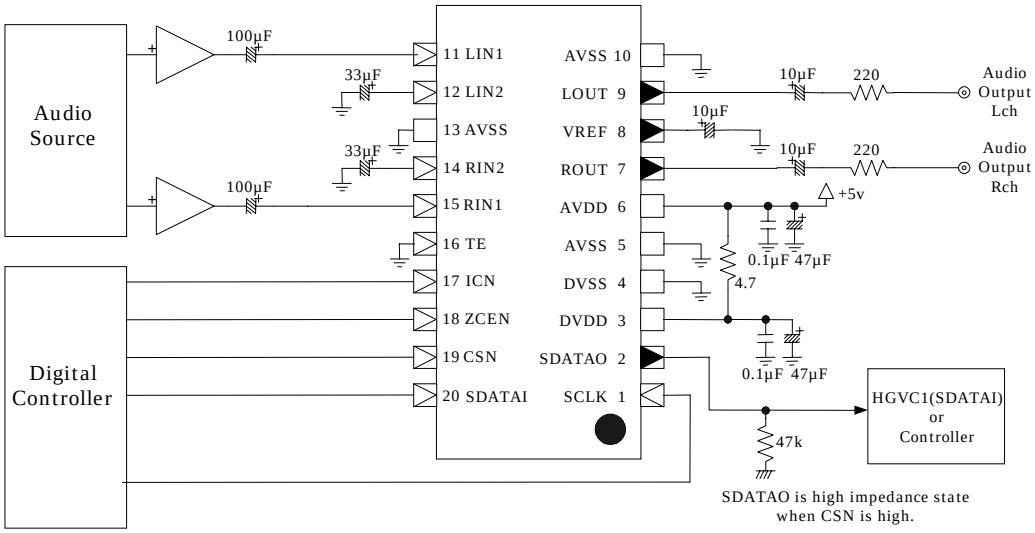
Serial Port Timing Diagram

■ Example of System Configuration (1)

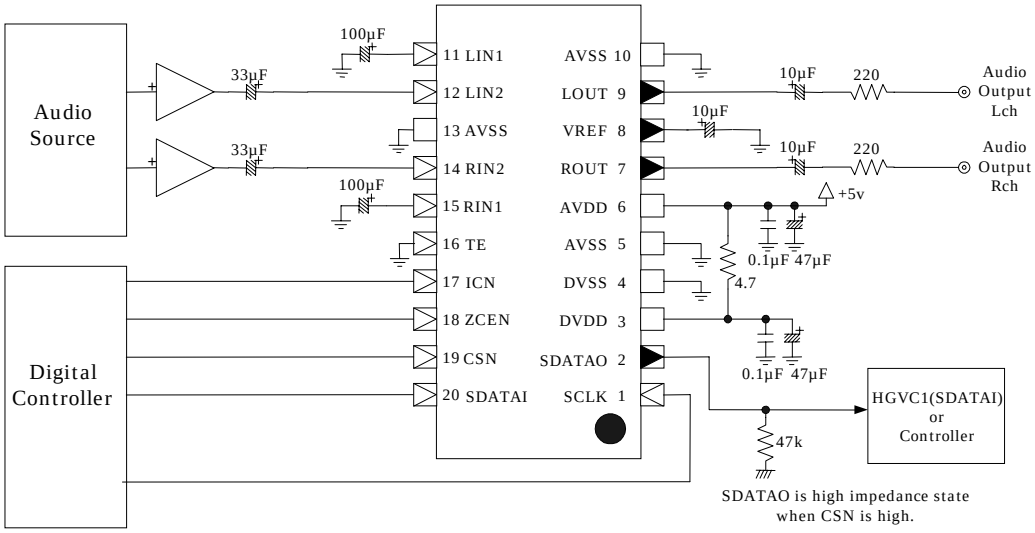
A type (+32.0 to – 95.0dB)
LIN1=LIN2
RIN1=RIN2



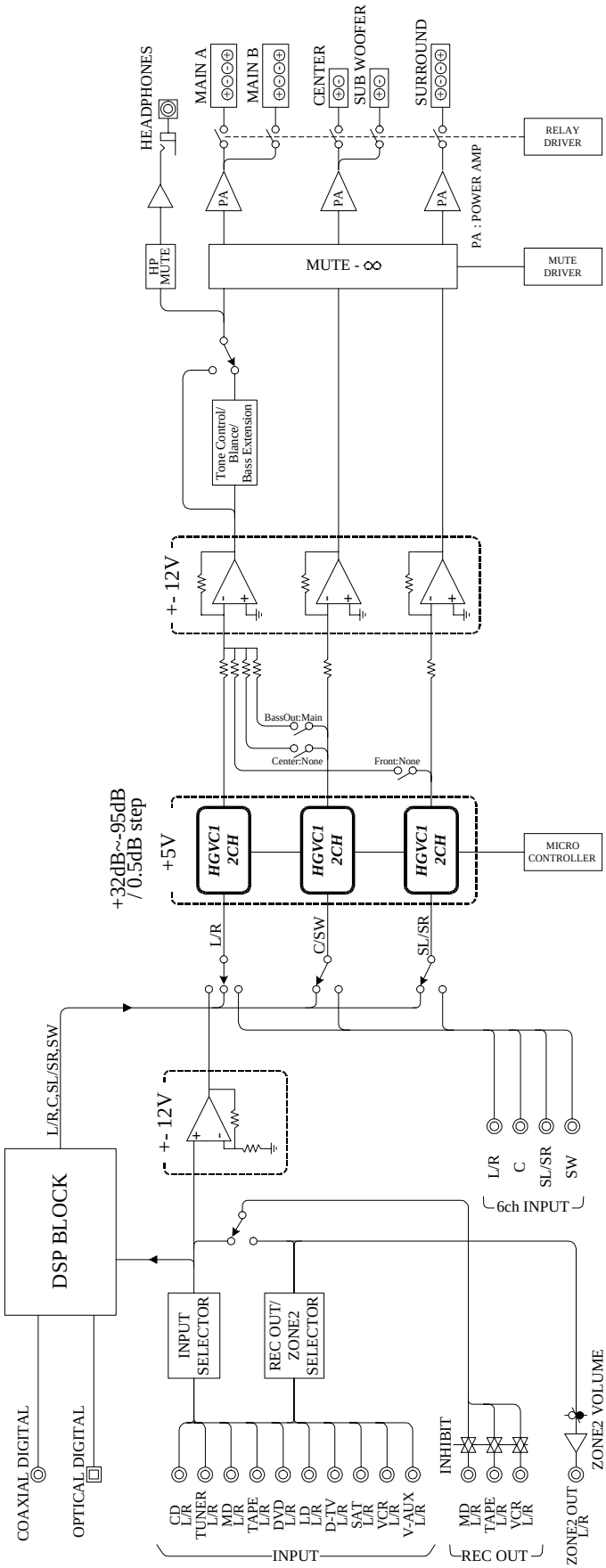
B type (+29.5 to – 97.5dB)
LIN2=GND
RIN2=GND



C type (+20.0 to – 107.0dB)
LIN1=GND
RIN1=GND

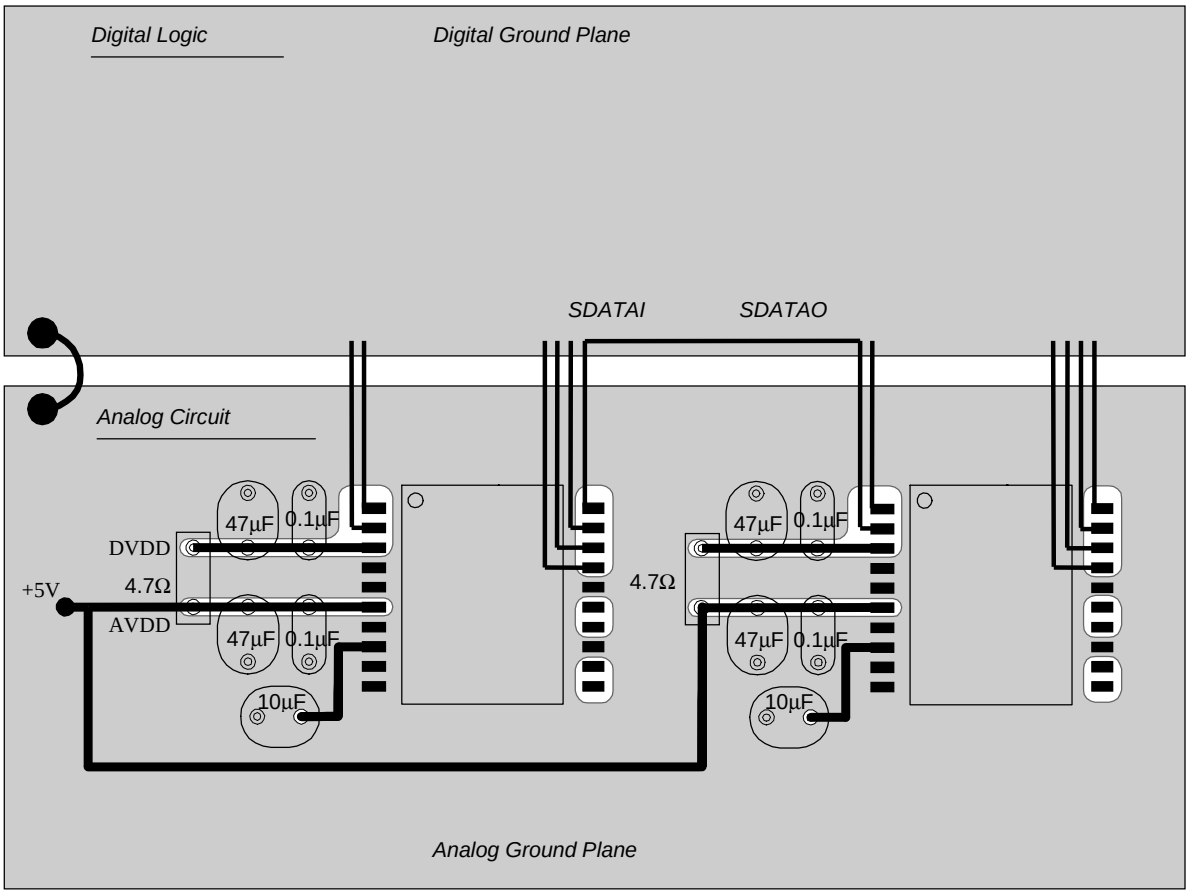


■ Example of System Configuration (2)



6 channels system

■ Example of PCB Layout

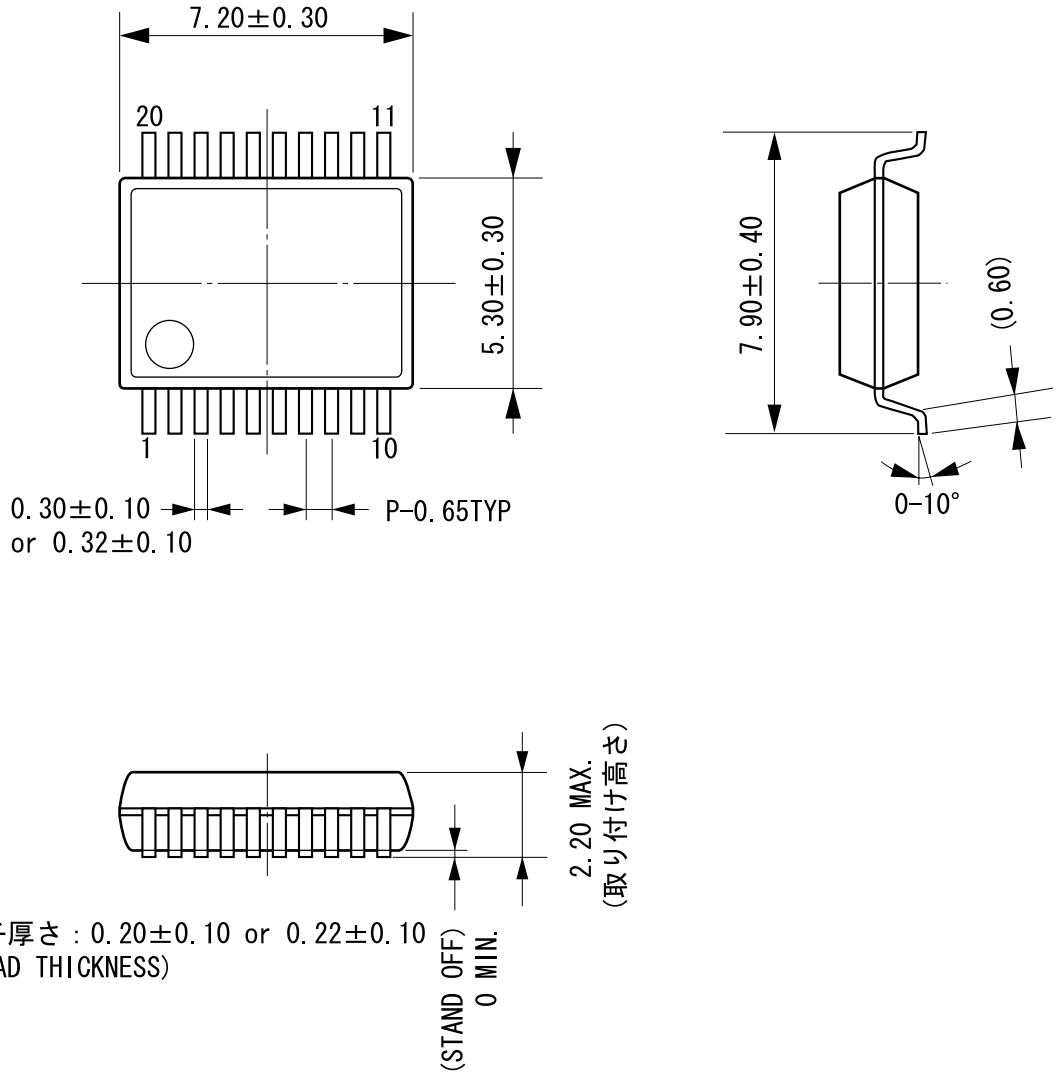


To achieve the maximum performance of this device, it is necessary to take special care for the power supply and the method of grounding. (The above figure shows an example of the layout on the PCB that assumes the daisy chain connection of two HGVC1s.) Connect a regulated low noise 5 V power supply to AVDD, and de-couple with DVDD through a resistor for the purpose of avoiding mixing of noise that is generated in the serial interface. (Refer to ■ Example of System Configuration) At this time, the de-coupling capacitor should be located as close as possible to HGVC1. The analog domain and digital domain should be grounded separately, and HGVC1 should be located in the analog domain side, so that a pattern layout with minimized impedance to AVSS and DVSS pins can be achieved. The analog ground and digital ground should be given sufficiently wide areas respectively so that the radiation of the noise can be suppressed effectively.

Control signals such as serial interface should be placed collectively in the area nearer to the digital ground plane (upper side), and analog signals and digital signals should be arranged without crossing each other and without running side by side to prevent their interference.

■ External Dimensions of Package

C-PK20EP-1



カッコ内の寸法値は参考値とする。
モールド外形寸法はバリを含まない。
単位(UNIT) : mm (millimeters)

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

注) 表面実装LSIは保管条件及び、半田付けについての特別な配慮が必要です。
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