
Table of Contents

Features	1
Applications	1
Description	1
1.0 Functional Description	7
1.1 RF Converter	8
1.2 SAW Driver Amplifier	8
1.3 AGC Detector and ADC	8
1.4 IF AGC Amplifier	8
1.5 VCO	9
1.6 PLL Frequency Synthesizer	10
1.7 General Purpose Switching Ports	10
1.8 I ² C Interface	10
2.0 Programming	11
2.1 Programmable Features	11
2.2 Register Map	11
2.3 Address Register	13
2.4 PLL Registers	13
2.5 Control Register - Byte 5	15
2.6 Control Register - Byte 6	16
2.7 Control Register - Byte 7	17
2.8 Read Mode	18
3.0 Applications Information	20
4.0 Pin Circuit Information	24
5.0 Absolute Maximum Ratings	29
6.0 Operating Range	29
7.0 Electrical Characteristics	30

List of Figures

Figure 1 - Basic Block Diagram	1
Figure 2 - Pin Diagram	5
Figure 3 - Detailed Block Diagram	7
Figure 4 - Low Band (VHF1) External Tank Circuit	9
Figure 5 - Mid Band (VHF3) External Tank Circuit	9
Figure 6 - High Band (UHF) External Tank Circuit	10
Figure 7 - Typical Application Circuit (DVB-T)	20
Figure 8 - Crystal Oscillator Circuit (4 MHz)	21
Figure 9 - Interstage Filter	22
Figure 10 - Noise Figure Measurement Conditions	23

List of Tables

Table 1 - Pin Names	5
Table 2 - Programmable Features	11
Table 3 - Control Registers	12
Table 4 - Address Bit MA1 and MA0 Settings	13
Table 5 - Byte 2- LO Divider (MSB)	13
Table 6 - Byte 3 LO Divider (LSB)	13
Table 7 - Byte 4 PLL Control	13
Table 8 - Charge Pump Current Selection	13
Table 9 - Reference Divide Ratio Settings	14
Table 10 - Byte 5 Control	15
Table 11 - Band Selection	15
Table 12 - Internal Circuit Block Control	15
Table 13 - GPPO Output Port Control	15
Table 14 - Byte 6 Control	16
Table 15 - AGC Decay Current Setting	16
Table 16 - AGC Threshold Selection	17
Table 17 - Byte 7 Control	17
Table 18 - ADC Input Selection	17
Table 19 - Test Modes	17
Table 20 - Read Data Format (MSB is transmitted first)	18
Table 21 - AGC Activity Flag Settings	19
Table 22 - ADC Output Values	19
Table 23 - Optimum CP and LO Trim Settings	23

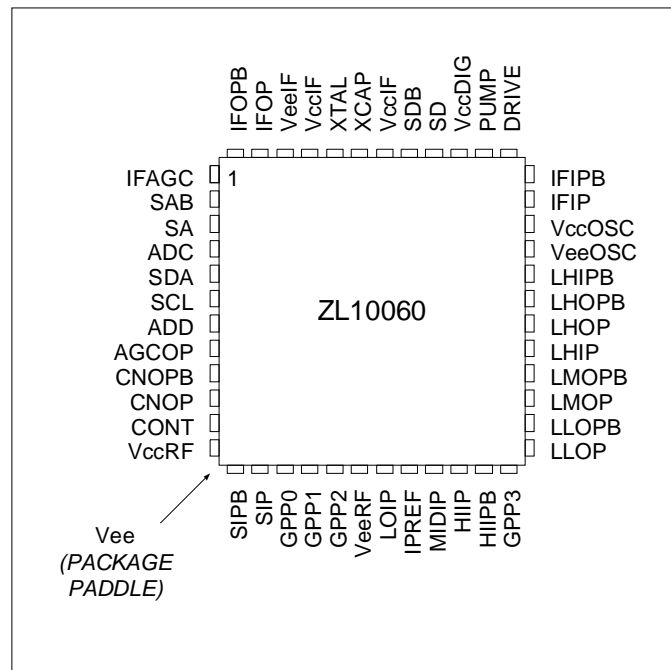


Figure 2 - Pin Diagram

Pin No.	Port Name	Function
1	IFAGC	IF amplifier AGC input
2	SAB	SAW filter driver output (analog)
3	SA	SAW filter driver output (analog)
4	ADC	External ADC input
5	SDA	I ² C bus serial data input/output
6	SCL	I ² C bus serial clock input
7	ADD	I ² C bus address selection input
8	AGCOP	AGC output
9	CNOPB	Analog converter output
10	CNOP	Analog converter output
11	CONT	Paddle (Ground)
12	VccRF	RF section supply
13	SIPB	SAW filter driver input
14	SIP	SAW filter driver input
15	GPP0	General purpose switching port
16	GPP1	General purpose switching port

Table 1 - Pin Names

Pin No.	Port Name	Function
17	GPP2	General purpose switching port
18	VeeRF	RF section ground
19	LOIP	Low band input
20	IPREF	Reference input for low and mid bands
21	MIDIP	Mid band input
22	HIIP	High band input
23	HIIPB	High band inverse input
24	GPP3	General purpose switching port
25	LLOP	Low band local oscillator output
26	LLOPB	Low band local oscillator inverse output
27	LMOP	Mid band local oscillator output
28	LMOPB	Mid band local oscillator inverse output
29	LHIP	High band local oscillator input
30	LHOP	High band local oscillator output
31	LHOPB	High band local oscillator inverse output
32	LHIPB	High band local oscillator inverse input
33	VeeOSC	Oscillator section ground
34	VccOSC	Oscillator supply
35	IFIP	IF amplifier input
36	IFIPB	IF amplifier inverse input
37	DRIVE	Loop amplifier drive output
38	PUMP	Loop amplifier charge pump output
39	VccDIG	Digital section supply
40	SD	SAW filter driver output (digital)
41	SDB	SAW filter driver output (digital)
42	VccIF	IF amplifier section supply
43	XCAP	Reference oscillator feedback input
44	XTAL	Reference oscillator crystal drive
45	VccIF	IF amplifier section supply
46	VeelF	IF section ground
47	IFOP	IF amplifier output
48	IFOPB	IF amplifier inverse output
Paddle	Vee	Global ground

Table 1 - Pin Names (continued)

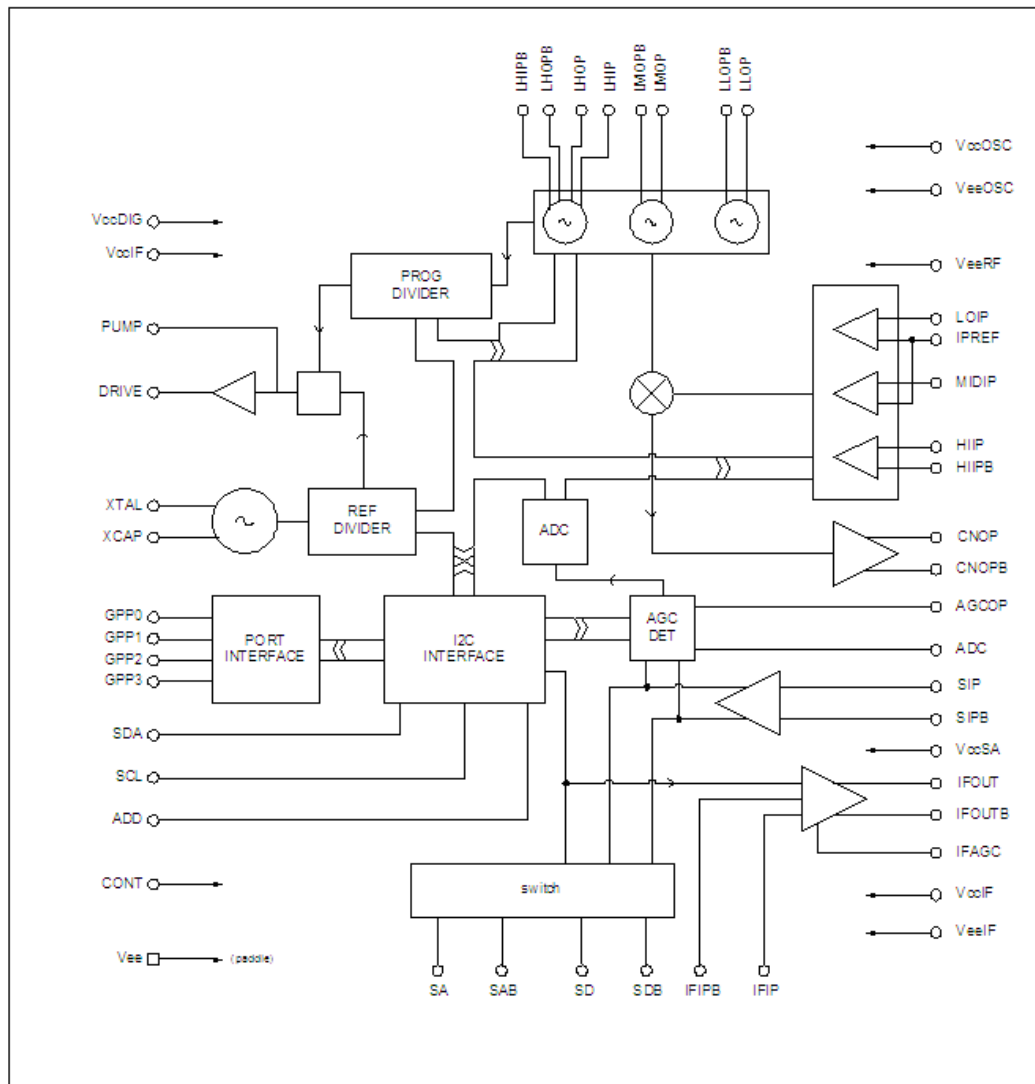


Figure 3 - Detailed Block Diagram

1.0 Functional Description

The ZL10060 is a three-band RF mixer oscillator with on-board frequency synthesizer and IF AGC amplifier, integrating all tuner active circuitry after the tracking filter in a single package.

It is intended for use in all band terrestrial tuners, and requires a minimum external component count. It contains all elements required for RF down conversion to a standard IF with the exception of external VCO tank circuits.

In normal application the RF input is interfaced to the selected mixer oscillator preamplifier through the tuner pre-filter and AGC stages. The ZL10060 provides an RF AGC control signal, which can be used to control the RF gain.

The preamplifier output feeds the mixer stage where the required channel is down converted to the IF frequency. The local oscillator frequency for the down conversion is obtained from the on board PLL and local oscillator, with an external varactor tuned tank.

The downconverted signal is then passed through an external filter into a SAW filter driver amplifier. This provides two output channels for hybrid analog and digital applications.

An AGC IF amplifier is included which provides an output signal to a digital demodulator.

The device is controlled through an I²C compatible interface.

1.1 RF Converter

The ZL10060 contains three input stages to cover the VHF1, VHF3 and UHF frequency bands. The inputs would normally be driven by front end amplifiers and tracking filters. All three inputs are differential, however, the VHF1 and VHF3 inputs would normally be single ended. These inputs therefore can share a common input reference pin. The UHF input should be driven with a differential signal. The inputs are all high impedance. The differential converter IF output is then passed through an external interstage filter. This can be tuned for 36 MHz for DVB-T applications but can also be used at 44 MHz and 57 MHz to be compatible with other TV standards. The recommended filter circuit is shown in Figure 9. The design of this filter provides an impedance transformation as well as rejection of adjacent channels. A 0.5 dB Chebychev filter with 10 MHz bandwidth is recommended. This gives a flat response across the pass band and takes into account normal component tolerances.

1.2 SAW Driver Amplifier

The output of the interstage filter then passes to the SAW filter drive amplifier. This provides further amplification and interfaces to the SAW filter. Two SAW filter drive outputs are provided for hybrid analog and digital applications. Both output stages are identical however the digital output (SD, SDB) should always be used for digital applications as the pin out of the device has been optimized to give the best isolation performance in this configuration. Output selection is programmable however it should be noted that the unselected output is not powered off but operates at a lower power level which means that a signal will still be present on the output.

The differential outputs will drive a balanced SAW filter with a tuning inductor to resonate with the SAW filter input capacitance. The SAW filter can also be driven without the tuning inductor but with the addition of 350 ohm resistors to ground on the SAW driver outputs to increase the output drive capability. This will increase total current consumption by 14 mA.

1.3 AGC Detector and ADC

The ZL10060 contains a broadband AGC detector circuit which provides an output to provide gain control for the RF frontend gain stages. The detector input signal is derived from the signal level in the SAW driver amplifier. The composite signal at this point is the wanted signal plus adjacent channels (N +/- 1, N +/- 2, N +/- 3). The AGC detector threshold point at which the agc output becomes active can be programmed to one of eight levels via the I²C interface. When the composite level reaches the agc threshold, the agc output pin will be active. The AGC attack current is fixed, however, the decay current can be programmed to two levels. The agc output can only drive a high impedance e.g., a dual gate FET. If RF gain control uses a PiN diode then a simple buffer circuit will be required.

An AGC flag output is also available through the I²C interface. This indicates when the AGC output is active i.e., less than 4 volts.

The agc output level can also be monitored by an on chip 3 bit ADC. Although the ADC is 3 bits, only 5 levels are available. Alternatively the ADC can be programmed to measure the voltage on an external pin (ADC Pin 4).

1.4 IF AGC Amplifier

The AGC amplifier amplifies the output of the SAW filter for the digital channel and provides a differential output to the demodulator. The analog gain control signal is normally derived from the demodulator. At least 41 dB of gain control is provided.

The AGC amplifier can be powered down independently of the rest of the device if not required. This mode could be used in analog applications to reduce overall power consumption.

1.5 VCO

Separate VCO's are provided for each band. The oscillator circuits are on chip however the tank circuitry is external. All three oscillators are differential. The typical external tank circuits are shown in Figures 4, 5 and 6. It is essential to take care to minimize track lengths and parasitics when designing the PCB layout to obtain best performance. The close-in phase noise of the local oscillator can be optimized at the programmed operating frequency by a programming bit which increases bias current in the VCO.

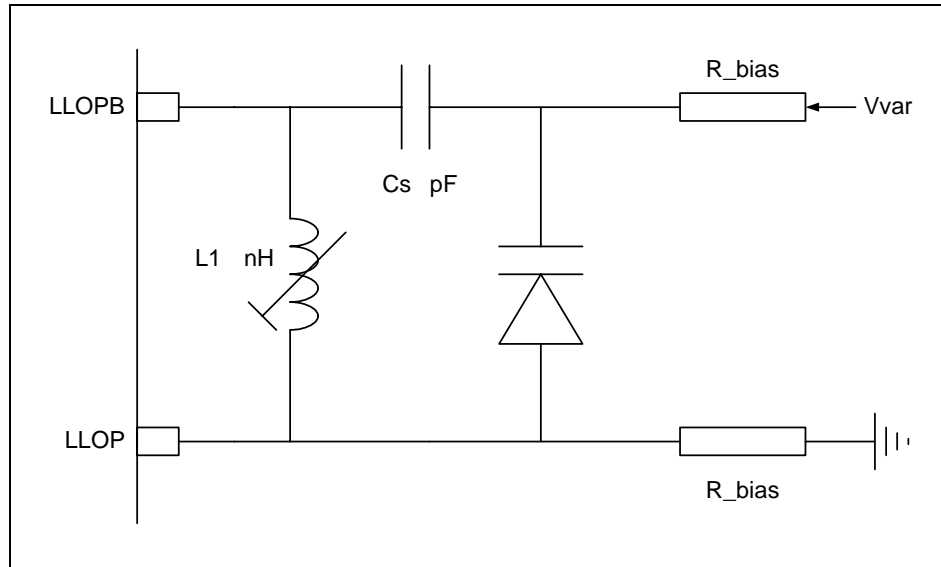


Figure 4 - Low Band (VHF1) External Tank Circuit

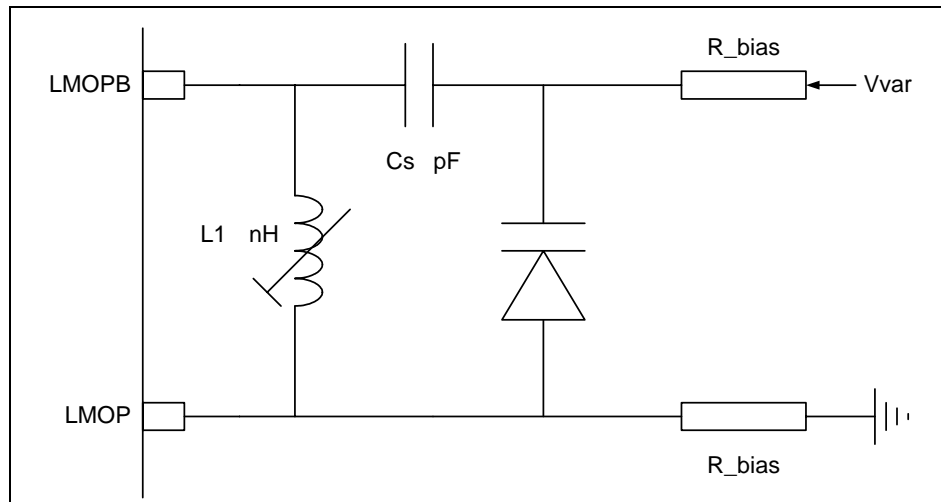


Figure 5 - Mid Band (VHF3) External Tank Circuit

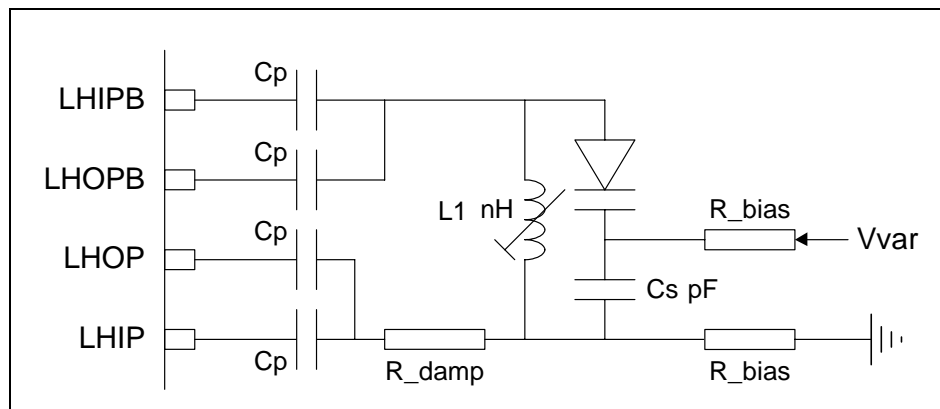


Figure 6 - High Band (UHF) External Tank Circuit

1.6 PLL Frequency Synthesizer

The PLL frequency synthesizer section contains all the elements necessary, with the exception of a frequency reference and loop filter to control a varicap tuned local oscillator, to form a complete PLL frequency synthesized source. The device allows for operation with a high comparison frequency and is fabricated in high speed logic, which enables the generation of a loop with good phase noise performance. It can be operated with comparison frequencies appropriate for frequency offsets as required in digital terrestrial (DTT) receivers.

The LO input signal from the selected oscillator section is routed to an internal preamplifier, which provides gain and reverse isolation from the divider signals. The output of the preamplifier interfaces directly to the 15-bit programmable divider, which is of MN+A architecture, with a 16/17 dual modulus prescaler. The A counter is 4-bits, and the M counter is 11 bits.

The output of the programmable divider is fed to the phase comparator where it is compared in both phase and frequency domain with the comparison frequency which is derived either from the on-board crystal controlled oscillator, or from an external reference source. In both cases the reference frequency is divided down to the comparison frequency by the reference divider, which is programmable into 1 of 16 ratios.

The output of the phase detector feeds a charge pump and loop amplifier section, which when used with an external loop filter, integrates the current pulses into the varactor control voltage.

The programmable divider output, F_{pd} , divided by two and the reference divider output, F_{comp} , can be switched to port P0 by programming the device into a test mode.

The PLL includes a lock detect circuit. The lock detect output is available by reading the Status byte on the I²C interface

1.7 General Purpose Switching Ports

The ZL10060 has four output switching ports. Three of these ports (GPP[3:1]) incorporate a 10 kohm pull up resistor. The remaining port (GPP0) is an open collector switch. These ports can be used for switching external RF input stages for example. Ports GPP[1:0] can also be used as test outputs for debug purposes.

1.8 I²C Interface

The ZL10060 is controlled by an I²C data bus and is compatible with both 3.3 V and 5 V control levels.

Data and Clock are fed in on the SDA and SCL lines respectively as defined by I²C bus format. The device can either accept data (write mode), or send data (read mode). The LSB of the address byte (R/W) sets the device into write mode if it is low, and read mode if it is high. The device can be programmed to respond to 1 of 4 addresses,

which enables the use of more than one device in an I²C bus system. The address is selected by applying a voltage to the 'ADD' input.

When the device receives a valid address byte, it pulls the SDA line low during the acknowledge period, and during following acknowledge periods after further data bytes are received. When the device is programmed into read mode, the controller accepting the data must pull the SDA line low during all status byte acknowledge periods to read another status byte. If the controller fails to pull the SDA line low during this period, the device generates an internal STOP condition, which inhibits further reading.

2.0 Programming

The ZL10060 is fully programmable through the I²C interface. The device can also output data to the controller.

2.1 Programmable Features

Feature	Description
RF programmable divider	Programs PLL main divider
Reference programmable divider	Programs PLL reference divider to set required frequency step
Band selection	Selects RF input and appropriate LO oscillator.
AGC Threshold	Sets the Input Power Level Threshold at which the AGC detector starts to generate a control level.
AGC Decay	Sets the AGC decay current.
Charge pump current	Selects one of the four charge pump current settings.
IF amplifier function	The IF amplifier can be enabled independently of other circuit blocks.
SAWF output select	Select the analog or digital SAW driver output.
Ports GPP[3:1]	These are configured as NPN buffers with 10 kohm pull-up resistors to V _{CC} . Logic '1' = on Logic '0' = off; default on power up
PORT GPP0	This is configured as a NPN open collector buffer. Logic '1' = on Logic '0' = off; default on power up
VCO Trim	Adjusts the VCO bias current to provide optimum phase noise performance.
ADC input Select	Select either the internal AGC detect output level or the external level applied to the ADC input pin.
Programmable power	The ZL10060 has various power saving modes.
Test modes	Test modes to monitor and control internal PLL signals.

Table 2 - Programmable Features

2.2 Register Map

There are a total of 7 write registers, the first of which is the Address register. The control registers are described in detail in the following section. The MSB of each register is written first.

After reception and acknowledgement of a correct address (byte 1), the first bit of the following byte determines whether the byte is interpreted as a byte 2 or 4, a logic '0' indicating byte 2, and a logic '1' indicating byte 4. Having

interpreted this byte as either byte 2 or 4 the following data byte will be interpreted as byte 3 or 5 respectively. Byte 5 will be followed by byte 6 or a stop condition. Byte 6 will be followed by byte 7 or a stop condition. Byte 7 will be followed by a stop condition or a byte 2 or byte 4 as described above. Further data bytes can be programmed following the above-described protocol. A STOP condition can be generated after any data byte, if however it occurs during a byte transmission, the previous byte data is retained. To facilitate smooth fine tuning, the frequency data bytes are only accepted by the device after all 15 bits of frequency data have been received, or after the generation of a STOP condition.

	MSB							LSB	ACK	
	7	6	5	4	3	2	1	0		
Address	1	1	0	0	0	MA1	MA0	0	A	Byte 1
Programmable divider	0	D14	D13	D12	D11	D10	D9	D8	A	Byte 2W
Programmable divider	D7	D6	D5	D4	D3	D2	D1	D0	A	Byte 3W
Control data	1	C1	C0	R4	R3	R2	R1	R0	A	Byte 4W
Control data	BS1	BS0	SL1	SL0	P3	P2	P1	P0	A	Byte 5W
Control Data	LO1	LO0	ATC	IFE	X	AT2	AT1	AT0	A	Byte 6W
Control Data	SAS	X	AGD	ADS	T3	T2	T1	T0	A	Byte 7W

Table 3 - Control Registers

A	Acknowledge bit
MA1, MA0	Address bits
D14-D0	Programmable division ratio control bits
R4-R0	Reference division ratio select
C1, C0	Charge pump current select
BS1-BS0	Band select bits
SL1-SL0	Power down modes
SAS	SAWF drive output select
P3-P0	P3-P0 port output states
ADS	ADC input select
ATC	AGC Decay Current
AGD	AGC Disable
AT2:AT0	AGC Onset threshold Control
LO1:LO0	LO trim control bits
T3-T0	Test mode control bits
IFE	IF AGC amplifier enable
X	Don't Care

Details of the programming registers are shown in the following sections. Default values on power up are also shown.

2.3 Address Register

The ZL10060 address (MA1, MA0) are determined by the voltage set at the address pin (ADD) as shown in Table 4.

Address Select (Byte 1)		
MA1	MA0	Address Input Voltage Level
0	0	0 - 0.1V _{CC} (Connect to V _{ee})
0	1	0.2V _{CC} – 0.3V _{CC} (Open circuit)
1	0	0.4 V _{CC} – 0.6 V _{CC} (30KΩ to V _{CC})
1	1	0.9 V _{CC} - 1.0 V _{CC} (Connect to V _{CC})

Table 4 - Address Bit MA1 and MA0 Settings

2.4 PLL Registers

Bytes 2,3 and 4 are used to program the PLL.

Bit Field	Name	Default	Description
7	-	0	Must be set to 0
6:0	D[14:8]	0	MSB bits of LO Divider register.

Table 5 - Byte 2- LO Divider (MSB)

Bit Field	Name	Default	Description
7:0	D[7:0]	0	LSB bits of LO Divider register.

Table 6 - Byte 3 LO Divider (LSB)

The LO frequency will not be updated until both Byte 1 and Byte 2 have been programmed.

Bit Field	Name	Default	Description
7	-	1	Must be set to 1
6:5	C[1:0]	0	Charge pump current.
4:0	R[4:0]	10011	Reference divider control.

Table 7 - Byte 4 PLL Control

The charge pump current values are selected from the following table:

C1	C0	Current
		μA
0	0	+155

Table 8 - Charge Pump Current Selection

C1	C0	Current
		μA
0	1	+330
1	0	+690
1	1	+1450
<i>Default State on power up = 00</i>		

Table 8 - Charge Pump Current Selection

The reference divider ratio can be selected from the following table:

R4	R3	R2	R1	R0	Ratio
0	0	0	1	1	16
0	0	1	0	0	32
0	0	1	0	1	64
0	0	1	1	0	128
0	1	0	1	1	20
0	1	1	0	0	40
0	1	1	0	1	80
0	1	1	1	0	160
1	0	0	1	1	24
1	0	1	0	0	48
1	0	1	0	1	96
1	0	1	1	0	192
1	1	0	1	1	28
1	1	1	0	0	56
1	1	1	0	1	112
1	1	1	1	0	224
<i>Default State on power up = 10011</i>					

Table 9 - Reference Divide Ratio Settings

2.5 Control Register - Byte 5

Bit Field	Name	Default	Description
7:6	BS[1:0]	11	Band Switching
5:4	SL[1:0]	01	Power-up modes
3:0	P[3:0]	0	General Purpose Output ports

Table 10 - Byte 5 Control

The band switching is controlled as shown below:

BS1	BS0	Band Selected
0	0	LO Band
0	1	MID Band
1	0	HI band
1	1	All off
		Default state on power up = 11

Table 11 - Band Selection

The various power-up modes are shown below. The IF AGC amplifier is controlled separately. The I²C interface and crystal oscillator circuit is active in all modes.

		Power Mode	Section Status			
SL1	SL0		I ² C interface and registers	Crystal oscillator	PLL & VCO	Converter and IF stages
0	X	Sleep	Enabled	Enabled	Disabled	Disabled
1	0	PLL and VCO enabled	Enabled	Enabled	Enabled	Disabled
1	1	Full	Enabled	Enabled	Enabled	Enabled

Table 12 - Internal Circuit Block Control

The ZL10060 has four output ports. Ports [3:1] have an internal 10 kohm pull up resistor to Vcc. GPP0 is open collector.

Function	Bit	0	1
GPP0 output Enable	P0	Off (High Impedance)	On (Current Sink)
GPP1 output Enable	P1	Off	On (Current Sink)
GPP2 output Enable	P2	Off	On (Current Sink)
GPP3 output Enable	P3	Off	On (Current Sink)

Table 13 - GPPO Output Port Control

2.6 Control Register - Byte 6

Bit Field	Name	Default	Description
7	LO1	0	VCO Bias Trim
6	LO0	0	Not used
5	ATC	0	AGC Decay current select
4	IFE	0	IF AGC Amplifier enable (1 = On)
3	X	0	Not used
2:0	AT[2:0]	0	AGC Threshold Select

Table 14 - Byte 6 Control

The VCO bias trim adjusts the VCO bias to give optimum close-in phase noise. In general this should be set to 1 for the lower third of the VCO frequency range.

The AGC attack current is fixed at 100 μA however the agc decay current can be programmed to one of two values as shown below. If the PLL is unlocked ($\text{FL} = 0$), then the ATC control is over-ridden and the AGC decay current is set to 10 μA . When the PLL locks ($\text{FL} = 1$) the decay current reverts to the programmed ATC value.

ATC	AGC Decay Current (μA)
0	10.0
1	0.3

Table 15 - AGC Decay Current Setting

The AGC threshold can be programmed using the AT[2:0] bits. Note that the programmed value is dB μ V peak.

AT2	AT1	AT0	AGC Threshold (peak signal in dB μ V into detector)
0	0	0	120
0	0	1	118
0	1	0	116
0	1	1	114
1	0	0	112
1	0	1	110
1	1	0	107
1	1	1	104
			Default state on power up = 000

Table 16 - AGC Threshold Selection

2.7 Control Register - Byte 7

Bit Field	Name	Default	Description
7	SAS	1	Digital SAW Drive Output Select (1 = Digital)
6	X	0	Not used
5	AGD	1	AGC Detector Enable (0 = Enabled)
4	ADS	0	ADC Input select
3:0	T[3:0]	0	Test Bits

Table 17 - Byte 7 Control

The ADC input selection is shown in the table below

ADS	ADC Function
0	AGC Output
1	External ADC input

Table 18 - ADC Input Selection

The test bits T[3:0] allow internal PLL signals to be monitored and also to manually control charge pump current and AGC detector output. This facilities may be useful during debug. The test bit selection is shown below. The reserved test modes should not be used.

T3	T2	T1	T0	Test Mode Description
0	0	0	0	Normal operation
0	0	0	1	Reserved Test Mode
0	0	1	0	AGC Sink, Force $I_{agc} = -100 \mu A$
0	0	1	1	AGC Source, Force $I_{agc} = 10 \mu A$ P0 = Output of AGC bias DAC

Table 19 - Test Modes

T3	T2	T1	T0	Test Mode Description
0	1	0	0	Reserved Test Mode
0	1	0	1	Reserved Test Mode
0	1	1	0	Reserved Test Mode
0	1	1	1	Reserved Test Mode
1	0	0	0	Reserved Test Mode
1	0	0	1	Charge pump sink * Status byte FL set to logic '0'
1	0	1	0	Charge pump source * Status byte FL set to logic '0'
1	0	1	1	Charge pump disabled * Status byte FL set to logic '1'
1	1	0	0	Port P0 = $F_{pd}/2$
1	1	0	1	Charge pump sink * Status byte FL set to logic '0' Port P0 = F_{comp}
1	1	1	0	Charge pump source * Status byte FL set to logic '0' Port P0 = F_{comp}
1	1	1	1	Charge pump disabled * Status byte FL set to logic '1' Port P0 = F_{comp}

Table 19 - Test Modes (continued)

2.8 Read Mode

When the device is in read mode, the status byte read from the device takes the form shown in Table 20.

	MSB							LSB	ACK	
	7	6	5	4	3	2	1	0		
Address	1	1	0	0	0	MA1	MA0	1	A	Byte 1
Status Byte	POR	FL	1	1	AGF	V2	V1	V0	A	Byte 2R

Table 20 - Read Data Format (MSB is transmitted first)

The following describes data read through the read byte;

- **Bit 7 (POR)** is the power-on reset indicator, and this is set to a logic '1' if the V_{CC} supply to the device has dropped below 3 V (at 25°C), e.g., when the device is initially turned ON. The POR is reset to '0' when the read sequence is terminated by a STOP command. When POR is set high this indicates that the programmed information may have been corrupted and the device reset to power up condition.
- **Bit 6 (FL)** is the PLL lock flag and indicates whether the device is phase locked, a logic '1' is present if the device is locked, and a logic '0' if the device is unlocked. The FL bit is set after 64 consecutive comparison cycles in lock.

- **Bit 3 (AGF)** is the AGC detector flag and indicates whether the AGC detector is active.

AGF	AGC Activity Flag
0	AGC active, $V_{AGC} < 4\text{ V}$ External RF LNA gain is reduced
1	AGC not active, $V_{AGC} > 4\text{ V}$ External RF LNA gain is at maximum

Table 21 - AGC Activity Flag Settings

- **Bits 2:0 (V2:V0)** contain the ADC output data. The ADC output is sampled on the ACK clock of the read address byte.

Input Level (V)	V2	V1	V0
< 0.32 Vcc	0	0	0
0.32Vcc to 0.48Vcc	0	0	1
0.48Vcc to 0.64Vcc	0	1	0
0.64Vcc to 0.80Vcc	0	1	1
> 0.80Vcc	1	0	0

Table 22 - ADC Output Values

The low (VHF1) and Mid (VHF3) bands are single ended however the high band (UHF) should be differential. All IF signals are differential.

It is essential to have good RF layout around the RF stages, i.e., RF inputs and the VCOs. Track lengths around the VCO's should be minimized to reduce track inductance.

The layout should be organized to give good isolation between the IF signal paths. In particular good isolation is required between the outputs and inputs of the IF AGC amplifier. Isolation across the SAW filter is also important to ensure rejection of unwanted adjacent signals. This can be achieved by routing input and output tracks on opposite sides of the board.

It is also important to have good isolation between the high level IF signal and the crystal oscillator circuit to minimize any interactions. Care should be taken when locating IF tuning inductors to ensure there is no radiation to other parts of the circuit.

The crystal oscillator can also provide a clock signal to the demodulator. This can be done by taking the oscillator signal from the crystal series capacitor (27 pF) as shown in the following diagram.

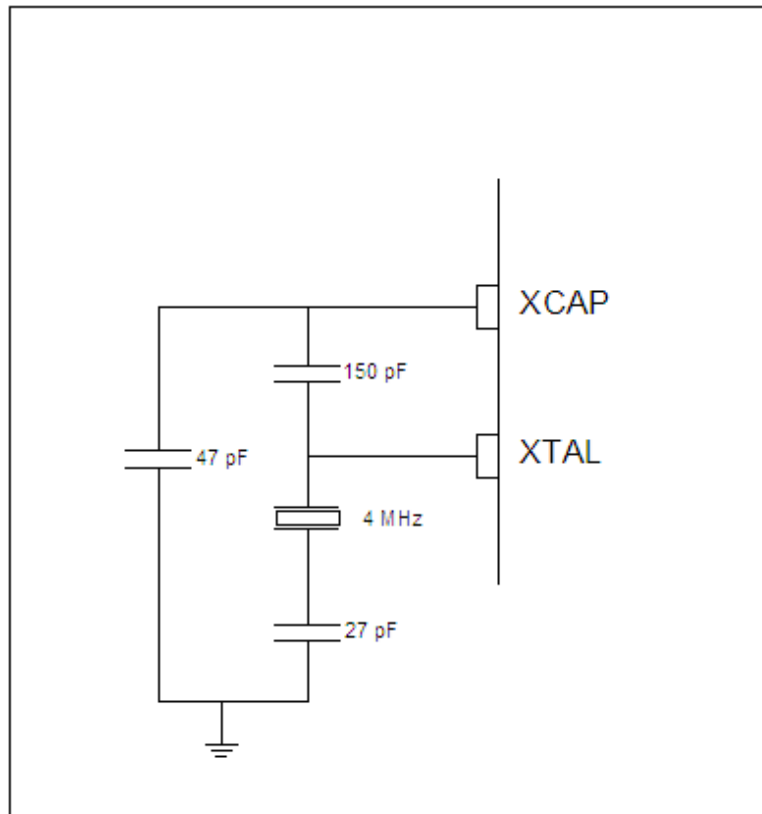


Figure 8 - Crystal Oscillator Circuit (4 MHz)

The interstage filter between the converter outputs provides some rejection of adjacent channels ($N \pm 2$). The recommended values are shown in Figure 9. The choice of components is important not only to give a flat response but also to provide an impedance transformation.

The specified noise figure for the low and mid bands assumes that there will be a network before the device to provide image rejection. In a tuner this would be part of the input tracking filters but for test purposes a network is shown in Figure 10.

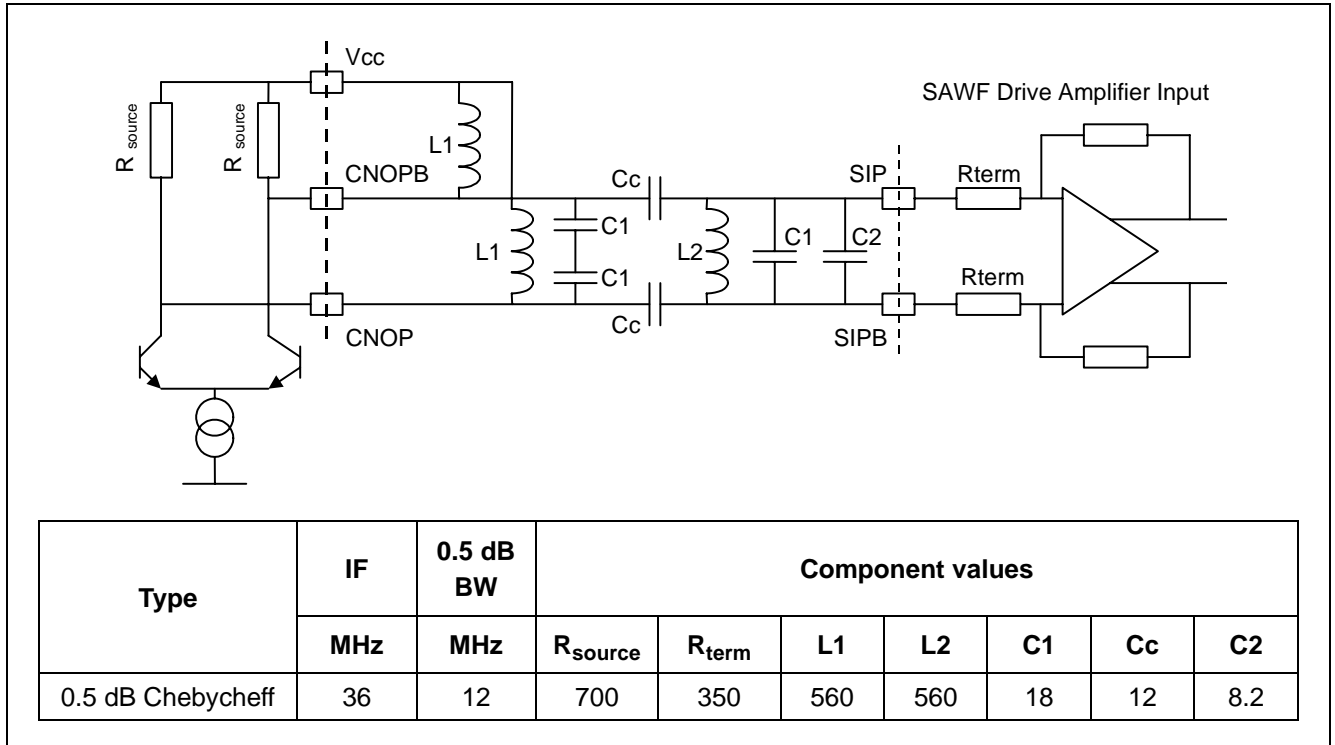
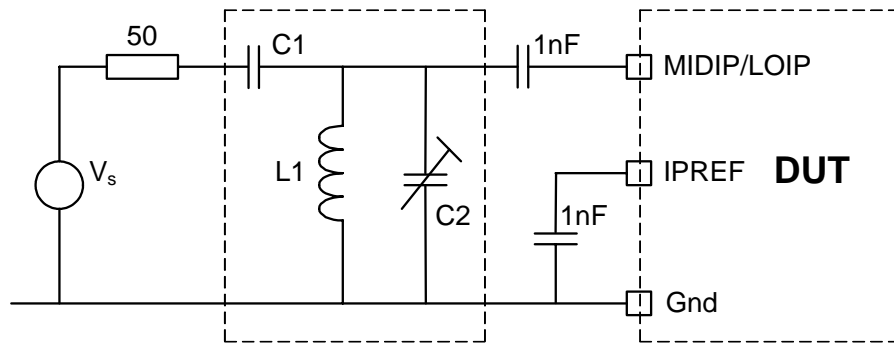


Figure 9 - Interstage Filter



Band	Frequency		C1	L1	C2
	LO	RF IN			
	MHz	MHz	pF	nH	pF
LOW	90	46	20	299	20
LOW	200	156	8	65	8
MID	240	196	8	41	8
MID	500	446	2.1	21	4

Figure 10 - Noise Figure Measurement Conditions

The optimum charge pump and LO trim settings for the application circuit shown in Figure 8 are shown in the table below. These give the optimum phase noise performance for the circuit shown. The changes in charge pump current compensate for frequency and VCO gain variations.

Frequency Range	Charge Pump Setting CP	LO Trim LO1
VHF1 50 -110 MHz	01	1
VHF1 100 -160 MHz	10	1
VHF3 160 - 250 MHz	10	1
VHF3 250 - 350 MHz	01	0
VHF3 350 - 450 MHz	10	0
UHF 450 - 500 MHz	00	1
UHF 500 - 700 MHz	01	1
UHF 700 - 800 MHz	10	1
UHF 800 - 850 MHz	11	1

Table 23 - Optimum CP and LO Trim Settings

4.0 Pin Circuit Information

Pin No.	Pin Name	Port Sense	Function	Schematic
1	IFAGC	Input	IF AGC control	<p>The schematic shows a differential pair of transistors. The input IFAGC is connected to the base of the left transistor through a 3K resistor. The base of the right transistor is also connected to the IFAGC input through a 3K resistor. The emitters of both transistors are connected to ground through a common resistor. The collector of the right transistor is connected to the VREF output.</p>
2, 3	SAB, SA	Output, Output	SAW filter driver output A inverse SAW filter driver output A	<p>The schematic shows a single transistor with its emitter connected to ground. The base is connected to VCC through a resistor. The collector is connected to the SA and SAB outputs through a 50 ohm resistor.</p>
4	ADC	Input	ADC input	<p>The schematic shows a differential pair of transistors. The input ADC is connected to the base of the left transistor. The base of the right transistor is connected to ground. The emitters of both transistors are connected to ground through a common resistor. The collector of the right transistor is connected to VCC through a resistor.</p>
5	SDA	Bi-directional	I ² C bus serial data input/output	<p>The schematic shows a bi-directional driver circuit. The input SDA is connected to the base of a transistor. The emitter is connected to ground. The collector is connected to VCC through a resistor. The output is taken from the collector.</p>
6	SCL	Input	I ² C bus serial clock input	<p>The schematic shows a simple input driver circuit. The input SCL is connected to the base of a transistor. The emitter is connected to ground. The collector is connected to VCC through a resistor. The output is taken from the collector.</p>

Pin No.	Pin Name	Port Sense	Function	Schematic
7	ADD	Input	I ² C address select	
8	AGCOP	Output	AGC output	
9, 10	CNOPB, CNOP	Output, Output	Converter Output inverse Converter Output	
11	Cont	-	Paddle	-
12	VccRF	Supply	RF section supply	-
13, 14	SIPB, SIP	Input, Input	SAW filter driver input inverse, SAW filter driver input	
15	GPP0	Output	Switching port/Test output 1	

Pin No.	Pin Name	Port Sense	Function	Schematic
16	GPP1	Output	Switching port/Test output 2	
17	GPP2	Output	Switching port	As GPP1 (pin16)
18	VeeRF	Supply	RF section ground	-
19, 20, 21	LOIP IPREF MIDIP	Input, Input, Input	Low band input, Mid- and Low-band i/p reference, Mid-band input	
22, 23	HIIP, HIIPB	Input, Input	Hi-band input, Hi-band input inverse	
24	GPP3	Output	Switching Port	As GPP1 (pin16)
25, 26	LLOP, LLOPB	Output	Low band oscillator output, Low-band oscillator output inverse	
27, 28	LMOP, LMOPB	Output, Output	Mid-band oscillator output, Mid-band oscillator output inverse	

Pin No.	Pin Name	Port Sense	Function	Schematic
29, 30, 31, 32	LHIP, LHOP, LHOPB, LHIPB	Input, Output, Output, Input	High band oscillator input, High-band oscillator output, High-band oscillator output inverse, High-band oscillator input inverse	
33	VeeOSC	Supply	LO ground	-
34	VccOSC	Supply	LO supply	-
35, 36	IFIP, IFIPB	Input, Input	IF AGC amp input, IF AGC amp input inverse	
37, 38	DRIVE, PUMP	Output, Output	Loop amplifier drive output, Loop amp charge pump output	
39	VccDIG	Supply	Digital section supply	-
40, 41	SD, SDB	Output, Output	SAW filter driver output D, SAW filter driver o/p D inverse	
42	VccIF	Supply	SAWF output supply	-
43	XCAP	Input	Reference osc feedback input	
44	XTAL	Output	Reference osc crystal drive	See XCAP (pin 43)

Pin No.	Pin Name	Port Sense	Function	Schematic
45	VccIF	Supply	IF AGC supply	-
46	VeeIF	Supply	IF AGC ground	-
47, 48	IFOP, IFOPB	Output, Output	IF AGC amp output, IF AGC amp inverse output	
Paddle	Vee	-	-	-

5.0 Absolute Maximum Ratings

All voltages are referred to V_{ee} at 0 V.

Characteristic	Min.	Max.	Units	Conditions
Supply voltage	-0.3	6	V	
RF input voltage		117	dB μ V	Transient condition only
Maximum voltage on SDA, SCL		5.5	V	$V_{cc} = 0$ to 5.5V
Max voltage on all remaining signal pins	-0.3	$V_{cc}+0.3$	V	The voltage on any pin must not exceed 6 V
Total port current		20	mA	
Storage temperature	-55	150	$^{\circ}$ C	
Junction temperature		125	$^{\circ}$ C	Power applied
Package thermal resistance (chip to ambient)		27	$^{\circ}$ C/W	Package paddle soldered to ground
ESD protection	2.0		kV	All pins except 9,10
Mil-std 883B method 3015 cat1	1.25		kV	Pins 9, 10 only

6.0 Operating Range

All voltages are referred to V_{ee} at 0 V.

Characteristic	Min.	Max.	Units.	Conditions
Supply voltage	4.5	5.5	V	Functional operation, specification not guaranteed
Supply voltage	4.75	5.25	V	Full specification
Ambient Temperature	-20	85	$^{\circ}$ C	
Low Band Input Frequency	50	170	MHz	
Mid Band Input Frequency	140	460	MHz	
High Band Input Frequency	400	900	MHz	

7.0 Electrical Characteristics

Test conditions (unless otherwise stated). T = 25°C, $V_{ee} = 0$ V, $V_{cc} = 5$ V, IF Frequency = 36 MHz. All signals are differential with the exception of VHF1 and VHF3 inputs.

Characteristic	Min.	Typ.	Max.	Units	Conditions
Supply current					
Normal operation		117	140	mA	Total Current – UHF band All switching ports off
All sections active		110	134	mA	Total Current - VHF Bands All switching ports off
All sections active except AGC IF amplifier		92		mA	UHF Band. Switching ports off
		85		mA	VHF Bands. Switching ports off
Sleep Mode		9		mA	Crystal oscillator and data interface enabled
		33		mA	PLL and crystal oscillator enabled
Composite system to SAW Filter driver outputs VHF1 Band					
Conversion gain	29	32	35	dB	RFin = 54 MHz. Single ended input
Conversion gain	29	32	35	dB	RFin = 155 MHz. Single ended input
Noise Figure		9	11	dB	$R_s = 50 \Omega$, SSB with input matching network. See Figure 10.
OPIP3	135	146		dB μ V	Two output tones at 110 dB μ V
Output level causing 1% cross modulation	113	120		dB μ V	Note 2
Output level causing 1.5 kHz FM	113	120		dB μ V	Note 3
I ² C bus transmission induced LO frequency modulation		2.5		kHz	Transmission repetition rate of 20 msec minimum with no change to previously loaded data, at 100 kHz SCL rate
N+5 Direct modulation of VCO			-40	dBc	Local oscillator sidebands induced by an input carrier at 80 dB μ V offset from local oscillator by 100 kHz
Supply ripple spurious			-40	dBc	Residual FM induced on local oscillator by 20 mV _{p-p} ripple on V_{cc} at 500 kHz
Local oscillator leakage to any band input		30		dB μ V	

Characteristic	Min.	Typ.	Max.	Units	Conditions
IPIP2	134	143		dB μ V	Two input tones at 87 dB μ V at 90 MHz and 66 MHz with local oscillator at 114 MHz
IPIP3	112	120		dB μ V	Desired = 54 MHz at 45 dB μ V Undesired = 60 and 72 MHz at 87 dB μ V
IPIP3	112	119		dB μ V	Desired = 155 MHz at 45 dB μ V Undesired = 161 and 173 MHz at 87 dB μ V
P1dB	93	106		dB μ V	
Output Impedance		100		Ω	
		10		nH	
Phase Noise, SSB					PLL Loop Bandwidth ~ 3 kHz $f_{comp} = 166.7$ kHz
1 kHz		-90	-70	dBc/Hz	
10 kHz		-95	-86	dBc/Hz	
100 kHz		-115	-106	dBc/Hz	
10 MHz			-135	dBc/Hz	Noise Floor
Reference spurs		-90	-50	dBc	
Phase Noise, SSB					Narrow PLL Loop Bandwidth $f_{comp} = 62.5$ kHz
10 kHz		-97		dBc/Hz	
100 kHz		-115		dBc/Hz	
Composite system to SAW Filter driver outputs VHF3 Band					
Conversion gain	29	32	35	dB	RFin = 164 MHz Single ended input
Conversion gain	29	32	35	dB	RFin = 442 MHz Single ended input
Noise Figure		9	11	dB	Rs = 50 Ω , SSB with input matching network. See Figure 10.
OPIP3	135	146		dB μ V	Two output tones at 110 dB μ V
Output level causing 1% cross modulation	113	120		dB μ V	Note 2
Output level causing 1.5 kHz FM	113	120		dB μ V	Note 3

Characteristic	Min.	Typ.	Max.	Units	Conditions
I ² C bus transmission induced LO frequency modulation		2.5		kHz	Transmission repetition rate of 20 msec minimum with no change to previously loaded data, at 100 kHz SCL rate
N+5 Direct modulation of VCO		-	-40	dBc	Local oscillator sidebands induced by an input 750 MHz carrier at 80 dB μ V offset from local oscillator by 100 kHz.
Supply ripple spurious			-40	dBc	Residual FM induced on local oscillator by 20 mV _{p-p} ripple on V _{CC} at 500 kHz
Local oscillator leakage to any band input		30		dB μ V	
IPIP2	134	143		dB μ V	Two input tones at 89 dB μ V at 198 MHz and 398 MHz with local oscillator at 240 MHz
IPIP3	112	122		dB μ V	Desired = 165 MHz at 45 dB μ V Undesired = 171 and 183 MHz at 89 dB μ V
IPIP3	112	119		dB μ V	Desired = 438 MHz at 45 dB μ V Undesired = 444 and 456 MHz at 89 dB μ V
P1dB	-95	107		dB μ V	
Output Impedance		100		Ω	
		10		nH	
Phase Noise, SSB					PLL Loop Bandwidth ~ 3 kHz f _{comp} = 166.7 kHz
1 kHz		-87	-70	dBc/Hz	
10 kHz		-92	-86	dBc/Hz	
100 kHz		-114	-106	dBc/Hz	
10 MHz			-135	dBc/Hz	Noise Floor
Reference spurs		-90	-50	dBc	
Phase Noise, SSB					Narrow PLL Loop Bandwidth f _{comp} = 62.5 kHz
10 kHz		-94		dBc/Hz	
100 kHz		-114		dBc/Hz	
Composite system to SAW Filter driver outputs UHF Band					
Conversion gain	35	38	41	dB	RFin = 450 MHz

Characteristic	Min.	Typ.	Max.	Units	Conditions
Conversion gain	35	38	41	dB	RFin = 866 MHz
Noise Figure		6	8	dB	Rs = 50 Ω, No image correction
OPIP3	135	146		dBμV	Two output tones at 110 dBμV
Output level causing 1% cross modulation	113	120		dBμV	Note 2
Output level causing 1.5 kHz FM	113	120		dBμV	Note 3
I ² C bus transmission induced LO frequency modulation		2.5		kHz	Transmission repetition rate of 20 msec minimum with no change to previously loaded data, at 100 kHz SCL rate
N+5 Direct modulation of VCO			-30	dBc	Local oscillator sidebands induced by an input 750 MHz carrier at 80 dBμV offset from local oscillator by 100 kHz
Supply ripple spurious			-40	dBc	Residual FM induced on local oscillator by 20 mV _{p-p} ripple on V _{CC} at 500 kHz
Local oscillator leakage to any band input		60		dBμV	
IPIP2	125	159		dBμV	Two input tones at 89 dBμV at 198 MHz and 398 MHz with local oscillator at 240 MHz
IPIP3	108	115		dBμV	Desired = 438 MHz at 45 dBμV Undesired = 444 and 456 MHz at 85 dBμV
IPIP3	108	112		dBμV	Desired = 858 MHz at 45 dBμV Undesired = 864 and 876 MHz at 85 dBμV
P1dB	91	99		dBμV	
Output Impedance		100		Ω	
		10		nH	
Phase Noise, SSB					PLL Loop Bandwidth ~ 3 kHz f _{comp} = 166.7 kHz
1 kHz		-78	-70	dBc/Hz	
10 kHz		-89	-84	dBc/Hz	
100 kHz		-113	-106	dBc/Hz	
10 MHz			-135	dBc/Hz	Noise Floor
Reference spurs		-80	-50	dBc	

Characteristic	Min.	Typ.	Max.	Units	Conditions
Phase Noise, SSB					Narrow PLL Loop Bandwidth $f_{\text{comp}} = 62.5 \text{ kHz}$
10 kHz		-91		dBc/Hz	
100 kHz		-113		dBc/Hz	
AGC Detector and ADC					
Operating frequency range	16		72	MHz	
AGC Threshold Level		120		dB μ V	AT[2:0] = 0
ADC leakage current			60	nA	$V_{\text{ADC}} = 4.0 \text{ V}$
	-60			nA	$V_{\text{ADC}} = 0.5\text{V}$
AGC source current	6.8	10	13.3	μ A	See Table 15
	0.25	0.33	0.43	μ A	
AGC sink current	-65	-100	-145	μ A	AGC attack current, triggered by detected level exceeding AGC attack point
AGC sink current 90% rise and fall time		1		μ sec	
AGC input level response			1	dB	Change in input level for AGC sink current to change from high impedance to 90% of maximum value, with AGC operative
AGCOP output impedance	20			M Ω	AGC inactive
AGCOP output voltage range			0.5	V	Minimum gain required
	4			V	Maximum gain required
External AGC voltage	0.5		$V_{\text{CC}}-0.4$	V	Maximum external voltage range which can be applied to AGCOP when disabled
AGCOP leakage current	-50		50	nA	Over normal operating range
ADC step size, LSB		$0.16V_{\text{C}}$ c		V	See Table 22
ADC step size accuracy			$0.01V_{\text{C}}$ c	V	See Table 22
AGCout_flag High threshold	$V_{\text{CC}}-0.66$			V	AGF flag set to 1
AGCout_flag Low threshold			$V_{\text{CC}}-0.76$		AGF flag set to 0

Characteristic	Min.	Typ.	Max.	Units	Conditions
IF amplifier					
Supply Current		25		mA	
Frequency range	16		72	MHz	
Input impedance	1.5	2	2.8	k Ω	
			1.5	pF	
Gain (Voltage conversion gain, differential source to maximum load as defined below)	61	66	70	dB	$V_{IFAGC} = 3.0\text{ V}$
	48	57	65	dB	$V_{IFAGC} = 2.2\text{ V}$
	21	25	29	dB	$V_{IFAGC} = 1.2\text{ V}$
	8	17	22	dB	$V_{IFAGC} = 0.5\text{ V}$
Noise Figure		6.3	8.5		$R_s=50\ \Omega$
AGC range	41	48		dB	
AGC control slope	25	31	38	dB/V	$1.2 \leq V_{AGC} \leq 2.2$
AGC input current			50	μA	
Gain variation within channel			0.25	dB	Channel bandwidth 8 MHz within operating frequency range, with maximum load as defined below
OPIP3	130	141		dB μV	Two output tones at 109 dB μV within output channel Gain range = 21 dB to maximum
Output impedance			120	Ω	
Maximum load condition			4.7	k Ω	Differential load
			15	pF	
I²C BUS SDA SCL					
Input high voltage	2.55		5.5	V	
Input low voltage	0		1.4	V	
Input current High			10	μA	$V_{in}=5.5\text{ V}, V_{cc}=5.25\text{ V}$
			10	μA	$V_{in}=5.5\text{ V}, V_{cc}=0\text{ V}$
Input Current Low	-10			μA	$V_{in}=0\text{ V}, V_{cc}=5.25\text{ V}$
Hysteresis		0.4		V	
SDA output voltage			0.4	V	$I_{sink}=3\text{ mA}$
			0.6	V	$I_{sink}=6\text{ mA}$
SCL clock rate			100	kHz	

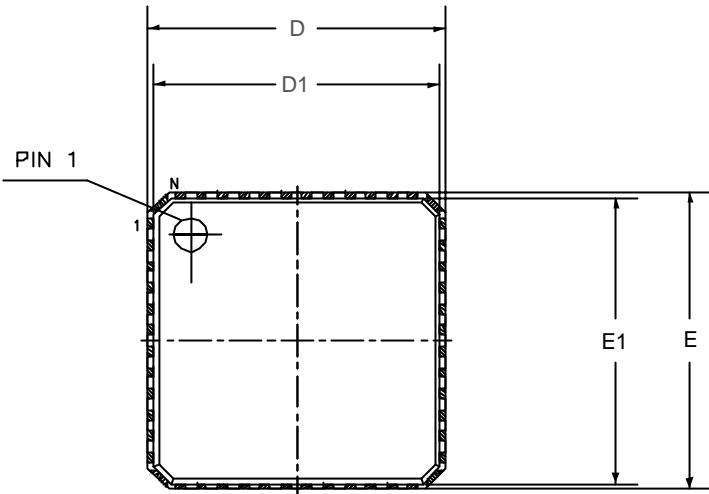
Characteristic	Min.	Typ.	Max.	Units	Conditions
ADD (address) select					See Table 4
Input high current			1	mA	$V_{in}=V_{ccD}$
Input low current			-0.5	mA	$V_{in}=V_{ee}$
PLL Synthesizer					
Charge pump output current					See Table 8 $V_{PUMP}=2\text{ V}$
Charge pump output leakage		+3	± 10	nA	Note 4
Charge pump drive output current	0.5			mA	$V_{DRIVE}=0.7\text{ V}$
Crystal frequency	4		16	MHz	Application as in Figure 13 with 4 MHz crystal
Recommended crystal series ESR	25	70	150	Ω	4 MHz parallel resonant crystal
External reference input frequency	4		20	MHz	Sine wave coupled through 10 nF capacitor
External reference drive level	0.2		2	V_{pp}	Sine wave coupled through 10nF capacitor
		0.5		V_{pp}	Recommended level for optimum phase noise at 4 MHz
Phase detector comparison frequency	31.25		250	kHz	
RF division ratio	240		32767		
Switching ports GPP3-GPP0					
Sink current	10			mA	$V_{port} = 0.4$
Pull up resistor GPP3- GPP1		10		k Ω	
Leakage current			10	μA	$V_{port} = V_{cc}$, Port P0 only

Note 1: 0 dBm =107 dB μ V. All input levels are specified as voltage that would be present if input signal generator was terminated in 50 ohms

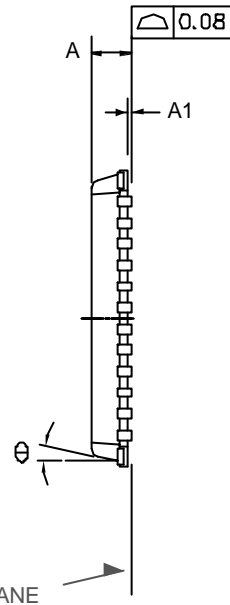
Note 2: Wanted signal (picture carrier) = 101 dBmV at output. Undesired signal (sound carrier) at 5.25 MHz offset modulated with 1 kHz 80% AM. Increase undesired signal to give 1% AM on wanted signal.

Note 3: Wanted signal at 101 dBmV. Unwanted signal at 5.25 MHz offset modulated with 1 kHz 50% AM. Increase undesired signal to give 1.5 kHz FM on wanted signal

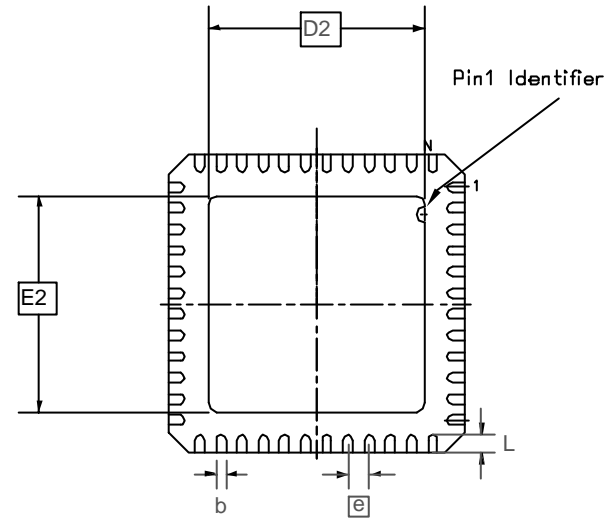
Note 4: Current into PUMP pin with 20 μA current from DRIVE pin



TOP VIEW



SEATING PLANE



BOTTOM VIEW

SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.800	0.850	0.900
A1	0.005	0.025	0.045
b	0.180	0.230	0.300
D	6.900	7.000	7.100
D1	6.650	6.750	6.850
D2	5.10 BSC		
E	6.900	7.000	7.100
E1	6.650	6.750	6.850
E2	5.10 BSC		
N	48		
Nd	12		
Ne	12		
Ⓛ	0.50 BSC		
L	0.300	0.400	0.500
⊖	10°	11°	12°

Conforms to JEDEC MQ-220

- NOTES:
1. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
 2. N IS THE NUMBER OF TERMINALS.
Nd & Ne ARE THE NUMBER OF TERMINALS IN X & Y DIRECTION RESPECTIVELY.
 3. ALL DIMENSIONS ARE IN MILLIMETERS.
 4. LEAD COUNT IS 48
 5. PACKAGE WARPAGE MAX 0.08mm.
 6. NOT TO SCALE.

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ISSUE	1			
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DATE	25-02-2004			
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Previous package codes

Package Code LD

Package Outline for 48 lead QFN (7 x 7 x 0.85mm)

103587



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