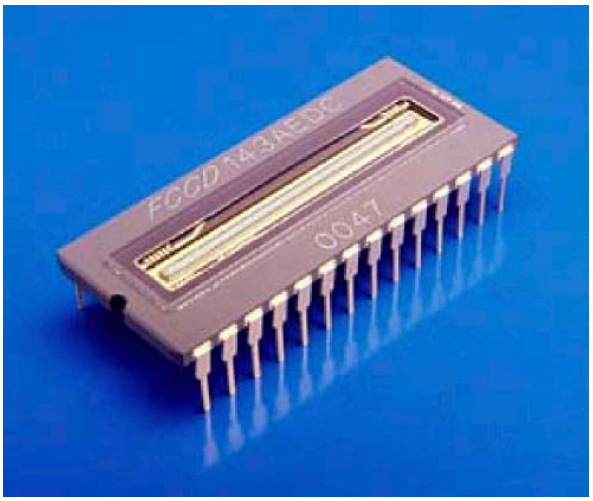
CCD 143A
2048-Element
High Speed Linear Image Sensor

FEATURES

- **2048 x 1 photosite array**
- **13µm x 13µm photosites on 13µm pitch**
- **High speed = up to 20MHz data rates**
- **Enhanced spectral response**
- **Low dark signal**
- **High responsivity**
- **On-chip clock drivers**
- **Dynamic range typical: 7500:1**
- **Over 1V peak-to-peak outputs**
- **Optional facility for correlated double sampling**
- **Dark and white references contained in sample-and-hold outputs**
- **RoHS Compliant**
- **Special selections available - consult factory**



GENERAL DESCRIPTION

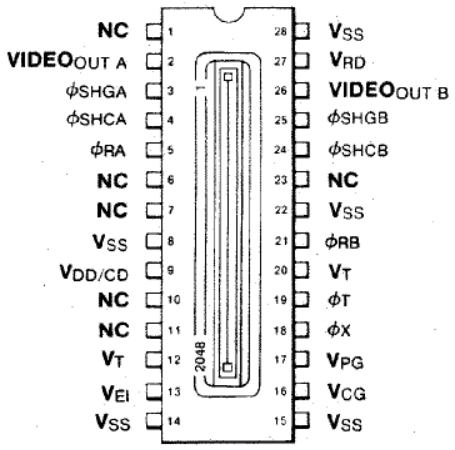
The CCD143A is a 2048-element line image sensor. The charge-coupled device is designed for page scanning applications including facsimile, optical character recognition, and other imaging applications which require high resolution, high sensitivity, and high data rates.

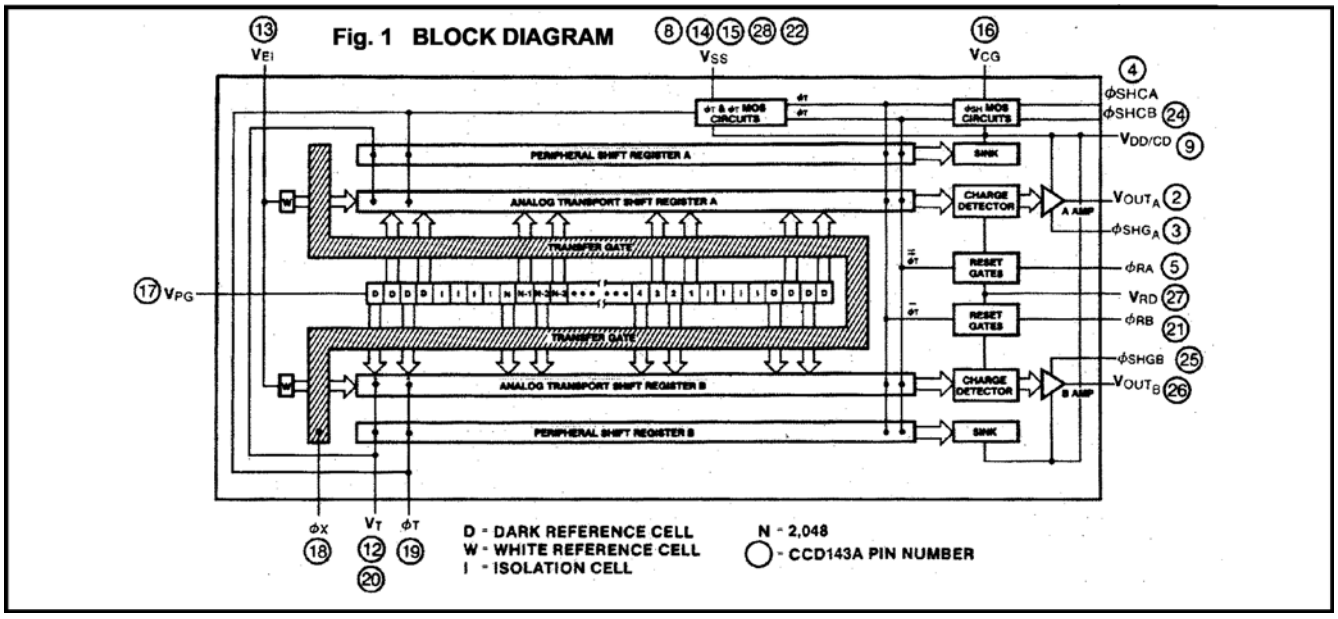
The 2048 sensing elements of the CCD143A give an 8-line per millimeter resolution across a 256-millimeter page adopted as the Japanese facsimile standard.

The CCD143A is a second generation device having an overall improved performance compared with the first generation devices including higher sensitivity, an enhanced blue response and a lower dark signal. The device also incorporates on-chip clock driver circuitry and the option of using external reset clocks for the purpose of Correlated Double Sampling. These high speed devices can be operated at up to 20 MHz data rate. The photoelement size is 13µm (0.51 mils) by 13µm (0.51 mils) on 13µm (0.51 mils) centers. The devices are manufactured using Fairchild Imaging advanced charge-coupled device n-channel Isoplanar buried-channel technology.

PIN NAMES	DESCRIPTION
V_{PG}	Photogate
ϕX	Transfer Clock
ϕT	Transport Clock
$VIDEO_{OUT\ A}$	Output Amplifier A Source
$VIDEO_{OUT\ B}$	Output Amplifier B Source
V_{DD}	Output Amplifier Drain
V_{CG}	Sample-and-Hold Clock Ground
V_{RD}	Reset Transistor Drain
V_{EI}	Electrical Input Bias
V_T	Analog Transport Shift Register DC Electrode
$\phi SHGA$	Sample-and-Hold Gate A
$\phi SHCA$	Sample-and-Hold Clock A
$\phi SHGB$	Sample-and-Hold Gate B
$\phi SHCB$	Sample-and-Hold Clock B
ϕRA	Reset Clock A
ϕRB	Reset Clock B
VSS	Substrate (GND)
NC	No Connection (Do not ground)

PIN CONNECTION DIAGRAM
(TOP VIEW)





FUNCTIONAL DESCRIPTION

The CCD143 consists of the following functional elements illustrated in the Block Diagram:

Image Sensor Elements — These are elements of a line of 2048 image sensors separated by diffused channel stops and covered by a silicon dioxide surface passivation layer. Image photons pass through the transparent silicon dioxide layer and are absorbed in the single crystal silicon creating hole-electron pairs. The photon generated electrons are accumulated in the photosites. The amount of charge accumulated in each photosite is a linear function of the incident illumination intensity and the integration period. The output signal will vary in an analog manner from a thermally generated noise background at zero illumination to a maximum at saturation under bright illumination.

Transfer Gates — This gate is a structure adjacent to the line of image sensor elements. The charge packets accumulated in the image sensor elements are transferred out via the transfer gate to the transport registers whenever the transfer gate goes HIGH. Alternate charge-packets are transferred to the analog transport shift registers. The transfer gate also controls the exposure time for the sensing elements.

Four 1041-Bit Analog Transport Shift Registers — Two registers are on each side of the line of image sensor elements and are separated from it by the transfer gate. The two inside registers, called the transport shift registers, are used to move the image generated charge packets delivered by the transfer gates serially to the two charge-detector/amplifiers. The complementary phase relationship of the last elements of the two transport registers provides for alternate delivery of charge-packets to the amplifiers so that the original serial sequence of the line of video may be reestablished at the outputs. The outer two registers serve to reduce peripheral electron noise in the inner shift registers.

Two Gated Charge-Detector/Amplifiers — From the end of each transport shift register, charge-packets are delivered to a precharge diode whose potential changes linearly in response to the quantity of the signal charge delivered. This potential is applied to the gate of an n-channel MOS transistor producing a signal which passes through the sample-and-hold gate to the output at "$Video_{out}$". The sample-and-hold gate is a switching MOS transistor in the output amplifier that allows the output to be delivered as a sample-and-hold waveform. The diode is recharged internally before the arrival of each new signal charge-packet from the transport shift register.

Clock Driver Circuitry — This circuitry allows operation of the CCD143A using only two external clocks, (1) a square wave transport clock which controls the readout rate of video data from the sensor, and (2) a transfer clock pulse which controls the integration time of the sensor.

Dark and Optional White Reference Circuitry — Four additional sensing elements at both ends of the 2048 array are covered by opaque metallization. They provide a dark (no illumination) signal reference which is delivered at both ends of the line of video output representing the 2048 illuminated sensor elements (labeled "D" in the Block Diagram). Also included at one end of the 2048 sensor element array is a white signal reference in the output signal (labeled "W" in the Block Diagram). These reference levels are useful as inputs to external dc restoration and automatic gain control circuitry. The white reference signal can be enabled by connecting V_{EI} to a DC voltage less than V_{DD}. A V_{EI} voltage of 6V will typically produce a white reference signal of 80=20% of the saturation output voltage.

DEFINITION OF TERMS

Charge-Coupled Device — A charge-coupled device is a semiconductor device in which finite isolated charge-packets are transported from one position in the semiconductor to an adjacent position by sequential clocking of an array of gates. The charge-packets are minority carriers with respect to the semiconductor substrate.

Transfer Clock x — The transfer clock is the voltage waveform applied to the transfer gate to move the accumulated charge from the image sensor elements to the CCD transport shift registers.

Transport Clock T **—** The transport clock is the clock applied to the gates of the CCD transport shift registers to move the charge-packets received from the image sensor elements to the gate charge-detector/amplifiers.

Gate Charge-Detector/Amplifier — These are the output circuits of the CCD143A which receive the charge packets from the CCD transport shift registers and provide a signal voltage proportional to the size of each charge-packet received. Before each new charge-packet is sensed, an internal reset clock returns the charge-detector voltages to a fixed base level.

Sample-and-Hold Clock SHC — This is an internally or externally supplied voltage waveform applied to the sample-and-hold gate in the amplifiers to create a continuous sampled video signal at the output. On-chip sample-and-hold operation is achieved by connecting SHGA to SHCA and SHGB to SHCB.

If the internal (on chip) sample-and-hold clocks are not used, the on-chip sample-and-hold clock driver circuits can be depowered, which greatly reduces on-chip power consumption. To disable (turn off) these drivers, V_{GG} is tied to V_{DD}/V_{CD}. The on-chip SH clock drivers are enabled by connecting V_{CG} to V_{SS}.

Optional External Reset Clocks RA and RB — Dynamic Range and S/N Ratio may be maximized by double-correlated sampling off-chip of the device output. This requires externally-supplied reset clocks for the on-chip amplifiers. Pins 5 and 21 are RA and RB, respectively. If this feature is not desired, both pins should be tied to V_{CD}/V_{DD}, which enables the internally generated reset circuits.

Dark Reference — Video output level generated from sensing elements covered with opaque metallization provides a reference voltage equivalent to device operation in the dark. This permits use of external dc restoration circuitry.

White Reference — Video output level generated by on-chip circuitry provides a reference voltage permitting external automatic gain control circuitry to be used. The reference voltage is produced by charge-injection under the control of the electrical input bias voltage (V_{EI}). The amplitude of the reference is typically 80% of the saturation output voltage.

Isolation Cell — This is a site on-chip producing an element in the video output that serves as a buffer between valid video data and dark reference signals. The output from an isolation cell contains no valid video information and should be ignored.

Dynamic Range — The dynamic range is the saturation exposure divided by the peak-to-peak noise equivalent exposure. (This does not take into account any dark signal components.) Dynamic range is sometimes defined in terms of rms noise. To compare the two definitions a factor of four to six is generally appropriate in that peak-to-peak noise is approximately equal to four to six times rms noise.

Peak-to-Peak Noise Equivalent Exposure — This is the exposure level which gives an output signal equal to the peak-to-peak noise level at the output in the dark.

Saturation Exposure — Saturation exposure is the minimum exposure level that will produce a saturated output signal. Exposure is equal to the light intensity times the photosite integration time.

Charge Transfer Efficiency — This is the percentage of valid charge information that is transferred between each successive stage of the transport registers.

Spectral Response Range — This is the spectral band in which the response per unit of radiant power is more than 10% of the peak response.

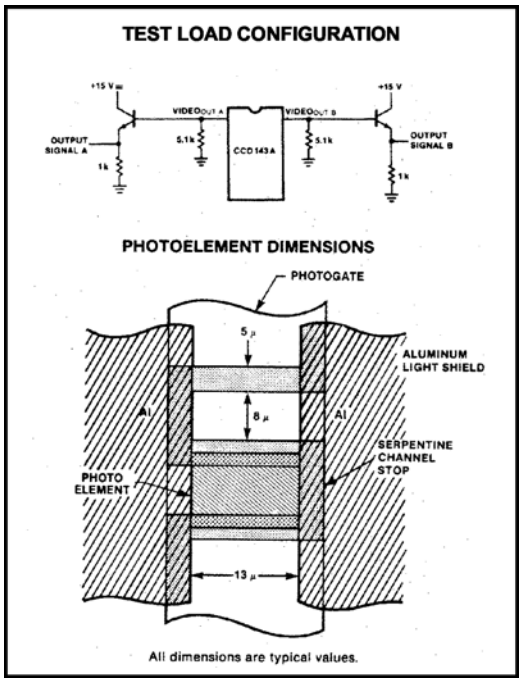
Responsivity — Responsivity is the output signal voltage per unit exposure for a specified spectral type of radiation. Responsivity equals output voltage divided by exposure level.

Dark Signal — This is the output signal in the dark caused by thermally generated electrons which is a linear function of integration time and highly sensitive to temperature. (See accompanying photos for details of definition.)

Total Photoresponse Non-Uniformity — This is the difference in the response levels between the most and least sensitive elements under uniform illumination. (See accompanying photos for details of definition.)

Integration Time — The time interval between the falling edges of any two successive transfer pulses X is the integration time shown in the Timing Diagram. The integration time is the time allowed for the photosites to collect charge.

Pixel — Picture element (photosite).



ABSOLUTE MAXIMUM RATINGS (Above which useful life may be impaired)

Storage Temperature	−25°C to +125°C
Operating Temperature (See curves)	−25°C to +70°C
CCD143A Pins 3, 4, 5, 9, 12, 13, 17, 18, 19, 20, 21, 24, 25, 27, 22.	−0.3V to 18V
Pins14, 15, 16, 28, 8.	0V
Pins 1, 6, 7, 11, 23.	NC
Pins 2, 26.	See Caution Note

CAUTION NOTE: These devices have limited built-in gate protection. It is recommended that static discharge be controlled and minimized. Care must be taken to avoid shorting pins $VIDEO_{OUT}$ A&B to V_{SS} or V_{DD} during operation of the devices. Shorting these pins temporarily to V_{SS} or V_{DD} may destroy the output amplifiers.

DC CHARACTERISTICS: $T_P = 25°C$ (Notes 1, 2)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V_{DD/CD}$	Amplifier & Clock Drain Supply Voltage	13.5	14	14.5	V	Note 3
$I_{CD/DD}$	Amplifier & Clock Drain Supply Current		22	40	mA	
V_{PG}	Photogate Bias Voltage	8.5	9.0	9.5	V	
V_T	DC Electrode Bias Voltage	5.5	6.0	6.5	V	Note 4
V_{EI}	Electrical Input Bias Voltage		V_{DD}		V	Note 5
V_{SS}	Substrate (Ground)		0.0		V	
V_{RD}	Reset Transistor Drain	12.0	12.5	13.0	V	

CLOCK CHARACTERISTICS: $T_P = 25°C$ (Note 1)

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
$V_{\phi RAL}$, $V_{\phi RBL}$	Optional External Reset Clock LOW	0.0	0.3	0.7		
$V_{\phi RA}$, $V_{\phi RB}$	Optional External Reset Clock HIGH	11	11.5	12	V	Note 22
$V_{\phi XL}$, $V_{\phi TL}$	Transfer & Transport Clock LOW	0.0	0.3	0.7	V	Notes 6, 7
$V_{\phi XH}$, $V_{\phi TH}$	Transfer & Transport Clock HIGH	11	11.5	12	V	Note 7
$f_{DATA\ MAX}$	Maximum Output Data Rate	12	20		MHz	Notes 8, 9

NOTES:

1. T_P is defined as the package temperature, measured on a copper block in good thermal contact with the backside of the device.
2. All V_{SS} pins must be grounded. All V_{DD} pins must be connected and tied to V_{CD}. All NC pins must be left unconnected.
3. $V_{DD} = V_{CD}$.
4. $V_T = 0.55\ V_{\phi XH} = 0.55\ V_{\phi TH}$.
5. White reference signal can be enabled by connecting V_{EI} to a voltage less than V_{DD}. $V_{EI} = 6V$ will typically produce a white reference signal of 80±20% of the saturation output voltage.
6. Negative transients on any clock pin going below 0.0V may cause charge-injection which results in an increase in apparent DS. (See "Charge Injection").
7. $C_{\phi T}$ = 700 pF for CCD143A, $C_{\phi X}$ = 300 pF for CCD143A.
8. Minimum clock frequency is limited by increase in dark signal.
9. $f_{DATA} = 2 \times f\ \phi_T$.
10. Dynamic range is defined as V_{SAT}/peak-to-peak temporal noise or V_{SAT}/rms temporal noise.
11. 1 $\mu j/cm^2 = 0.02\ f_{CS}$ at 2854°K, 1 $f_{CS} = 50\ \mu j/cm^2$ at 2854°K.
12. SE for 2854°K broadband light without 2.0 mm Schott BG-38 and OCLI WBHM filters is typically 0.8 $\mu j/cm^2$.
13. CTE is the measurement for a one-stage transfer.
14. See photographs for PRNU definitions.
15. Video mismatch is the difference in ac amplitudes between $VIDEO_{OUTA}$ and $VIDEO_{OUTB}$ under uniform illumination. It can be eliminated by attenuation/amplification of one of the video outputs.
16. DC mismatch is the difference in dc output level (V_O) between $VIDEO_{OUTA}$ and $VIDEO_{OUTB}$.
17. See photographs for DS definitions.
18. Dark signal component approximately doubles for every 5°C increase in T_P.
19. Each SPDSNU is measured from the DS level adjacent to the base of the SPDSNU. The SPDSNU approximately doubles for every 8°C increase in T_P.
20. Responsivity for 2854°K broadband light source without 2.0 mm Schott BG-38 and OCLI WBHM filters is typically 2 V per $\mu j/cm^2$.
21. See test load configurations.
22. Internal reset of the gated charge detector is achieved by connecting ϕ_{RA} and ϕ_{RB} to V_{DD}.

AC CHARACTERISTICS: (Note 1)
T_P = 25° C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms, Light Source* = 2854° K + 2.0 mm thick
Schott BG-38 and OCLI WBHM filters
All operating voltages nominal specified values

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
DR	Dynamic Range (relative to peak-to-peak noise) (relative to rms noise)		1500:1 7500:1			Note 10
NEE	RMS Noise Equivalent Exposure		0.00009		$\mu j/cm^2$	Note 11
SE	Saturation Exposure		0.67		$\mu j/cm^2$	Note 12
CTE	Charge Transfer Efficiency	0.99995	0.99999			Note 13
V_O	Output DC Level	4.0	8.0	11.0	V	
Z	Output Impedance		0.75	1.5	kΩ	
P	On-Chip Power Dissipation Clock Drivers Amplifiers		 100 170	 215 325	 mW mW	
N	Peak-to-Peak Temporal Noise		1.0		mV	

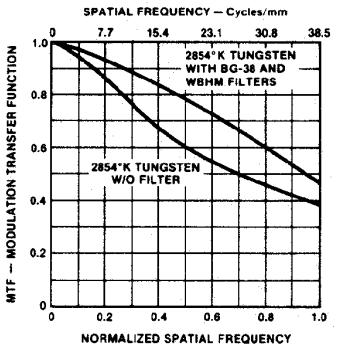
PERFORMANCE CHARACTERISTICS: (Note 1)
T_P = 25° C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms, Light Source* = 2854° K + 2.0 mm thick
Schott BG-38 and OCLI WBHM filters
All operating voltages nominal specified values

SYMBOL	CHARACTERISTIC	RANGE			UNITS	CONDITIONS
		MIN	TYP	MAX		
PRNU**	Photoresponse Non-Uniformity:					Note 14
	Peak-to-Peak		60	160	mV	
	Peak-to-Peak Without Single-Pixel Positive & Negative Pulses		40		mV	
	Single-Pixel Positive Pulses		10		mV	
	Single-Pixel Negative Pulses		20		mV	
M_{VIDEO}	Video Mismatch		10	100	mV	Note 15
M_{DC}	DC Mismatch		0.5	2.0	V	Note 16
DS	Dark Signal:					Notes 17, 18
	DC Component		1.0	2.0	mV	
	Low Frequency Component		1.0	2.0	mV	
SPDSNU	Single-Pixel DS Non-Uniformity		1.0	2.0	mV	Notes 17, 19
R	Responsivity	1.8	3.0	5.5	Volts per $\mu j/cm^2$	Note 20
V_{SAT}	Saturation Output Voltage	1.0	2.0	2.5	V	Note 21

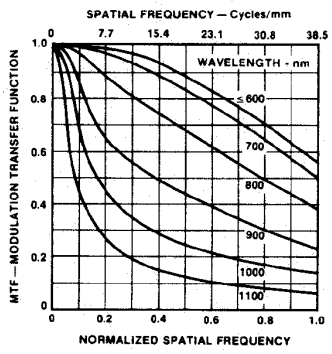
* OCLI WBHM = Optical Coating Laboratory, Inc. Wide Band Hot Mirror
** PRNU measurements include both register outputs but exclude the outputs from the first and last elements of the array. Also excluded from the measurement are video and dc mismatch.
All PRNU measurements are taken at a 800 mV output level using an f/5.0 lens.
The "f" number is defined as the distance from the lens to the array divided by the diameter of the lens aperture. As the "f" number increases, the resulting more highly collimated light causes the package window imperfections to dominate and increase PRNU. A lower "f" number results in less collimated light causing device photosite blemishes to dominate the PRNU.

TYPICAL PERFORMANCE CURVES

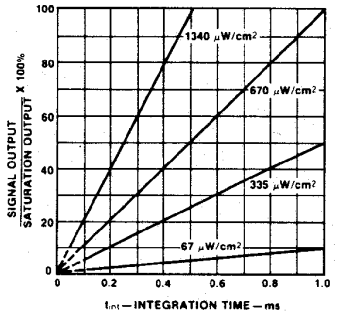
MODULATION TRANSFER FUNCTIONS FOR TWO BROADBAND ILLUMINATION SOURCES



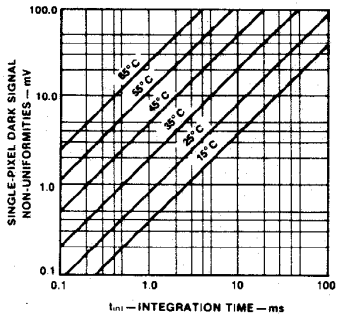
MODULATION TRANSFER FUNCTIONS FOR NARROW BAND ILLUMINATION SOURCES



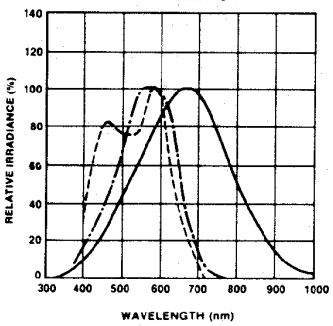
OUTPUT SIGNAL LEVEL VERSUS INTEGRATION TIME 2854°K TUNGSTEN SOURCE WITH BG-38 AND WBHM FILTERS



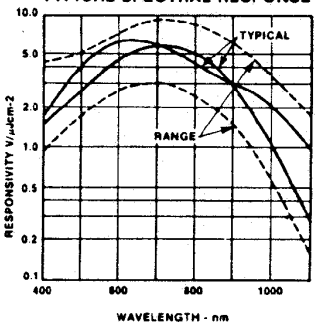
SINGLE-PIXEL DARK SIGNAL NON-UNIFORMITIES VERSUS INTEGRATION TIME



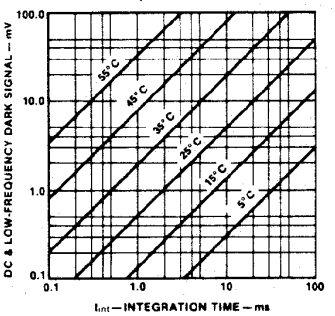
*RELATIVE RADIANT FLUX VS WAVELENGTH



TYPICAL SPECTRAL RESPONSE



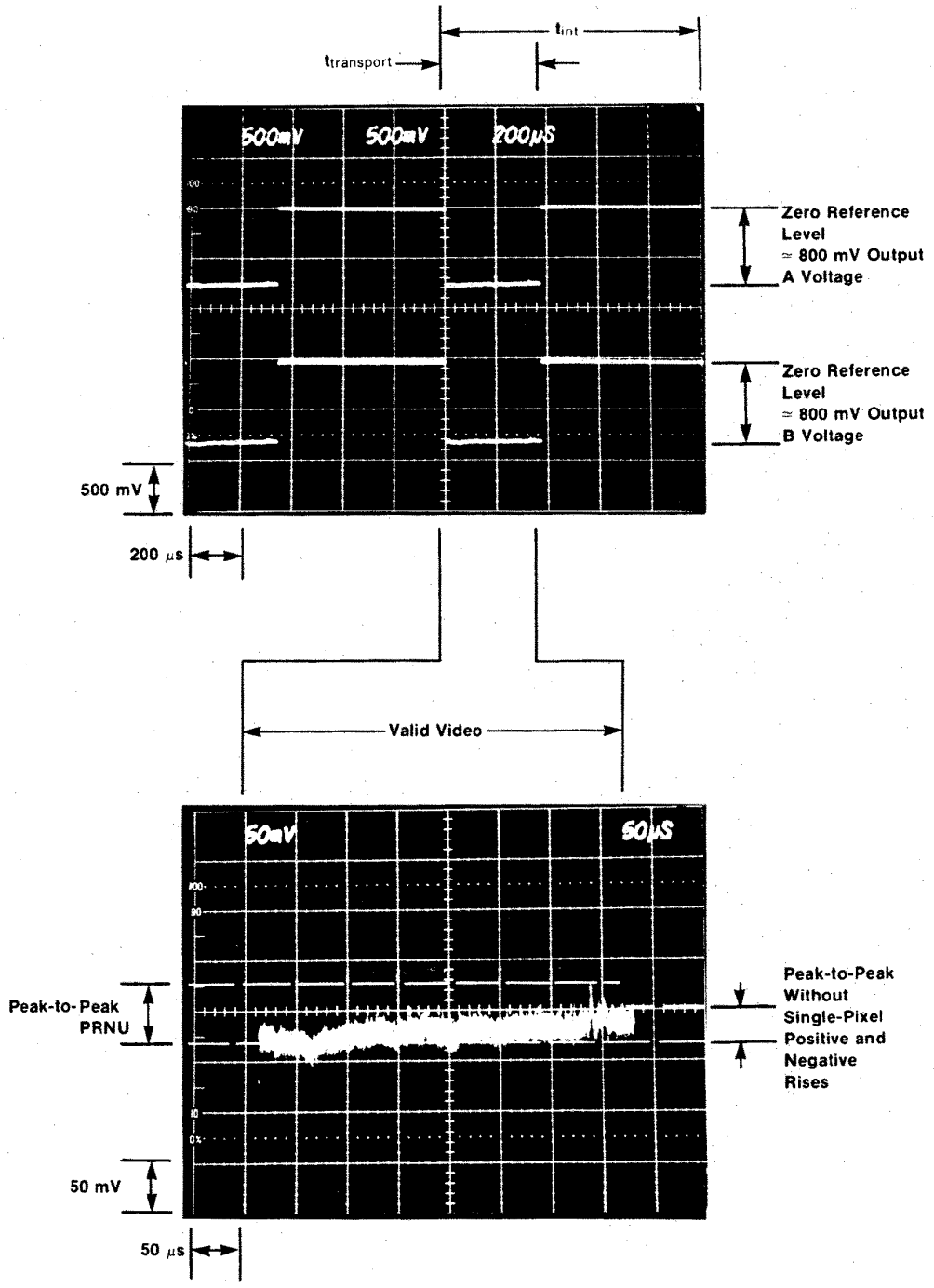
DC AND LOW-FREQUENCY DARK SIGNAL VS INTEGRATION TIME



TYPICAL "DAYLIGHT FLUORESCENT" BULB
2854°K LIGHT SOURCE +WBHM + 2.0 mm THICK BG-38
2854°K LIGHT SOURCE + 3.0 mm THICK 1-75

CCD143A

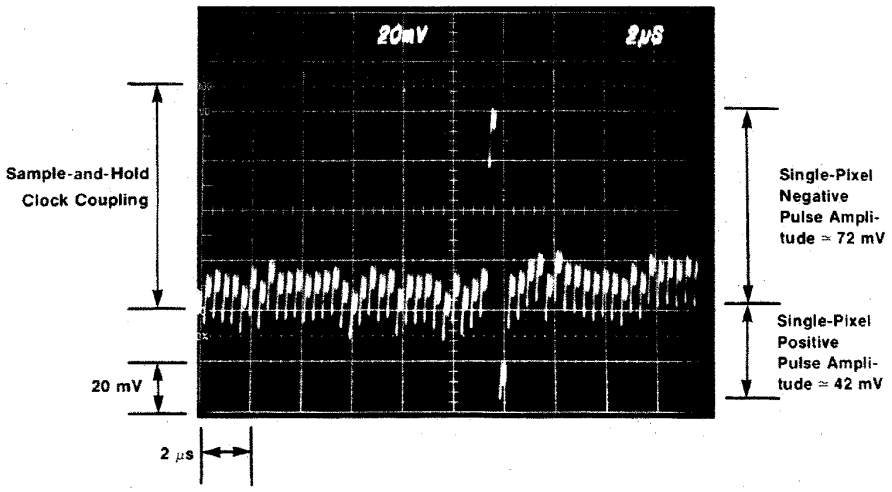
PHOTORESPONSE NON-UNIFORMITY PARAMENTERS (PRNU)



TEST CONDITIONS

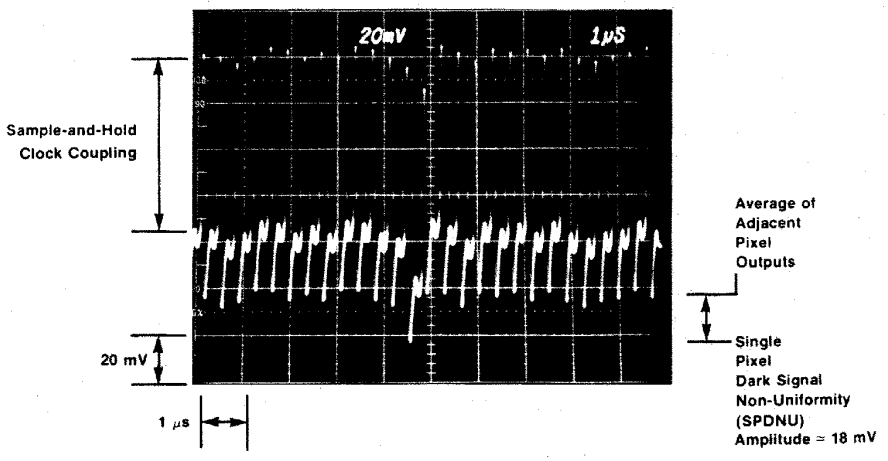
T_P = +25° C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854° K tungsten = 2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of ≃ 800 mV. Output fed through 5 MHz low pass filter.

PHOTORESPONSE NON-UNIFORMITY PARAMETERS (PRNU)



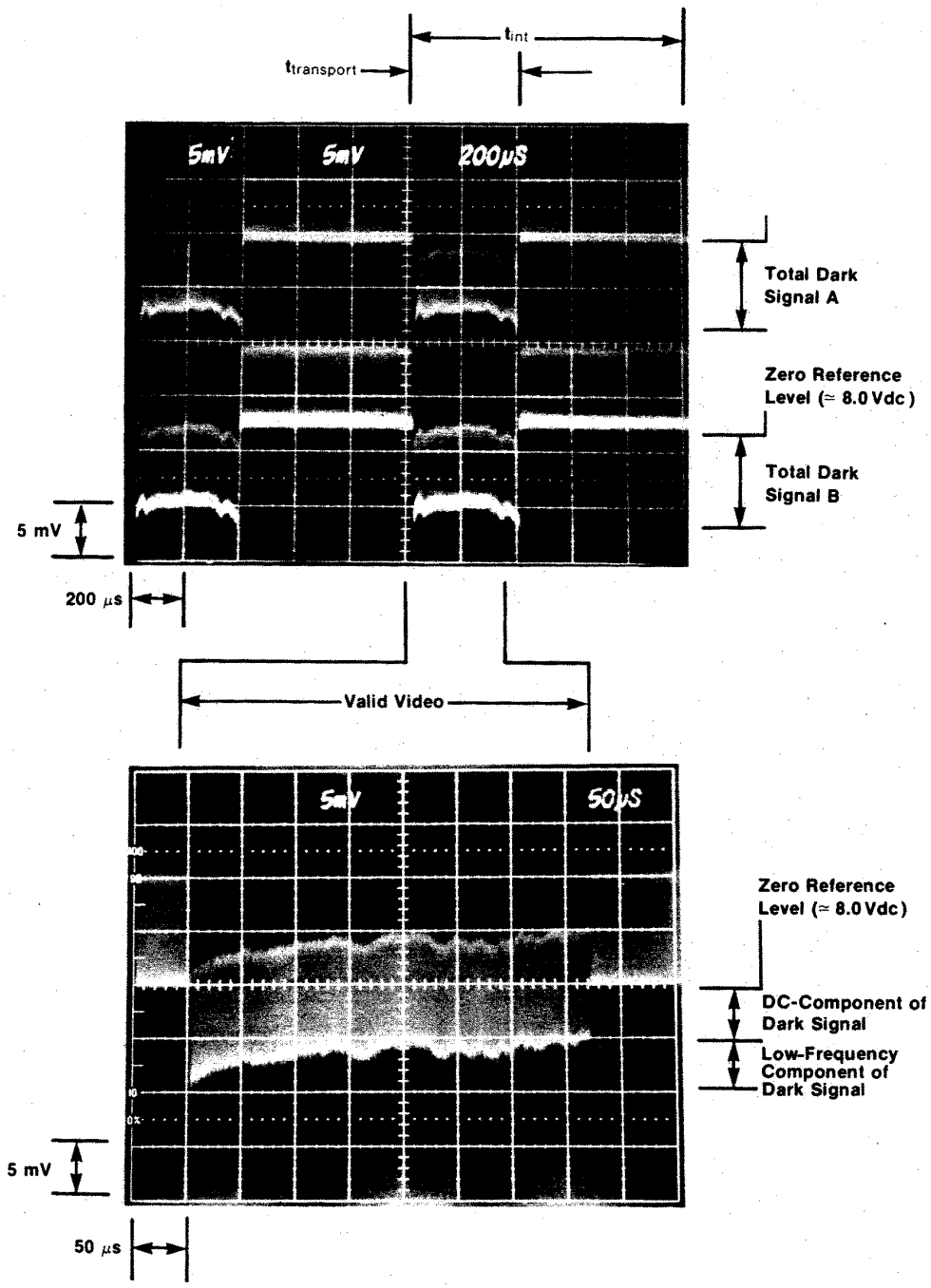
TEST CONDITIONS
T_P = +25°C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854°K tungsten +2.0 mm thick Schott BG-38 and OCLI WBHM filters. PRNU measurements taken at an output voltage of ≃ 800 mV. Output fed through 5 MHz low pass filter.

DARK SIGNAL PARAMETERS (DS)



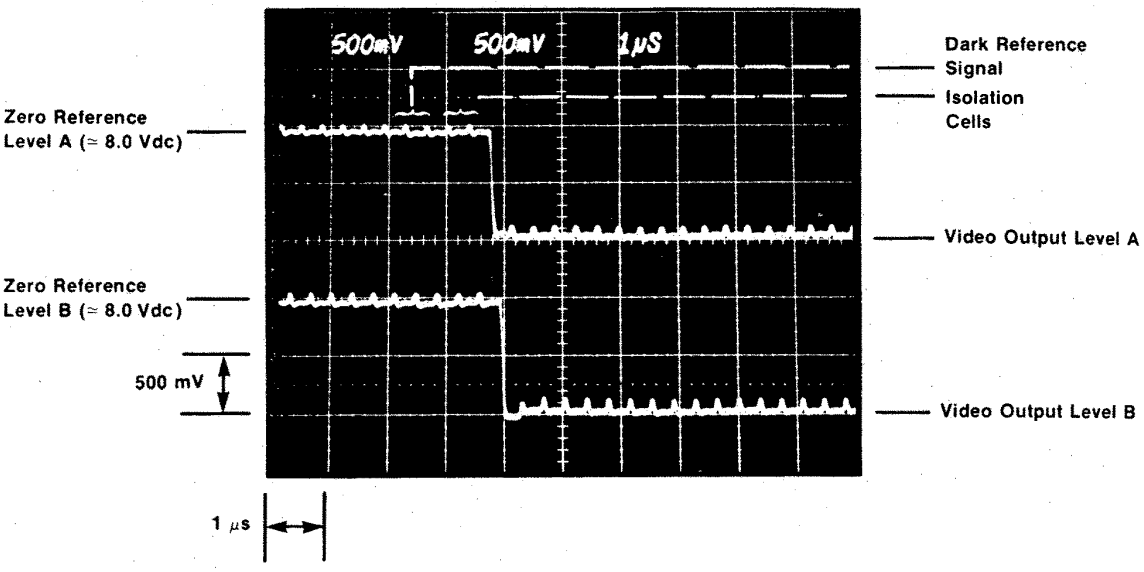
TEST CONDITIONS
Tp = +25° C, fDATA = 5.0 MHz, tint = 1.0 ms. All voltages nominal specified values. Output fed through 5MHz low pass filter.

DARK SIGNAL PARAMETERS (DS)



TEST CONDITIONS
T_P = +25° C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Output fed through 5 MHz low pass filter.

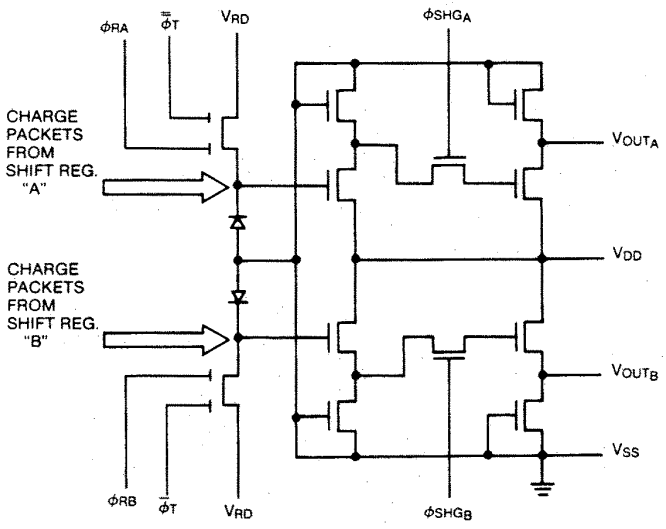
VIDEO OUTPUT TIMING PHOTOGRAPHS



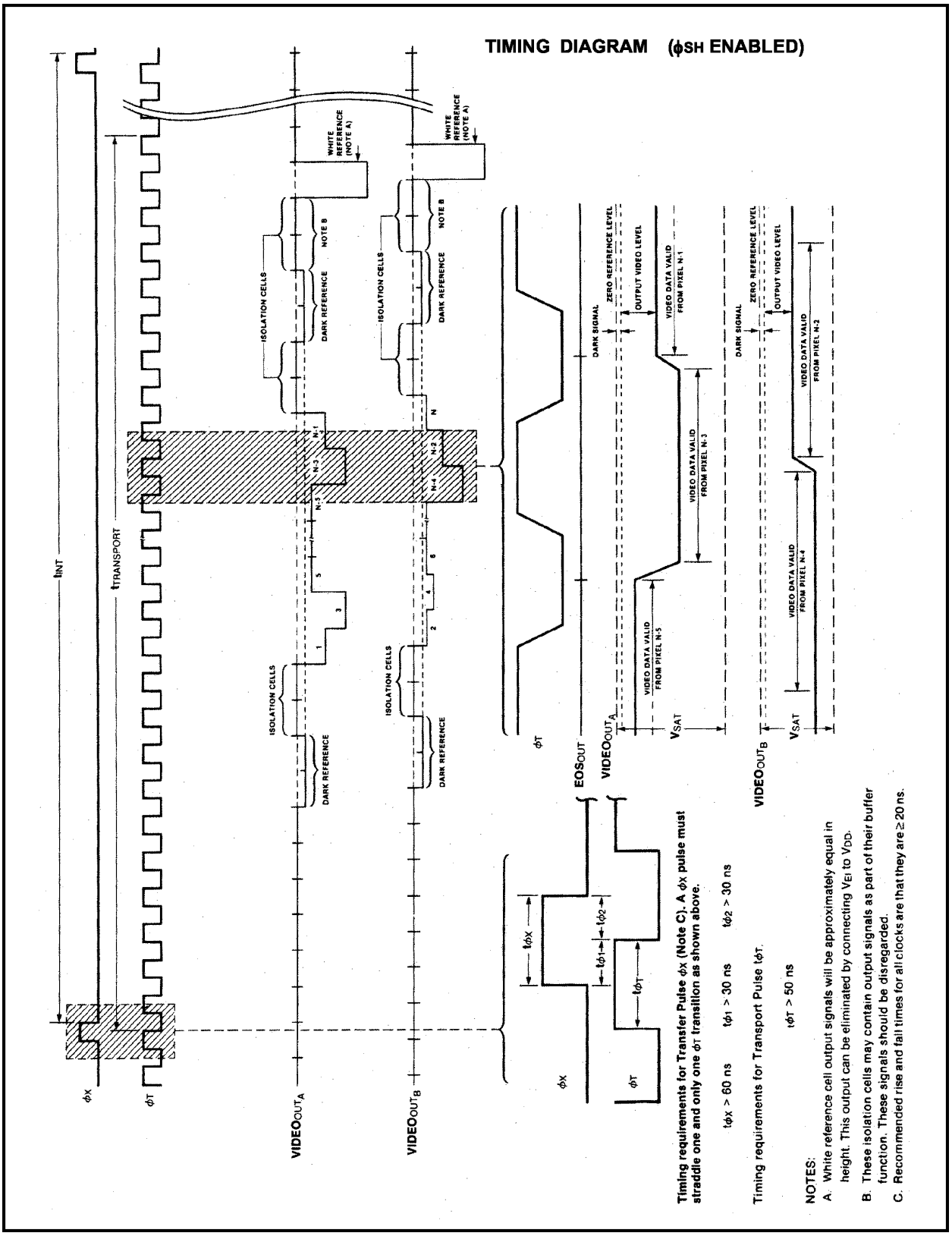
Start of One Scan Video Output

TEST CONDITIONS
T_P = +25° C, f_{DATA} = 5.0 MHz, t_{int} = 1.0 ms. All voltages nominal specified values. Light source = 2854° K tungsten = 2.0 mm thick Schott BG-38 and OCLI WBHM filters. Output fed through 5 MHz low pass filter.

OUTPUT AMPLIFIER SCHEMATIC



NOTE: $\bar{\phi}_T$ AND $\bar{\bar{\phi}}_T$ ARE INTERNALLY GENERATED RESET CLOCKS.


TIMING DIAGRAM (ϕSH ENABLED)
tINT
tTRANSPORT
ϕX
ϕT
VIDEOOUTA
VIDEOOUTB
WHITE REFERENCE (NOTE A)
ISOLATION CELLS
DARK REFERENCE
NOTE B
N-1
N-3
N-5
N
N-2
N-4
1
2
3
4
5
6
EOSOUT
DARK SIGNAL
ZERO REFERENCE LEVEL
OUTPUT VIDEO LEVEL
VIDEO DATA VALID FROM PIXEL N-5
VIDEO DATA VALID FROM PIXEL N-3
VIDEO DATA VALID FROM PIXEL N-1
VIDEO DATA VALID FROM PIXEL N-4
VIDEO DATA VALID FROM PIXEL N-2
VSAT
tϕX
tϕ1
tϕ2
tϕT
Timing requirements for Transfer Pulse ϕX (Note C). A ϕX pulse must straddle one and only one ϕT transition as shown above.
tϕX > 60 ns tϕ1 > 30 ns tϕ2 > 30 ns
Timing requirements for Transport Pulse tϕT.
tϕT > 50 ns
NOTES:
A. White reference cell output signals will be approximately equal in height. This output can be eliminated by connecting VEI to VDD.
B. These isolation cells may contain output signals as part of their buffer function. These signals should be disregarded.
C. Recommended rise and fall times for all clocks are that they are ≥ 20 ns.

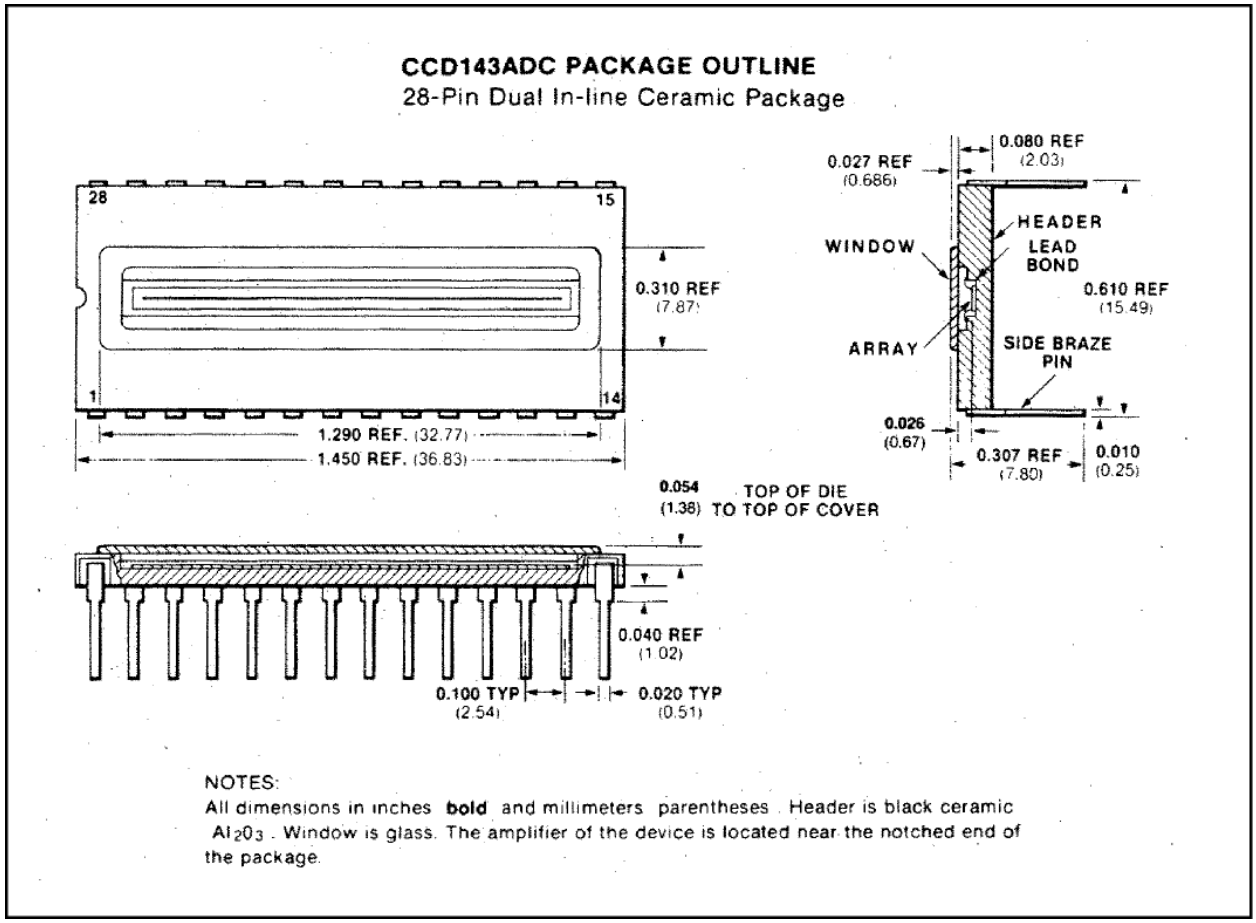
DEVICE CARE AND OPERATION

Glass may be cleaned by saturating a cotton swab in alcohol and lightly wiping the surface. Rinse off the alcohol with deionized water. Allow the glass to dry, preferably by blowing with filtered dry N_2 or air.

It is important to note in design and applications considerations that the devices are very sensitive to thermal conditions. The dark signal dc and low frequency components approximately double for every 5°C temperature increase and single-pixel dark signal non-uniformities approximately double for every 8°C temperature increase. The devices may be cooled to achieve very long integration times and very low light level capability.

ORDER INFORMATION

Order CCD143ADC where “D” stands for a ceramic package and “C” for commercial temperature range.



WARRANTY

Within twelve months of delivery to the end customer, Fairchild Imaging will repair or replace, at our option, any Fairchild Imaging camera product if any part is found to be defective in materials or workmanship. Contact factory for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Fairchild Imaging certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specification under which it is furnished.

This product is designed, manufactured, and distributed utilizing the ISO 9000:2000 Business Management System.