Genesys Logic, Inc.

GL826

USB 2.0 Multi-Slot
Flash Card Reader Controller
(All-in-one with Dual SD/MMC bus Interface)

Datasheet
Revision 1.03
Aug. 2, 2007

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Revision History

Revision	Date	Description
0.90	10/5/2006	Initial version
0.91	1/19/2007	Modify SD/MMC Card Description
1.00	3/12/2007	Modify some pin type and pin name Add AC Characteristics of MS PRO
1.01	4/23/2007	Add serial EEPROM interface, p31 Add description about pin118,119, p10 Modify DC Characteristics: $V_{OH,}$ $I_{OH,}$ $I_{OL,}$ p13
1.02	6/7/2007	Add feature description below, p7: ● Support Dual SD and MS-PRO 4-bit for 5 slots. ● Support MS PRO-HG 8-bit for 4 slots ● Pass Windows Vista and XP Modify Chapter 2: ● Chapter 2.1 LQFP 128 Without MS PRO-HG 8bit support ● Chapter 2.2 LQFP 128 With MS PRO-HG 8bit support ● Chapter 2.3 Comparison Modify Chapter4.8 Modify Chapter4.10
1.03	8/2/2007	Add LQFP48 Pin Package Application

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CHAPTER 1 FEATURES

- USB specification compliance
  - Compliant with Universal Serial Bus specification rev. 2.0.
  - Compliant with USB Mass Storage Class Bulk only Transport Specification rev. 1.0.
  - Supports one USB device address and up to 5 endpoints, including one control, one interrupt and 2 bulk IN / OUT endpoint pairs.
- Integrated USB building blocks
  - USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE), embedded Power-On Reset (POR) and Low-Voltage Detector (LVD)
- Embedded 8051 micro-controller
  - Operate @ 60 MHz clock, 12 clocks per instruction cycle
  - Embedded 64K Byte mask ROM and internal 256 byte SRAM
- Support firmware upgrade to external flash via USB port (ISP : In System Programming)
- Embedded five power switches for power control of five cards interface
  - Programmable over-current detected period is from 1us to 0.64 ms
  - Internal pull-up/pull-down resistance I/O pad controlled by firmware
- On-chip 5V to 3.3V and 3.3V to 1.8V regulators
- On board 12 Mhz Crystal driver circuit
- 128-pin LQFP: Support the following memory card interfaces
  - CompactFlash™ (CF), Microdrive
  - Secure Digital™ (SD), miniSD™, microSD™/TransFlash™
  - MultiMediaCard™ (MMC), MMCplus™, MMCmobile™, MMCmicro™, RS-MMC
  - Memory Stick™ (MS), Memory Stick PRO™ (MS PRO), MS Duo, MS PRO Duo, MS Micro (M2)
  - SmartMedia™ (SM)
  - xD-Picture Card™ Type M/H
- Support CF v4.0 with PIO mode 0-6 and UDMA 0-4 mode
- Support SD and MMC
  - SDHC(SD v2.0) 4-bit
  - MMC v4.2 8-bit
- Support CE-ATA v1.0b (external flash)
- Support Dual SD and MS-PRO 4-bit for 5 slots (CF, SM/xD, SD/MMC 8bit, MS/MSPRO, microSD/ MMCmicro/ T-Flash 4bit)
- Support MS PRO-HG 8-bit for 4 slots (CF, SM/xD, SD/MMC 8bit, MS/MSPRO-HG)
- Support SM v1.00
- Support xD-Picture v1.2C Type M/H (TID:AA-CG0451)
- Two independent SD/MMC interfaces
  - One is SD/MMC 8bit, the other is microSD/ MMCmicro/ T-Flash 4bit
  - Support SD/MMC-to-SD/MMC read/write operations.
- 48-pin LQFP: Support MS PRO-HG 8-bit and SDHC/MMC v4.2 8-bit
- Operating system supported: Windows Vista32&64/XP/2000/Me/98/98SE, Mac OS 9.X/10.X, Linux Kernel 2.4.X/2.6.X
  - Pass Windows Vista32&64 (submission ID:1231473)
  - Pass Windows XP (submission ID: 1231870)
- Support external serial EEPROM interface (8-bit format) for the flexibility to load vender information and system option
- High efficient hardware engine
  - Integrated Fast 8051 microprocessor
  - High efficient DMA hardware engine improves transfer rate between USB and flash card interfaces
- Available in 128-pin LQFP 14x14 mm and 48-pin LQFP green package

CHAPTER 2 PIN ASSIGNMENT

2.1 LQFP 128 Dual SD and MS-PRO 4-bit Support

2.1.1 Pinout Diagram

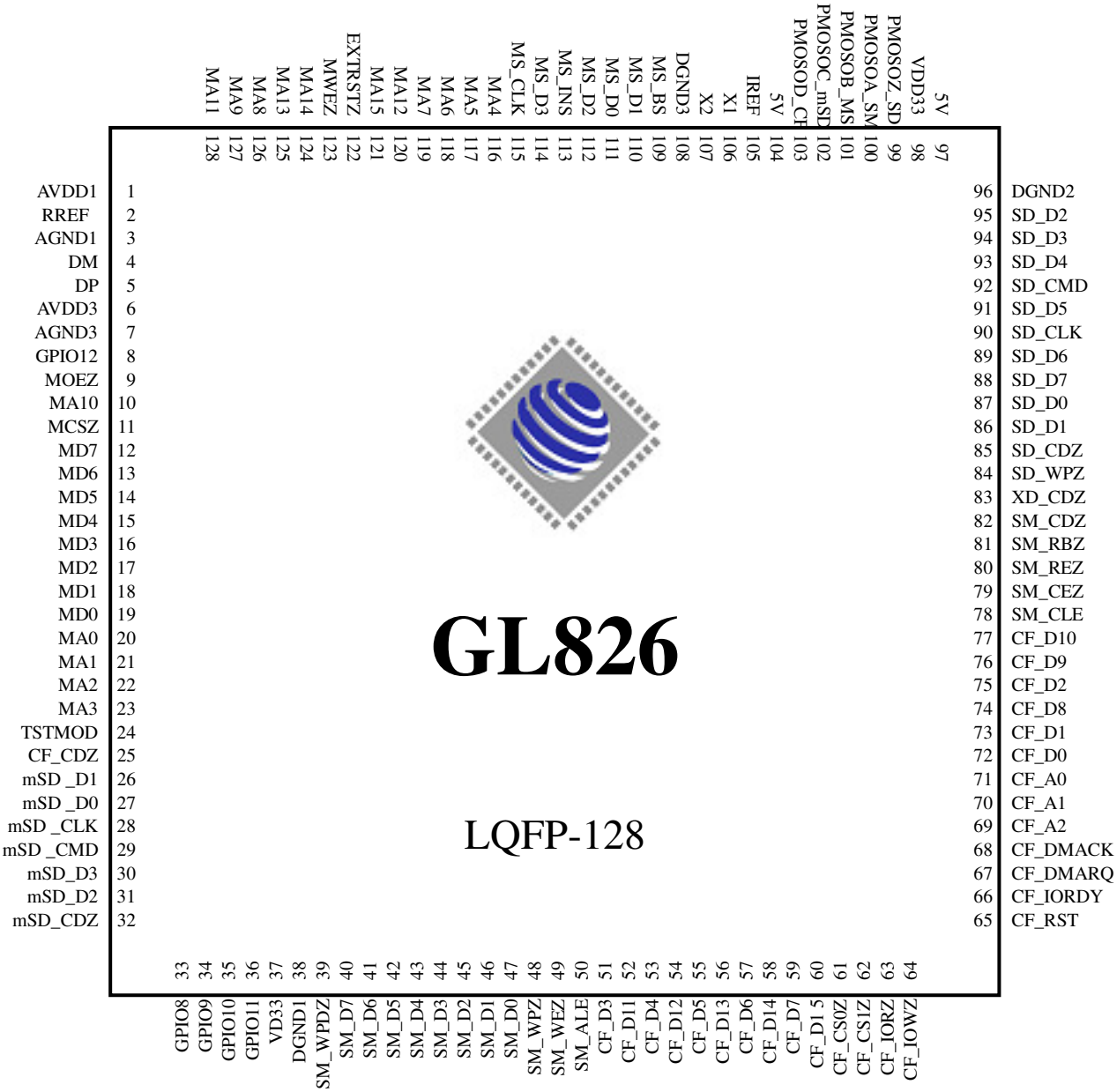


Figure 2.1－LQFP 128 Pinout Diagram(without MS PRO-HG 8-bit support)

2.1.2 Pin List

Table 2.1－Pin List

Pin #	Pin Name	Type	Pin #	Pin Name	Type	Pin #	Pin Name	Type	Pin #	Pin Name	Type
1	AVDD1	P	33	GPIO8	B	65	CF_RST	O	97	5V	P
2	RREF	A	34	GPIO9	B	66	CF_IORDY	I	98	VDD33	P
3	AGND1	P	35	GPIO10	B	67	CF_DMARQ	I	99	PMOSOZ_SD	P
4	DM	A	36	GPIO11	B	68	CF_DMACK	O	100	PMOSOA_SM	P
5	DP	A	37	VDD33	P	69	CF_A2	O	101	PMOSOB_MS	P
6	AVDD3	P	38	DGND1	P	70	CF_A1	O	102	PMOSOC_mSD	P
7	AGND3	P	39	SM_WPDZ	I	71	CF_A0	O	103	PMOSOD_CF	P
8	GPIO12	B	40	SM_D7	B	72	CF_D0	B	104	5V	P
9	MOEZ	B	41	SM_D6	B	73	CF_D1	B	105	IREF	A
10	MA10	B	42	SM_D5	B	74	CF_D8	B	106	X1	I
11	MCSZ	B	43	SM_D4	B	75	CF_D2	B	107	X2	B
12	MD7	B	44	SM_D3	B	76	CF_D9	B	108	DGND3	P
13	MD6	B	45	SM_D2	B	77	CF_D10	B	109	MS_BS	O
14	MD5	B	46	SM_D1	B	78	SM_CLE	O	110	MS_D1	B
15	MD4	B	47	SM_D0	B	79	SM_CEZ	O	111	MS_D0	B
16	MD3	B	48	SM_WPZ	B	80	SM_REZ	O	112	MS_D2	B
17	MD2	B	49	SM_WEZ	O	81	SM_RBZ	I	113	MS_INS	I
18	MD1	B	50	SM_ALE	O	82	SM_CDZ	B	114	MS_D3	B
19	MD0	B	51	CF_D3	B	83	XD_CDZ	I	115	MS_CLK	O
20	MA0	B	52	CF_D11	B	84	SD_WPZ	I	116	MA4	O
21	MA1	B	53	CF_D4	B	85	SD_CDZ	I	117	MA5	O
22	MA2	B	54	CF_D12	B	86	SD_D1	B	118	MA6	O
23	MA3	B	55	CF_D5	B	87	SD_D0	B	119	MA7	O
24	TSTMOD	I	56	CF_D13	B	88	SD_D7	B	120	MA12	O
25	CF_CDZ	I	57	CF_D6	B	89	SD_D6	B	121	MA15	O
26	mSD _D1	B	58	CF_D14	B	90	SD_CLK	O	122	EXTRSTZ	I
27	mSD_D0	B	59	CF_D7	B	91	SD_D5	B	123	MWEZ	O
28	mSD _CLK	O	60	CF_D15	B	92	SD_CMD	B	124	MA14	O
29	mSD _CMD	B	61	CF_CS0Z	O	93	SD_D4	B	125	MA13	O
30	mSD _D3	B	62	CF_CS1Z	O	94	SD_D3	B	126	MA8	O
31	mSD _D2	B	63	CF_IORZ	O	95	SD_D2	B	127	MA9	O
32	mSD _CDZ	I	64	CF_IOWZ	O	96	DGND2	P	128	MA11	O

2.1.3 Pin Description

Table 2.2－Pin Description

Pin Name	Pin #	Type	Description
AVDD1	1	P	Analog power
RREF	2	A	USB Reference resistor
AGND1	3	P	Analog ground
DM	4	A	USB D-
DP	5	A	USB D+
AVDD3	6	P	Analog power
AGND3	7	P	Analog ground
VDD33	37, 98	P	PAD power 3.3V
DGND	38, 96, 108	P	Digital Ground
GPIO	8, 33~36	B	8: Common Access LED 33: SM/xD LED 34: SD/MMC LED 35: MS/MSP LED 36: CF/MD LED
TSTMOD	24	I, pd	Test mode
MCSZ	11	O, pu	External flash chip select
MOEZ	9	O, pu	External flash output enable
MWEZ	123	O, pu	External flash write enable
MA15~0	121~125, 120, 128, 10, 127, 126, 119~116, 23~20	O	External flash address ports
MA6	118	O	Serial EEPROM clock
MA7	119	B, pu	Serial EEPROM data
MD7~0	12~19	B, pd	External flash data ports
mSD _D3~0	30, 31, 26, 27	B, pd	SD2 data ports
mSD _CLK	28	O, pd	SD2 clock
mSD _CMD	29	B, pd	SD2 command port
mSD _CDZ	32	I, pu	SD2 card detect
CF_CDZ	25	I, pu	CF card detect
CF_D15~0	60, 58, 56, 54, 52, 77, 76, 74, 59, 57, 55, 53, 51, 75, 73, 72	B	CF data ports
CF_CS0Z	61	O, pu	CF chip select 0
CF_CS1Z	62	O, pu	CF chip select 1
CF_IORZ	63	O, pu	CF IO read
CF_IOWZ	64	O, pu	CF IO write

CF_RST	65	O, pu	CF reset
CF_IORDY	66	I, pu	CF IO ready
CF_DMARQ	67	I, pd	CF DMA request
CF_DMACK	68	O	CF DMA acknowledge
CF_A2~0	69~71	O	CF address
SM_WPDZ	39	I, pu	SM WP#
SM_D7~0	40~47	B, pd	SM data ports
SM_WPZ	48	B, pu	SM write protect
SM_WEZ	49	O, pu	SM write enable
SM_ALE	50	O, pd	SM_ALE
SM_CLE	78	O, pd	SM command latch enable
SM_CEZ	79	O, pu	SM card enable
SM_REZ	80	O, pu	SM read enable
SM_RBZ	81	I, pu	SM read/busy
SM_CDZ	82	B, pu	SM card detect
XD_CDZ	83	I, pu	XD card detect
SD_WPZ	84	I, pu	SD write protect
SD_CDZ	85	I, pu	SD card detect
SD_D7~0	88, 89, 91, 93 94, 95, 86, 87	B, pd	SD data line
SD_CLK	90	O, pd	SD clock
SD_CMD	92	B	SD command/response
MS_BS	109	O, pd	MS/MSP bus state
MS_INS	113	I, pu	MS insertion detect
MS_D3~0	114, 112, 110, 111	B, pd	MS/MSP data signal
MS_CLK	115	O, pd	MS clock
5V	97, 104	P	5V power input
PMOSOZ_ SD	99	P	SD power 250mA
PMOSOA_SM	100	P	SM power 100mA
PMOSOB_MS	101	P	MS power 100mA
PMOSOC_mSD	102	P	mSD power 100mA
PMOSOD_CF	103	P	CF power 500mA
IREF	105	A	Regulator reference voltage
X1	106	I	XTAL 1
X2	107	B	XTAL 2
EXTRSTZ	122	I, pu	System reset

Notation:

Type **O** Output

I Input

B	Bi-directional
pu	internal pull-up when input
pd	internal pull-down when input
P	Power / Ground
A	Analog

2.2 LQFP 128 With MS PRO-HG 8-bit support

2.2.1 Pinout Diagram

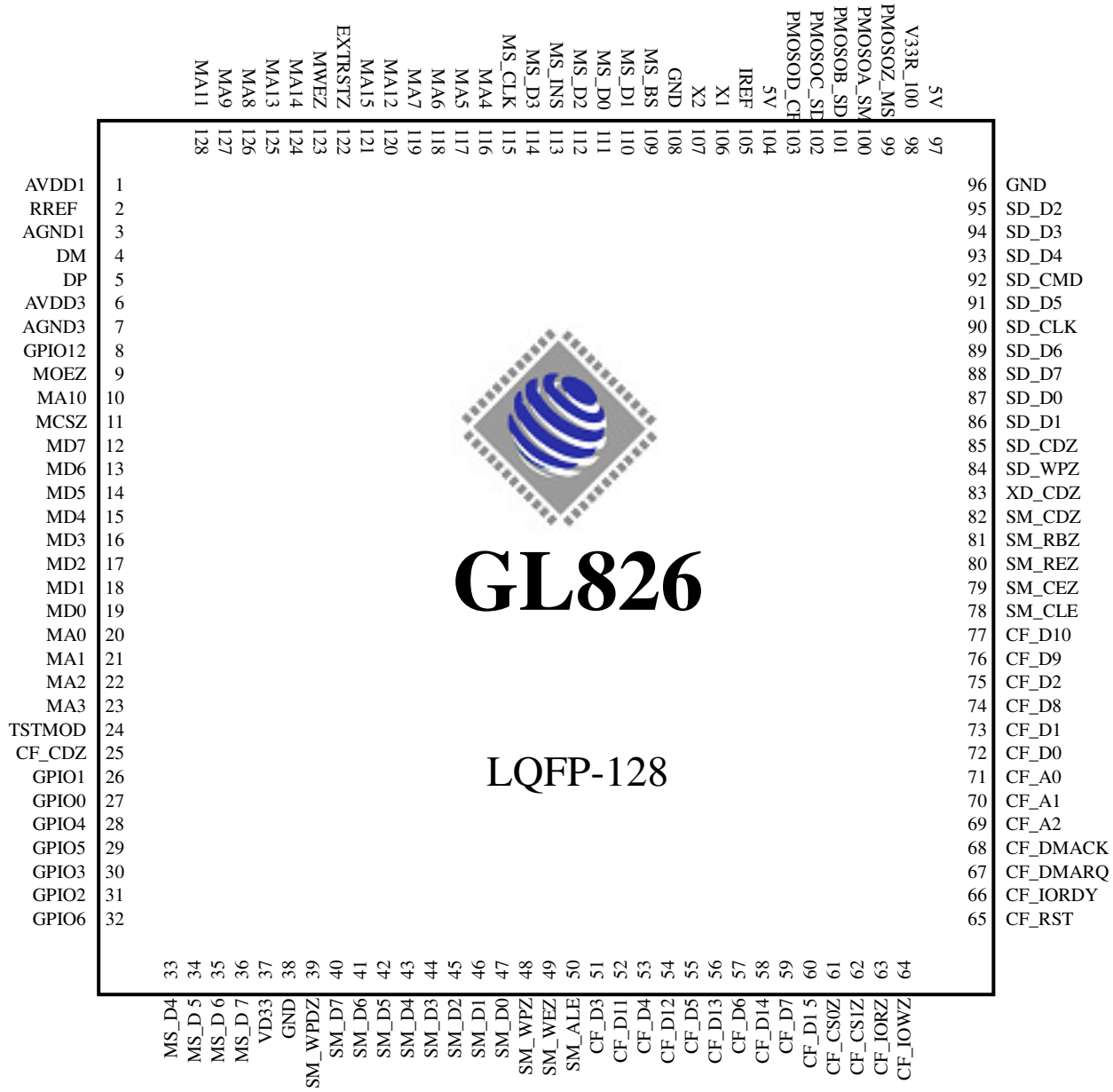


Figure 2.2－LQFP 128 Pinout Diagram(with MSPRO-HG 8-bit support)

2.2.2 Pin List

Table 2.3－Pin List

Pin #	Pin Name	Type	Pin #	Pin Name	Type	Pin #	Pin Name	Type	Pin #	Pin Name	Type
1	AVDD1	P	33	MS_D4	B	65	CF_RST	O	97	5V	P
2	RREF	A	34	MS_D5	B	66	CF_IORDY	I	98	VDD33	P
3	AGND1	P	35	MS_D6	B	67	CF_DMARQ	I	99	PMOSOZ_MS	P
4	DM	A	36	MS_D7	B	68	CF_DMACK	O	100	PMOSOA_SM	P
5	DP	A	37	VDD33	P	69	CF_A2	O	101	PMOSOB_SD	P
6	AVDD3	P	38	GND	P	70	CF_A1	O	102	PMOSOC_SD	P
7	AGND3	P	39	SM_WPDZ	I	71	CF_A0	O	103	PMOSOD_CF	P
8	GPIO12	B	40	SM_D7	B	72	CF_D0	B	104	5V	P
9	MOEZ	B	41	SM_D6	B	73	CF_D1	B	105	IREF	A
10	MA10	B	42	SM_D5	B	74	CF_D8	B	106	X1	I
11	MCSZ	B	43	SM_D4	B	75	CF_D2	B	107	X2	B
12	MD7	B	44	SM_D3	B	76	CF_D9	B	108	GND	P
13	MD6	B	45	SM_D2	B	77	CF_D10	B	109	MS_BS	O
14	MD5	B	46	SM_D1	B	78	SM_CLE	O	110	MS_D1	B
15	MD4	B	47	SM_D0	B	79	SM_CEZ	O	111	MS_D0	B
16	MD3	B	48	SM_WPZ	B	80	SM_REZ	O	112	MS_D2	B
17	MD2	B	49	SM_WEZ	O	81	SM_RBZ	I	113	MS_INS	I
18	MD1	B	50	SM_ALE	O	82	SM_CDZ	B	114	MS_D3	B
19	MD0	B	51	CF_D3	B	83	XD_CDZ	I	115	MS_CLK	O
20	MA0	B	52	CF_D11	B	84	SD_WPZ	I	116	MA4	O
21	MA1	B	53	CF_D4	B	85	SD_CDZ	I	117	MA5	O
22	MA2	B	54	CF_D12	B	86	SD_D1	B	118	MA6	O
23	MA3	B	55	CF_D5	B	87	SD_D0	B	119	MA7	O
24	TSTMOD	I	56	CF_D13	B	88	SD_D7	B	120	MA12	O
25	CF_CDZ	I	57	CF_D6	B	89	SD_D6	B	121	MA15	O
26	GPIO1	B	58	CF_D14	B	90	SD_CLK	O	122	EXTRSTZ	I
27	GPIO0	B	59	CF_D7	B	91	SD_D5	B	123	MWEZ	O
28	GPIO4	B	60	CF_D15	B	92	SD_CMD	B	124	MA14	O
29	GPIO5	B	61	CF_CS0Z	O	93	SD_D4	B	125	MA13	O
30	GPIO3	B	62	CF_CS1Z	O	94	SD_D3	B	126	MA8	O
31	GPIO2	B	63	CF_IORZ	O	95	SD_D2	B	127	MA9	O
32	GPIO6	I	64	CF_IOWZ	O	96	GND	P	128	MA11	O

2.2.3 Pin Description

Table 2.4－Pin Description

Pin Name	Pin #	Type	Description
AVDD1	1	P	Analog power
RREF	2	A	USB Reference resistor
AGND1	3	P	Analog ground
DM	4	A	USB D-
DP	5	A	USB D+
AVDD3	6	P	Analog power
AGND3	7	P	Analog ground
VDD33	37, 98	P	PAD power 3.3V
GND	38, 96, 108	P	Digital Ground
GPIO1~6, 12	8, 26~32	B	General purpose IO
TSTMOD	24	I, pd	Test mode
MCSZ	11	O, pu	External flash chip select
MOEZ	9	O, pu	External flash output enable
MWEZ	123	O, pu	External flash write enable
MA15~0	121~125, 120, 128, 10, 127, 126, 119~116, 23~20	O	External flash address ports
MA6	118	O	Serial EEPROM clock
MA7	119	B, pu	Serial EEPROM data
MD7~0	12~19	B, pd	External flash data ports
CF_CDZ	25	I, pu	CF card detect
CF_D15~0	60, 58, 56, 54, 52, 77, 76, 74, 59, 57, 55, 53, 51, 75, 73, 72	B	CF data ports
CF_CS0Z	61	O, pu	CF chip select 0
CF_CS1Z	62	O, pu	CF chip select 1
CF_IORZ	63	O, pu	CF IO read
CF_IOWZ	64	O, pu	CF IO write
CF_RST	65	O, pu	CF reset
CF_IORDY	66	I, pu	CF IO ready
CF_DMARQ	67	I, pd	CF DMA request
CF_DMACK	68	O	CF DMA acknowledge
CF_A2~0	69~71	O	CF address
SM_WPDZ	39	I, pu	SM WP#
SM_D7~0	40~47	B, pd	SM data ports
SM_WPZ	48	B, pu	SM write protect

SM_WEZ	49	O, pu	SM write enable
SM_ALE	50	O, pd	SM_ALE
SM_CLE	78	O, pd	SM command latch enable
SM_CEZ	79	O, pu	SM card enable
SM_REZ	80	O, pu	SM read enable
SM_RBZ	81	I, pu	SM read/busy
SM_CDZ	82	B, pu	SM card detect
XD_CDZ	83	I, pu	xD card detect
SD_WPZ	84	I, pd	SD write protect
SD_CDZ	85	I, pu	SD card detect
SD_D7~0	88, 89, 91, 93 94, 95, 86, 87	B, pd	SD data line
SD_CLK	90	O, pd	SD clock
SD_CMD	92	B, pd	SD command/response
MS_BS	109	O, pd	MS/MSP bus state
MS_INS	113	I, pu	MS insertion detect
MS_D3~0, 4~7	114, 112, 110, 111, 33~36	B, pd	MS/MSP data signal
MS_CLK	115	O, pd	MS clock
5V	97, 104	P	5V power input
PMOSOZ_ MS	99	P	MS power 250mA
PMOSOA_SM	100	P	SM power 100mA
PMOSOB_SD	101	P	SD power 200mA
PMOSOC_SD	102	P	
PMOSOD_CF	103	P	CF power 500mA
IREF	105	A	Regulator reference voltage
X1	106	I	XTAL 1
X2	107	B	XTAL 2
EXTRSTZ	122	I, pu	System reset

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	pu	internal pull-up when input
	pd	internal pull-down when input
	P	Power / Ground
	A	Analog

2.2.4 Comparison of MS PRO-HG 8-bit support

Table 2.5－Difference of pin name

	With Dual SD and MS-PRO 4 bits		With MS PRO-HG 8bit	
Pin #	Pin Name	Type	Pin Name	Type
26	mSD _D1	B	GPIO1	B
27	mSD_D0	B	GPIO0	B
28	mSD _CLK	O	GPIO4	B
29	mSD _CMD	B	GPIO5	B
30	mSD _D3	B	GPIO3	B
31	mSD _D2	B	GPIO2	B
32	mSD _CDZ	I	GPIO6	I
33	GPIO8	B	MS_D4	B
34	GPIO9	B	MS_D5	B
35	GPIO10	B	MS_D6	B
36	GPIO11	B	MS_D7	B
99	PMOSOZ_ SD	P	PMOSOZ_ MS	P
101	PMOSOB_MS	P	PMOSOB_ SD	P
102	PMOSOC_mSD	P	PMOSOC_SD	P

2.3 LQFP 48

2.3.1 Pinout Diagram

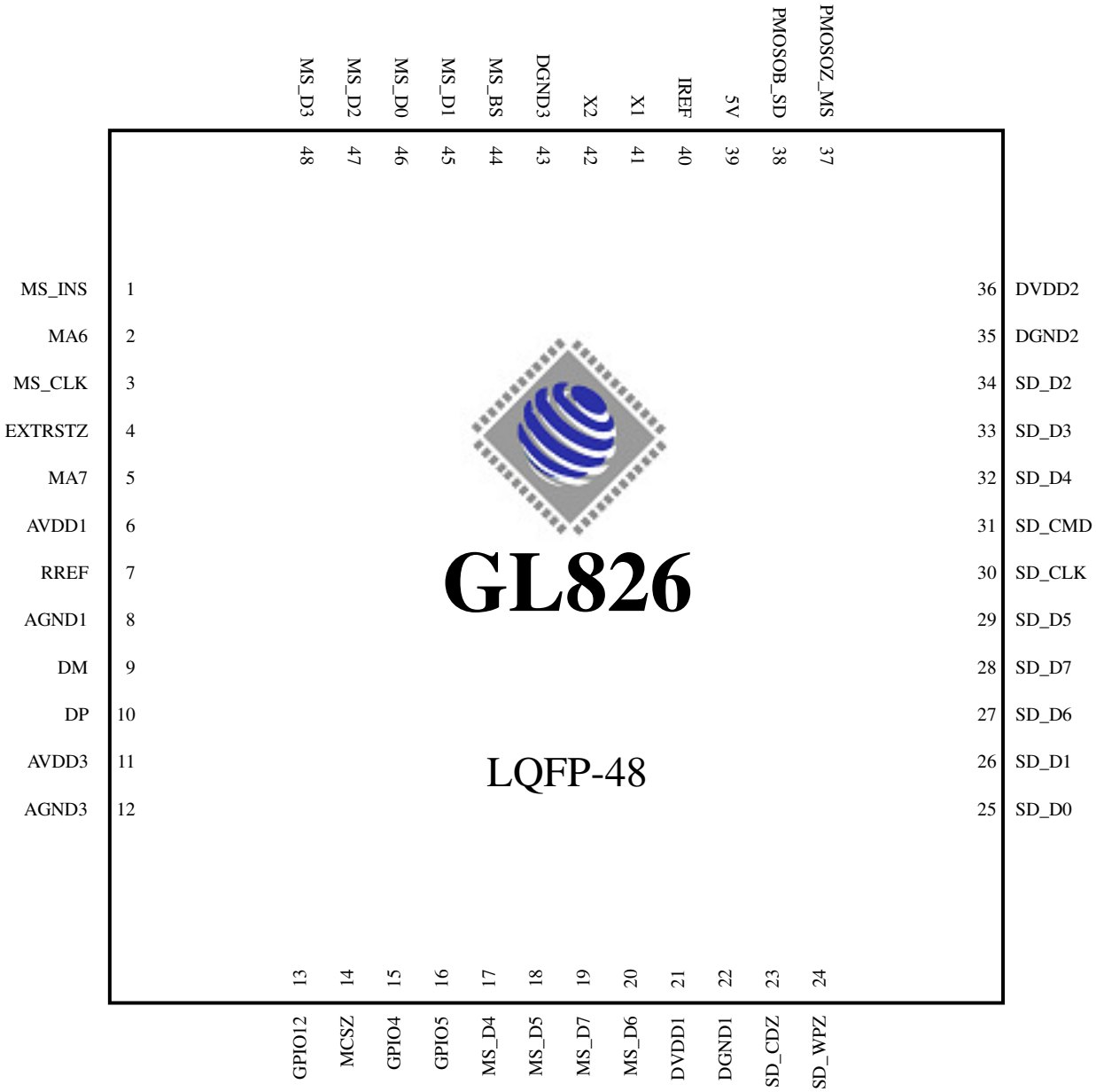


Figure 2.3－LQFP 48 Pinout Diagram

2.3.2 Pin List

Table 2.6－Pin List

Pin #	Pin Name	Type	Pin #	Pin Name	Type	Pin #	Pin Name	Type	Pin #	Pin Name	Type
1	MS_INS	I	13	GPIO12	B	25	SD_D0	B	37	PMOSOZ_MS	P
2	MA6	O	14	MCSZ	B	26	SD_D1	B	38	PMOSOB_SD	P
3	MS_CLK	O	15	GPIO4	B	27	SD_D6	B	39	5V	P
4	EXTRSTZ	I	16	GPIO5	B	28	SD_D7	B	40	IREF	A
5	MA7	B	17	MS_D4	B	29	SD_D5	B	41	X1	I
6	AVDD1	P	18	MS_D5	B	30	SD_CLK	O	42	X2	B
7	RREF	A	19	MS_D7	B	31	SD_CMD	B	43	DGND3	P
8	AGND1	P	20	MS_D6	B	32	SD_D4	B	44	MS_BS	O
9	DM	A	21	DVDD1	P	33	SD_D3	B	45	MS_D1	B
10	DP	A	22	DGND1	P	34	SD_D2	B	46	MS_D0	B
11	AVDD3	P	23	SD_CDZ	I	35	DGND2	P	47	MS_D2	B
12	AGND3	P	24	SD_WPZ	I	36	DVDD2	P	48	MS_D3	B

2.3.3 Pin Description

Table 2.7－Pin Description

Pin Name	Pin #	Type	Description
AVDD1	6	P	Analog power 3.3V
RREF	7	A	USB Reference resistor
AGND1	8	P	Analog ground
DM	9	A	USB D-
DP	10	A	USB D+
AVDD3	11	P	Analog power 3.3V
AGND3	12	P	Analog ground
DVDD	21, 36	P	PAD power 3.3V
DGND	22, 35, 43	P	Digital Ground
GPIO4	15	I	General purpose strapping 1
GPIO5	16	I	General purpose strapping 2
GPIO12	13	O	General purpose LED
MCSZ	14	O	Chip select LED
MA6	2	O	Serial EEPROM clock
MA7	5	B, pu	Serial EEPROM data
SD_WPZ	24	I, pd	SD write protect
SD_CDZ	23	I, pu	SD card detect

SD_D7~0	28, 27, 29, 32, 33, 34, 26, 25	B, pd	SD data line
SD_CLK	30	O, pd	SD clock
SD_CMD	31	B, pd	SD command/response
MS_BS	44	O, pd	MS/MSP bus state
MS_INS	1	I, pu	MS insertion detect
MS_D7~0	19, 20, 18, 17 48, 47, 45, 46	B, pd	MS/MSP data signal
MS_CLK	3	O, pd	MS clock
5V	39	P	5V power input
PMOSOZ_ MS	37	P	MS power 250mA
PMOSOB_SD	38	P	SD power 200mA
IREF	40	A	Regulator reference voltage
X1	41	I	XTAL 1
X2	42	B	XTAL 2
EXTRSTZ	4	I, pu	System reset

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	pu	internal pull-up when input
	pd	internal pull-down when input
	P	Power / Ground
	A	Analog

CHAPTER 3 Block Diagram

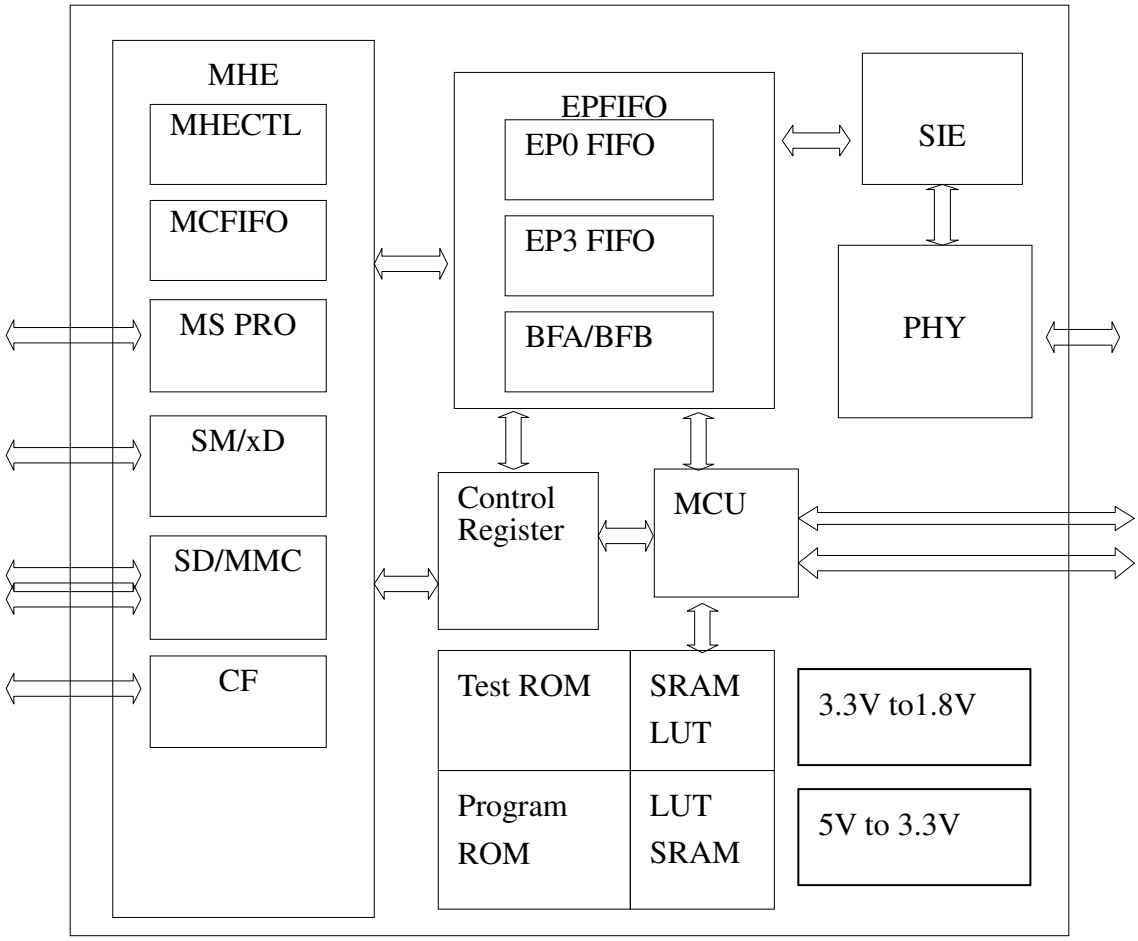


Figure 3.1—Functional Block Diagram

Notation:

1. Support Dual SD and MS PRO 4-bit for 5 slots (CF, SM/xD, SD/MMC 8bit, MS/MSPRO, microSD/ MMCmicro/ T-Flash 4bit)
2. Support MS PRO-HG 8-bit for 4 slots (CF, SM/xD, SD/MMC 8bit, MS/MSPRO-HG)

CHAPTER 4 ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Table 4.1－Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-65°C to +150 °C
Ambient Temperature	-40°C to +80 °C
Supply Voltage to Ground Potential	-0.5V to +4.0V
DC Input Voltage to Any Pin	-0.5V to +5.8V

4.2 Operating Conditions

Table 4.2－Operating Conditions

Parameter	Value
Ta (Ambient Temperature Under Bias)	0°C to 70°C
Supply Voltage	+3.0V to +3.6V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	12 MHz ± 0.05% 12 MHz ± 0.25% (for USB full-speed only)

4.3 DC Characteristics

Table 4.3－DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0	-	3.6	V
V_{IH}	Input High Voltage		2.0	-	3.6	V
V_{IL}	Input Low Voltage		-0.3	-	0.8	V
I_I	Input Leakage current	$0 < V_{IN} < V_{CC}$	-10	-	10	µA
V_{OH}	Output High Voltage		3.0	-	-	V
V_{OL}	Output Low Voltage		-	-	0.4	V
I_{OH}	Output Current High	VDD=3.3V VOH=2.4V	-	4	-	mA
I_{OL}	Output Current Low	VDD=3.3V VOL=0.4V	-	4	-	mA
C_{IN}	Input Pin Capacitance		-	5	-	pF
I_{SUSP}	Suspend current	1.5K external pull-up included	-	-	450	µA
I_{CC}	Supply current	Connect to USB with 8051 operating	-	-	60	mA

4.4 AC Characteristics of External Flash

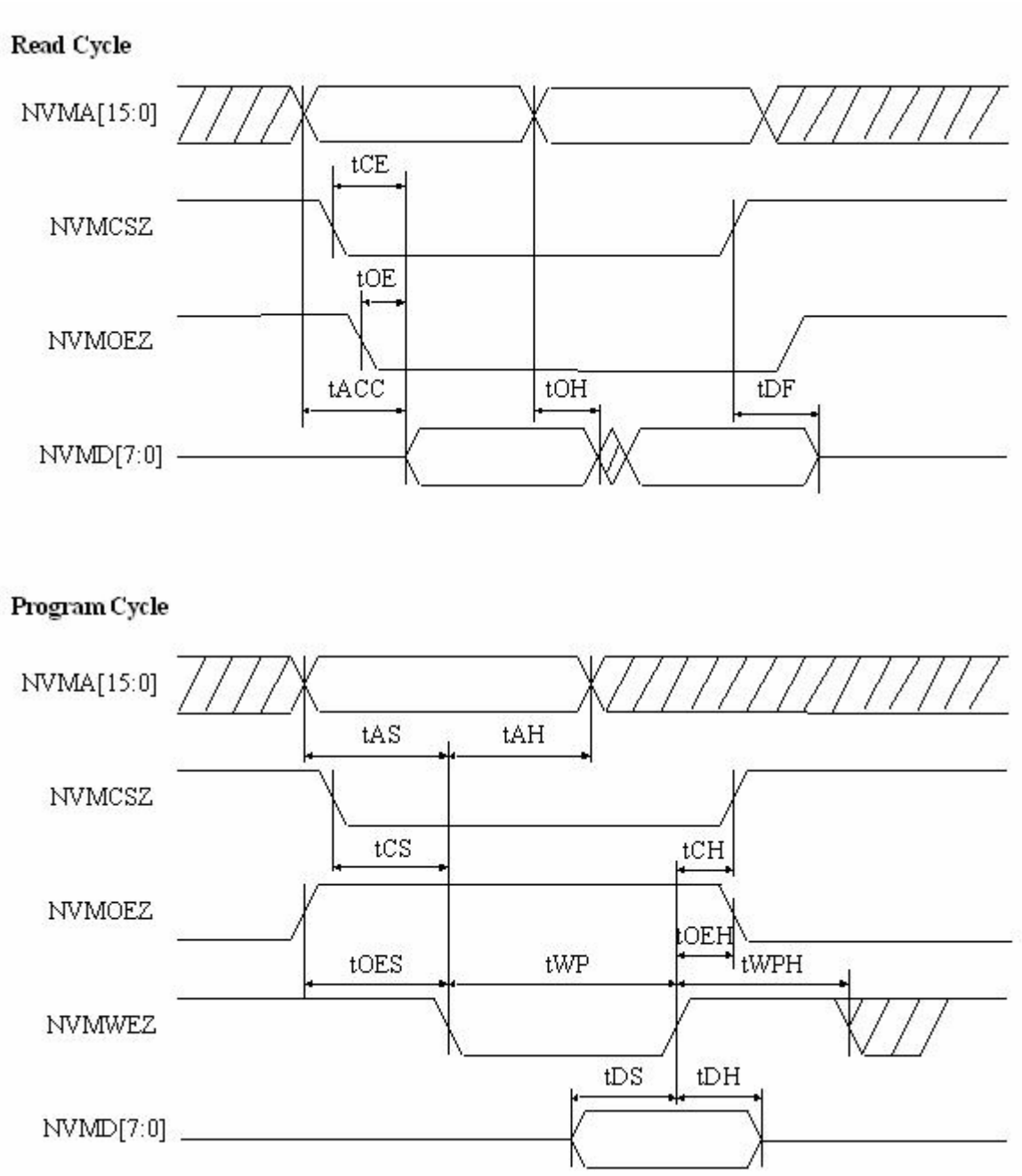


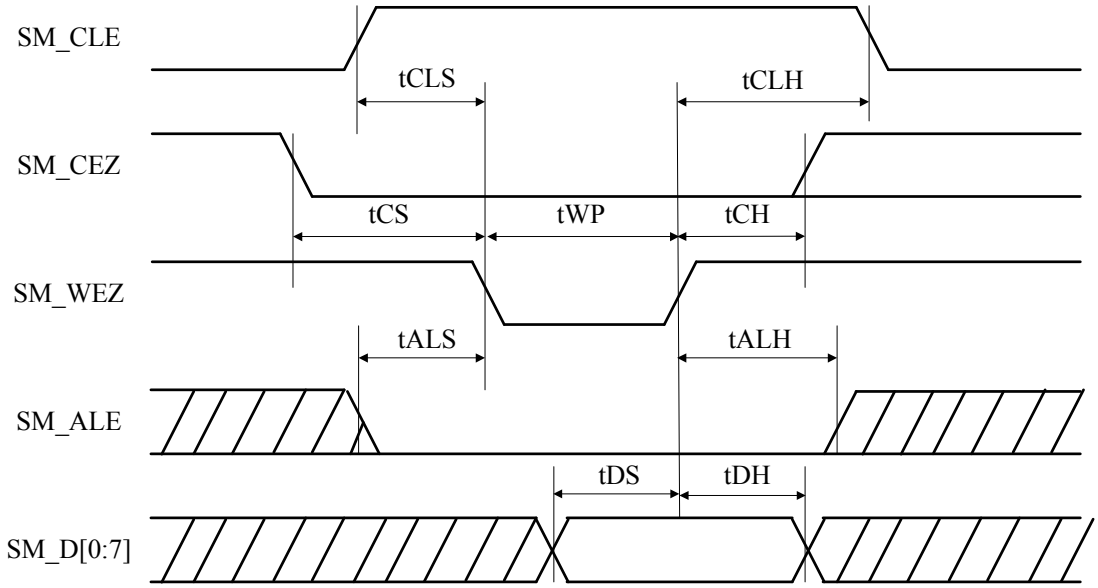
Figure 4.1－Timing Diagram of External Flash

Table 4.4－AC Characteristics of Flash Interface (C_L = 30pF)

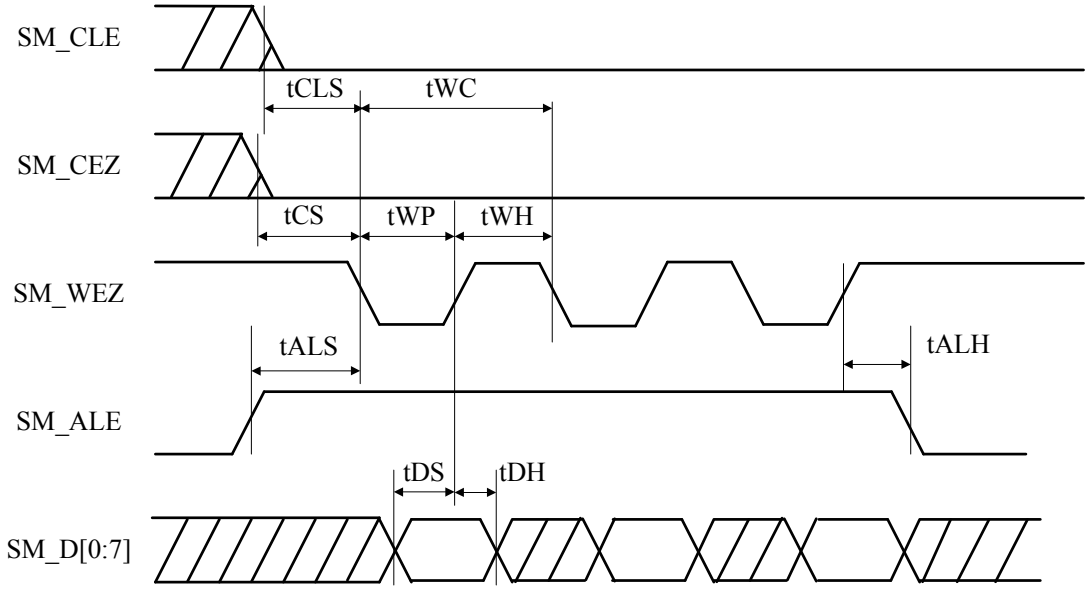
Symbol	Parameter	Max.	Unit
tACC	Address to Output Delay (max)	83	ns
tCE	NVMCSZ to Output Delay (max)	83	
tDF	NVMCEZ or NVMOEZ, whichever occurred first, to Output Float (max)	0	
tOH	Output Hold from NVMOEZ, NVMCSZ or Address, whichever occurred first (min)	0	
tAS	Address Setup Time (min)	760	
tAH	Address Hold Time (min)	760	
tOES	NVMOEZ Setup Time (min)	300	
tCS	NVMCSZ Setup Time (min)	0	
tCH	NVMCSZ Hold Time (min)	0	
tWP	Write Pulse Width (min)	66	
tWPH	Write Pulse Width High (min)	300	
tDS	Data Setup Time (min)	300	
tDH	Data Hold Time (min)	0	
tOEH	NVMOEZ Hold Time (min)	16	

4.5 AC Characteristics of SmartMedia

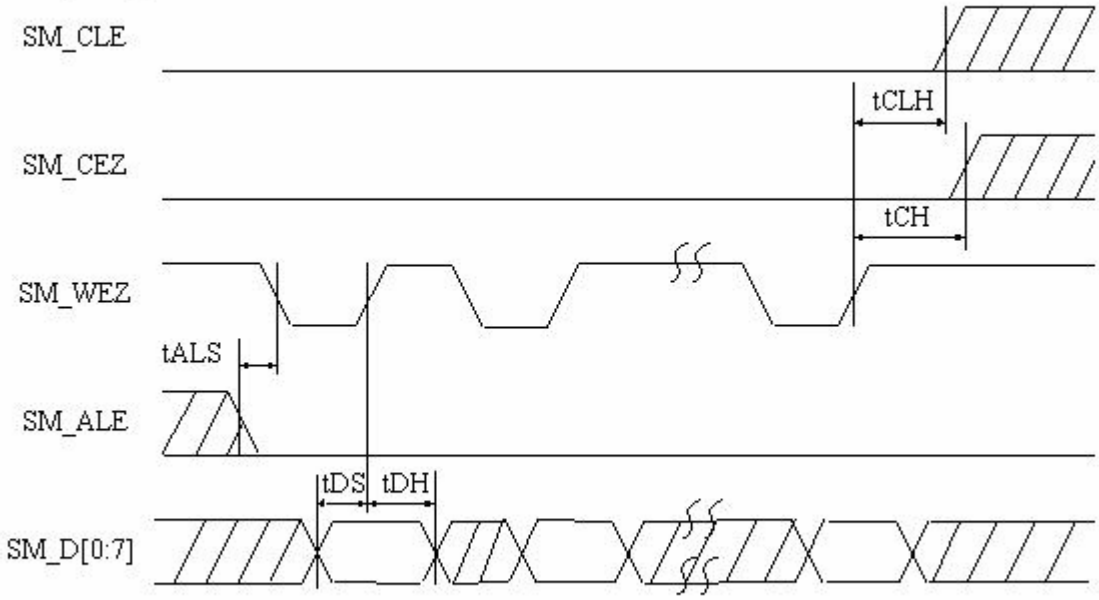
Command Input Cycle



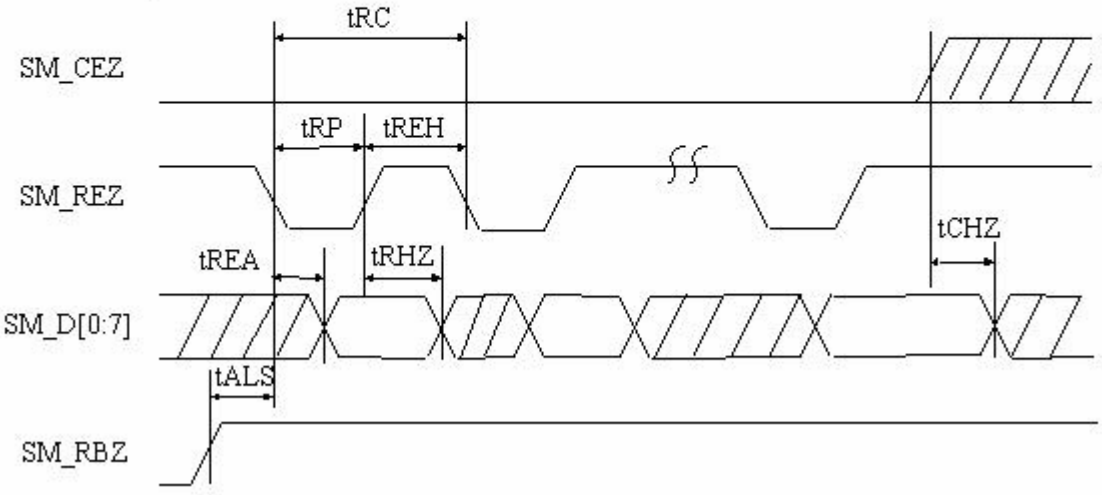
Address Input Cycle



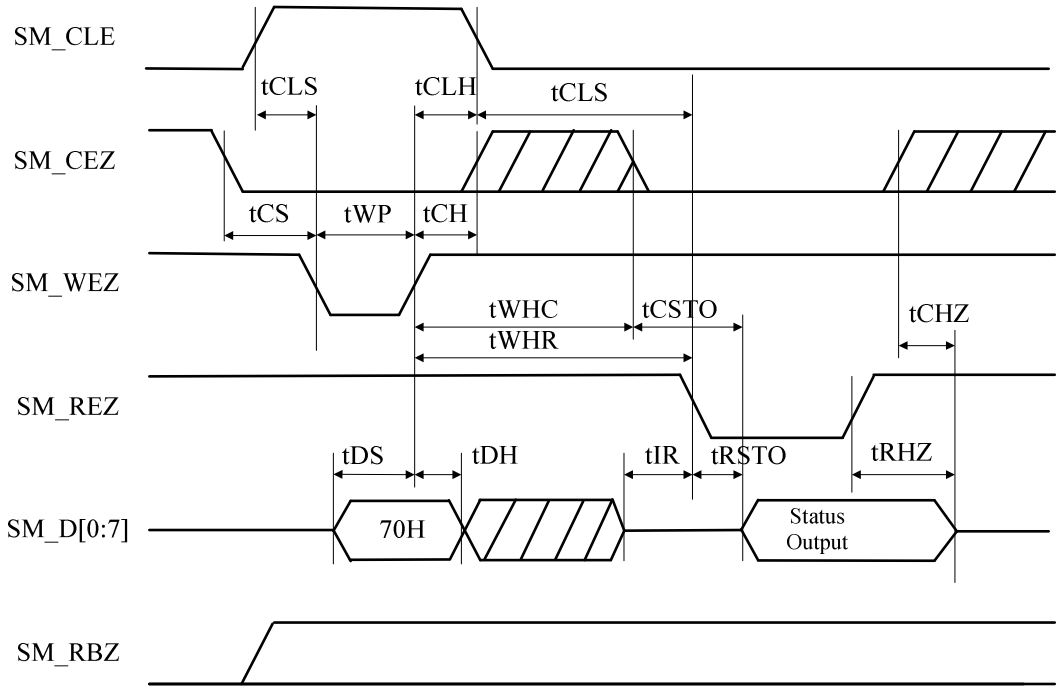
Data Input Cycle



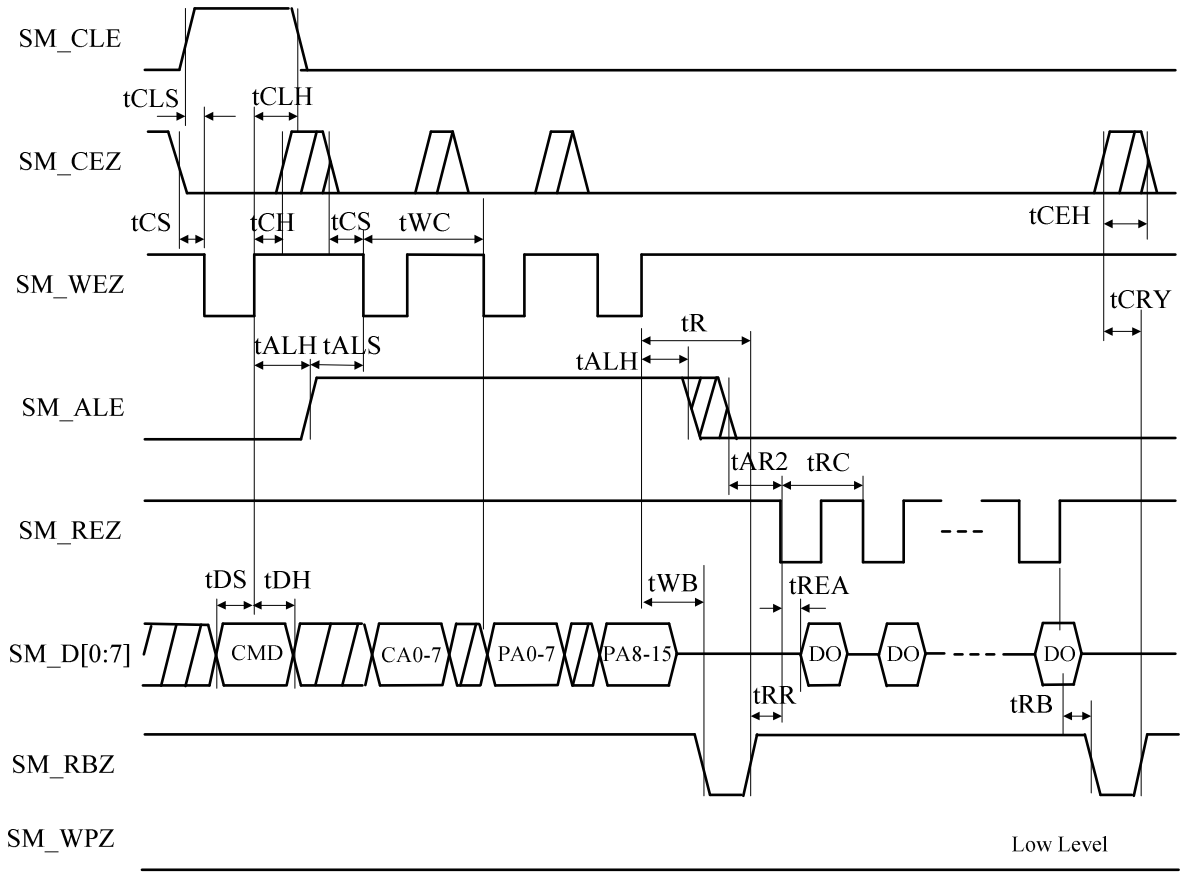
Serial Read Cycle



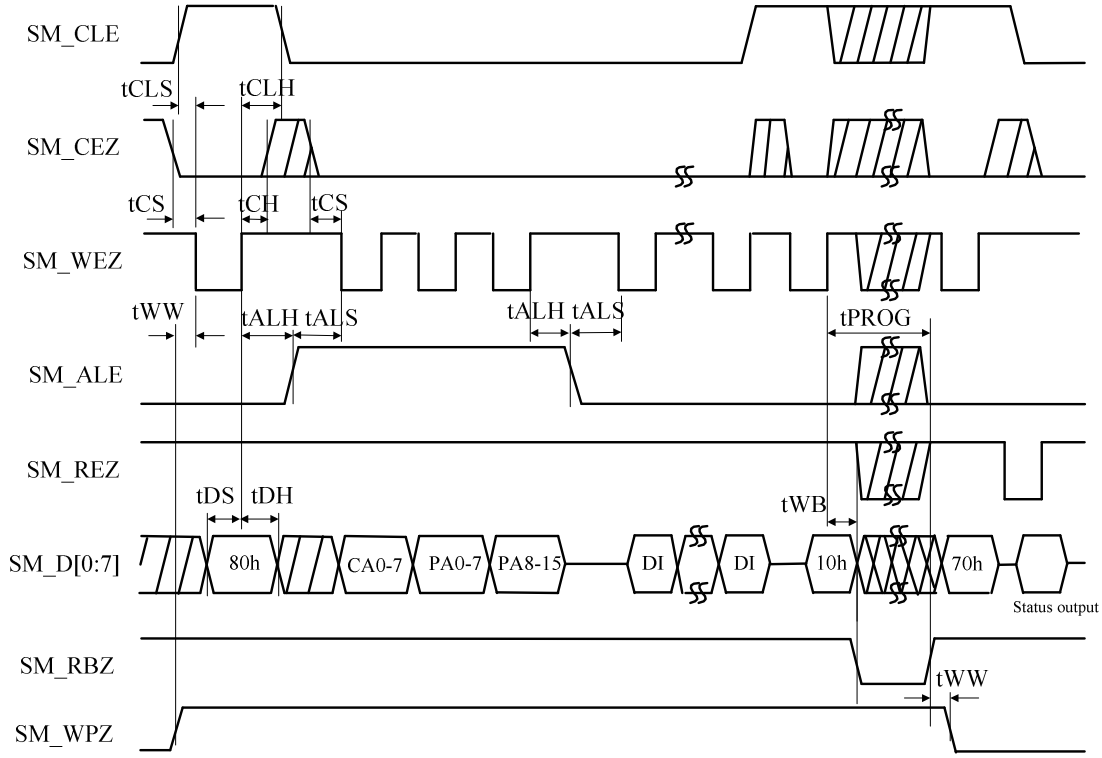
Status Read Cycle



Read Cycle



Auto Page Program Timing



ID Read Timing

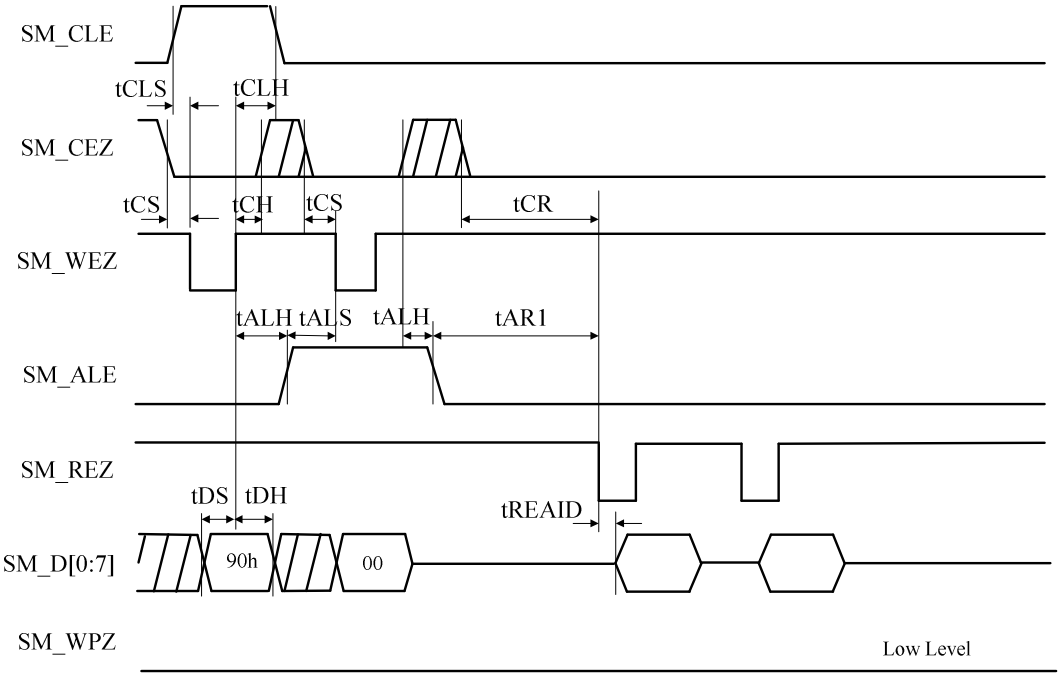


Figure 4.2－Timing Diagram of SmartMedia

Table 4.5－AC Characteristics of Smart Media Interface (C_L = 40 pF)

Symbol	Parameter	Min.	Max.	Unit
tCLS	CLE Setup Time	20	-	ns
tCLH	CLE Hold Time	40	-	ns
tCS	-CE Setup Time	20	-	ns
tCH	-CE Hold Time	40	-	ns
tWP	-WE Pulse Width	40	-	ns
tALS	ALE Setup Time	20	-	ns
tALH	ALE Hold Time	40	-	ns
tDS	Data Setup Time	30	-	ns
tDH	Data Hold Time	20	-	ns
tWC	Write Cycle Time	80	-	ns
tWH	-WE High Hold Time	20	-	ns
tWW	-WP High to –WE Low	100	-	ns
tRR	Ready to –RE Low	20	-	ns
tRP	Read Pulse Width	60	-	ns
tRC	Read cycle Time	80	-	ns
tREA	-RE Access Time (Serial Data Access)	-	45	ns
tCEH	-CE High Hold Time (At the Last Serial Read)	250	-	ns
tREAID	-RE Access Time (ID Read)	-	90	ns
tRHZ	-RE High to Output Hi-Z	5	30	ns
tCHZ	-CE High to Output Hi-Z	-	30	ns
tREH	-RE High Hold Time	20	-	ns
tRSTO	-RE Access Time	-	45	ns
tCSTO	-CE Access Time	-	55	ns
tRHW	-RE High to -WE Low	0	-	ns
tWHC	-WE High to –CE Low	50	-	ns
tWHR	-WE High to –RE Low	60	-	ns
tAR1	ALE Low to –RE Low (Address Register Read, ID Read)	200	-	ns
tCR	-CE Low to –RE Low (Data Register Read, ID Read)	200	-	ns
tWB	-WE High to Busy	-	200	ns
tAR2	ALE Low to RE Low (Read Cycle)	150		ns
tRB	Last –RE High to Busy (at Sequential Read)	-	500	ns
tCRY	-CE High to Ready	-	1	µs

4.6 AC Characteristics of xD-Picture

The Timing diagrams are the same as SM.

Table 4.6－AC Characteristics of xD (C_L = 40pF)

Parameter	Description	Min.	Max.	Unit
tCLS	CLE Set up Time	20	-	ns
tCLH	CLE Hold Time	40	-	
tCS	CE Setup up Time	20	-	
tCH	CE Hold Time	40	-	
tWP	WE Pulse Width	40	-	
tALS	ALE Setup Time	20	-	
tALH	ALE Hold Time	40	-	
tDS	Data Setup Time	30	-	
tDH	Data Hold Time	20	-	
tWC	Write Cycle Time	80	-	
tWH	WE High Hold Time	20	-	
tWW	WP High to WE Low	100	-	
tRR	Ready to RE Low	20	-	
tRP	Read Pulse Width	60	-	
tRC	Read Cycle Time	80	-	
tREA	RE Access Time(Serial Data Access)	-	45	
tCEH	CE High Hold Time	250	-	
tREAID	RE Access Time(ID Read)	-	90	
tRHZ	RE High to Output Hi-Z	5	30	
tCHZ	CE High to Output Hi-Z	-	30	
tREH	RE High Hold Time	20	-	
tRSTO	RE Access Time	-	45	
tCSTO	CE Access Time	-	55	
tRHW	RE High to WE Low	0	-	
tWHC	WE High to CE Low	50	-	
tWHR	WE High to RE Low	60	-	
TAR1	ALE Low to RE Low	200	-	
tCR	CE Low to RE Low	200	-	
tWB	WE High to Busy	-	200	
TAR2	ALE LOW to RE LOW	150	-	
tRB	Last RE High to Busy	-	200	

4.7 AC Characteristics of Memory Stick

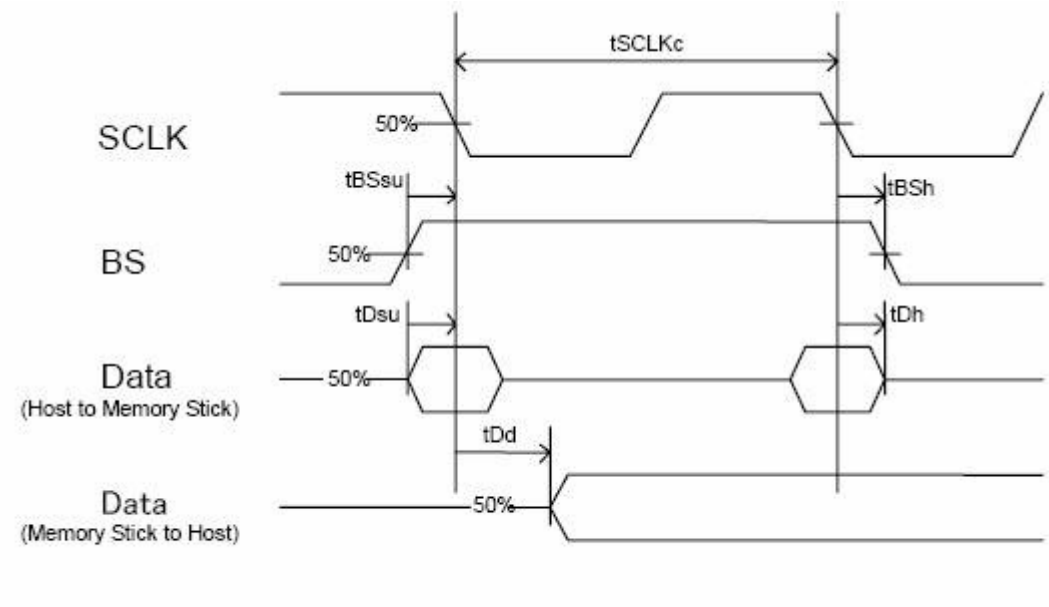


Figure 4.3－MemoryStick Parallel Transfer Operation Timing

Table 4.7－AC Characteristics of Memory Stick Interface (C_L = 26 pF)

Parameter	Description	Type	Unit
F_{SCLK}	SCLK frequency	20	MHz
Parameter	**Description**	**F_{SCLK} = 20 MHz**	**Unit**
tSCLKc	SCLK Cycle	50.0	ns
tSCLKwh	SCLK H pulse length (min)	15	ns
tSCLKwl	SCLK L pulse length (min)	15	ns
tSCLKr	SCLK rise time (min)	5	ns
tSCLKr	SCLK rise time (max)	10	ns
tSCLKf	SCLK Fall time (min)	5	ns
tSCLKf	SCLK Fall time (max)	10	ns
tBSsu	BS setup time (min)	5	ns
tBSh	BS hold time (min)	5	ns
tDsu	DATA setup time (min)	5	ns
tDh	DATA hold time (min)	5	ns
tDd	DATA output delay time (max)	5	ns

4.8 AC Characteristics of Memory Stick PRO/ Memory Stick PRO-HG

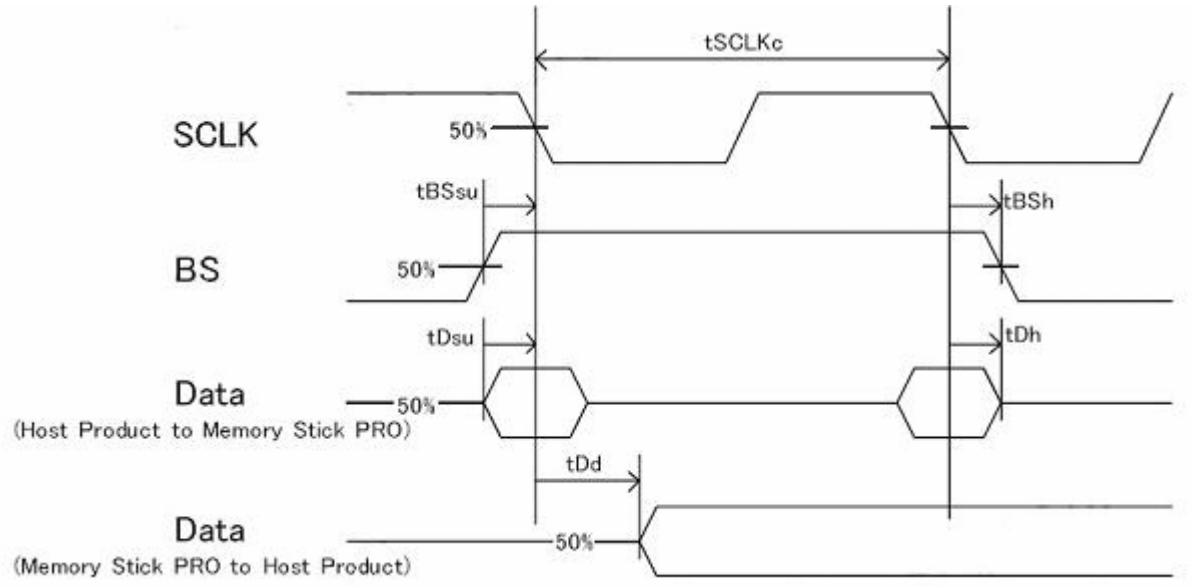


Figure 4.4－MemoryStick PRO Parallel Transfer Operation Timing

Table 4.8－AC Characteristics of MS PRO interface (C_L = 15 pF)

Parameter	Description	F_{SCLK} = 40 MHz	Unit
tSCLKc	SCLK Cycle	25.0	ns
tSCLKwh	SCLK H pulse length (min)	5	ns
tSCLKwl	SCLK L pulse length (min)	5	ns
tSCLKr	SCLK rise time (min)	5	ns
tSCLKr	SCLK rise time (max)	7.5	ns
tSCLKf	SCLK Fall time (min)	5	ns
tSCLKf	SCLK Fall time (max)	7.5	ns
tBSsu	BS setup time (min)	8	ns
tBSh	BS hold time (min)	1	ns
tDsu	DATA setup time (min)	8	ns
tDh	DATA hold time (min)	1	ns
tDd	DATA output delay time (max)	5	ns

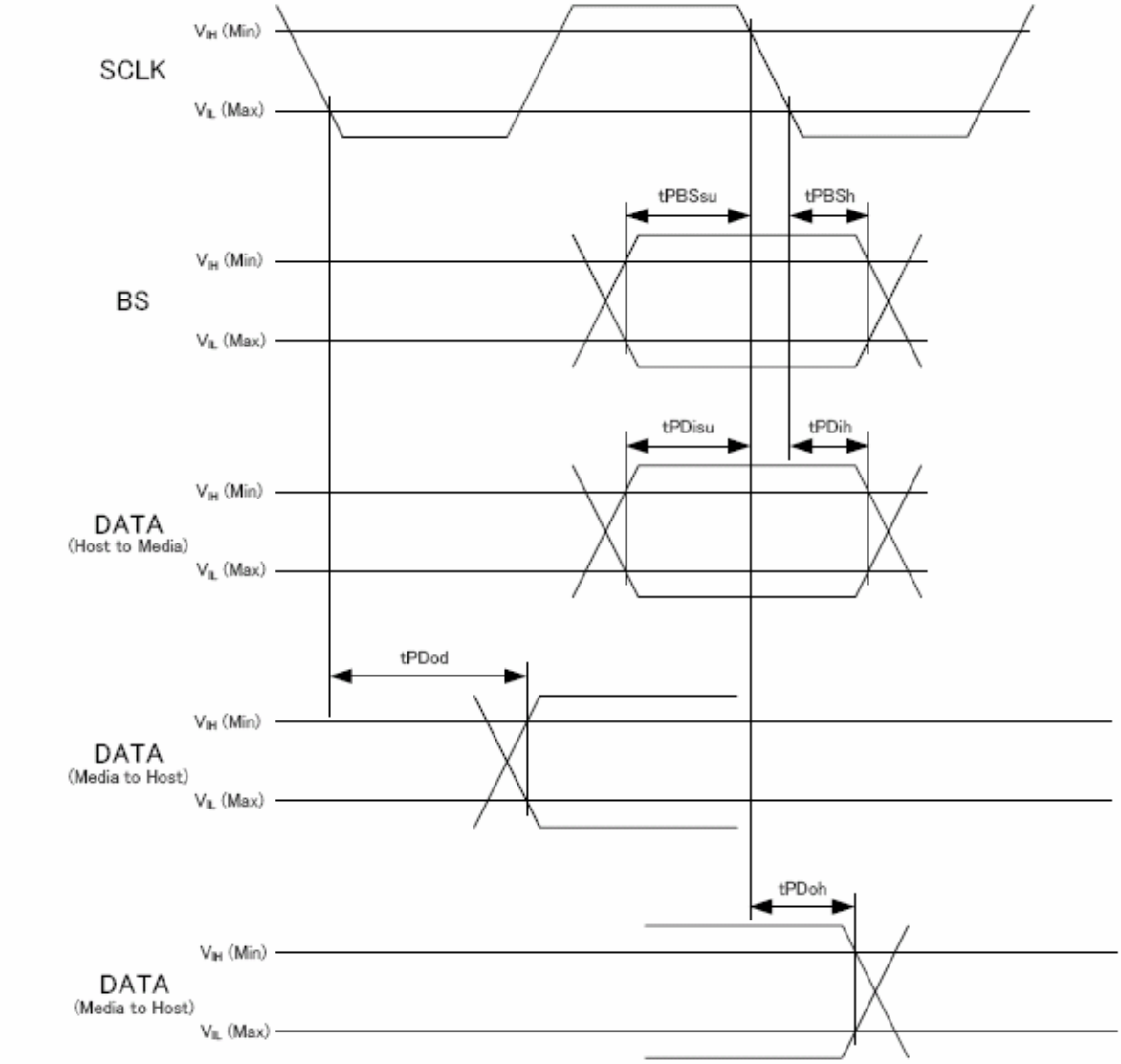


Figure 4.5－MemoryStick PRO-HG Parallel Transfer Operation Timing

Table 4.9－AC Characteristics of Parallel MS PRO-HG interface (C_L = 15 pF)

Parameter	Description	FSCLK= 40 MHz (4-bit)	FSCLK= 60 MHz (8-bit)	Unit
tSCLKc	SCLK Cycle(min)	25	16.66	ns
tSCLKwh	SCLK H pulse length (min)	5	5	ns
tSCLKwl	SCLK L pulse length (min)	5	5	ns
tSCLKr	SCLK rise time (max)	7.5	7.5	ns
tSCLKf	SCLK Fall time (max)	7.5	7.5	ns

tPBSsu	BS setup time (min)	7	7	ns
tPBSh	BS hold time (min)	0	0	ns
tBSr	BS rise time (max)	7.5	7.5	ns
tBSf	BS Fall time (max)	7.5	7.5	ns
tPDisu	DATA setup time (min)	7	7	ns
tPDih	DATA hold time (min)	0	0	ns
tPDod	DATA output delay time (max)	15	10	ns
tPDoh	DATA output hold time (min)	1.5	1.5	ns

4.9 AC Characteristics of Secure Digital / MultiMediaCard

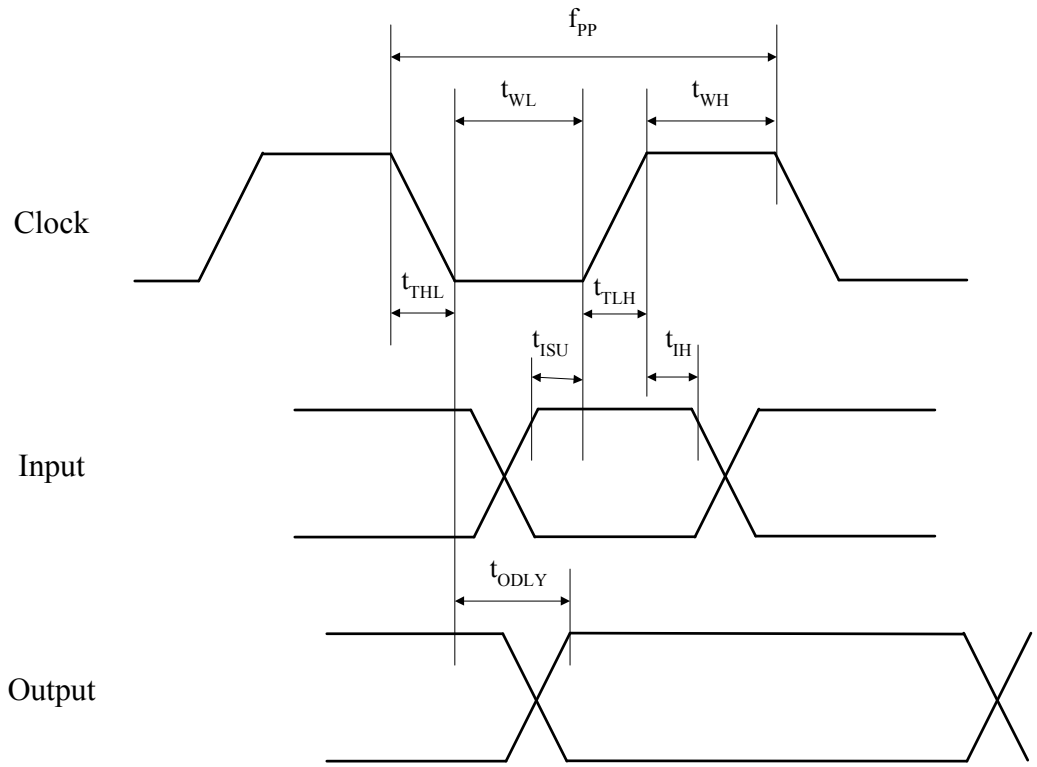


Figure 4.6－Timing Diagram of Secure Digital / MultiMediaCard

Table 4.10－AC Characteristics of SD/MMC Interface Timing (C_L = 10 pF)

Symbol	Parameter	Clock Rate				Unit
f_{PP}	Clock frequency Data Transfer Mode	48	24	20	15	MHz
f_{OD}	Clock frequency Identification Mode	375	375	375	375	KHz
t_{WL}	Clock low time (min)	7	20	22	30	ns
t_{WH}	Clock high time (min)	7	20	22	30	ns
t_{TLH}	Clock rise time (max)	3	3	3	3	ns
t_{THL}	Clock fall time (max)	3	3	3	3	ns
t_{ISU}	Input set-up time (min)	6	5	20	27	ns
t_{IH}	Input hold time (min)	2	5	20	27	ns
t_{ODLY}	Output delay time (max)	14	14	14	14	ns

4.10 AC Characteristics of Compact Flash PIO mode

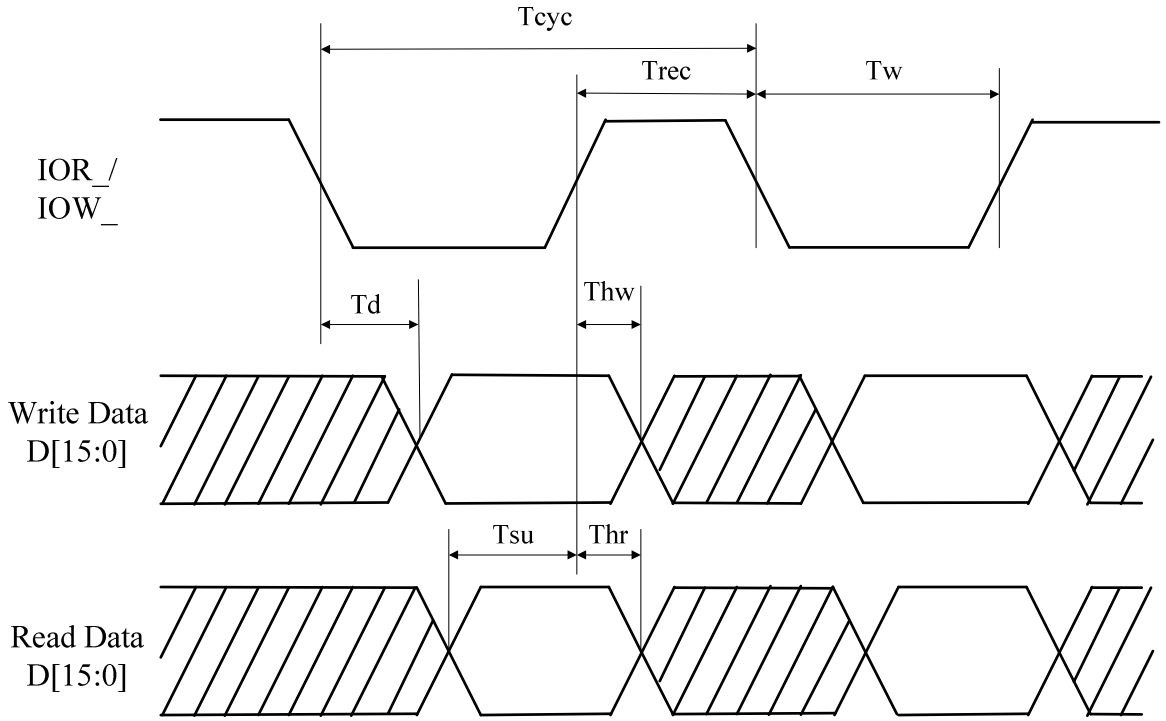


Figure 4.7－Timing Diagram of Compact Flash PIO mode

Table 4.11－AC Characteristics of CF PIO mode (C_L = 40 pF)

Parameter	Item	Mode0	Mode1	Mode2	Mode3	Mode4	Mode5	Mode6	Unit
Tcyc	Cycle Time (min)	600	399	249	183	133	100	83	ns
Tw	Read/Write Active Width (min)	399	266	150	100	83	66	58	ns
Trec	Read/Write Recovery Time (min)	199	132	99	83	49	33	24	ns
Td	Write Data Setup (min)	0	0	0	0	0	0	0	ns
Twh	Write Data Hold (min)	208	142	109	90	55	40	24	ns
Tsu	Read Data Setup (min)	50	35	20	20	20	15	10	ns
Thr	Read Data Hold (min)	5	5	5	5	5	5	5	ns

4.11 AC Characteristics of Compact Flash UDMA mode

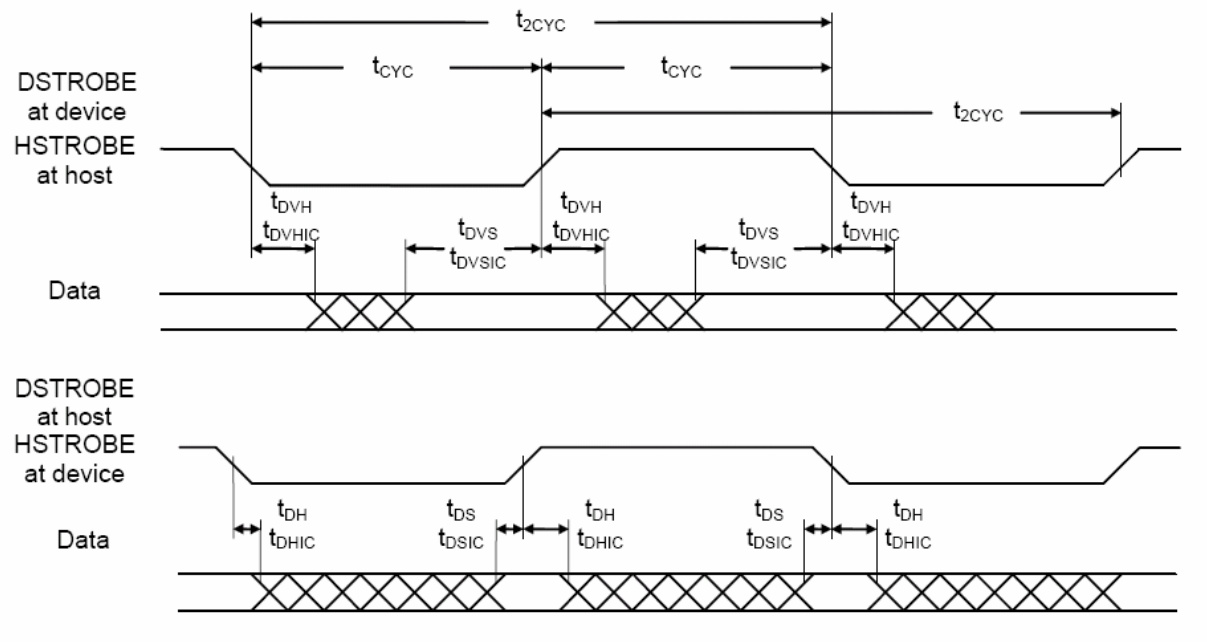


Figure 4.8－Timing Diagram of Compact Flash UDMA mode

Table 4.12－AC Characteristics of CF UDMA mode

Parameter	Description	Mode0	Mode1	Mode2	Mode3	Mode4	Unit
t_{2CYC}	2 Cycle time(min)	230	153	115	86	57	ns
t_{CYC}	Cycle time(min)	112	73	54	39	25	ns
t_{DVS}	Data valid setup time at sender(min)	70	48	31	20	6.7	ns
t_{DVH}	Data valid hold time at sender(min)	6.2	6.2	6.2	6.2	6.2	ns
t_{DS}	Data setup time at recipient(min)	15	10	7	7	5	ns
t_{DH}	Data hold time at recipient(min)	5	5	5	5	5	ns

4.12 AC Characteristics of Reset Timing

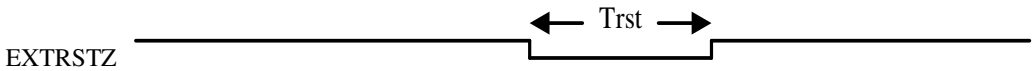


Figure 4.9－Timing Diagram of Reset width

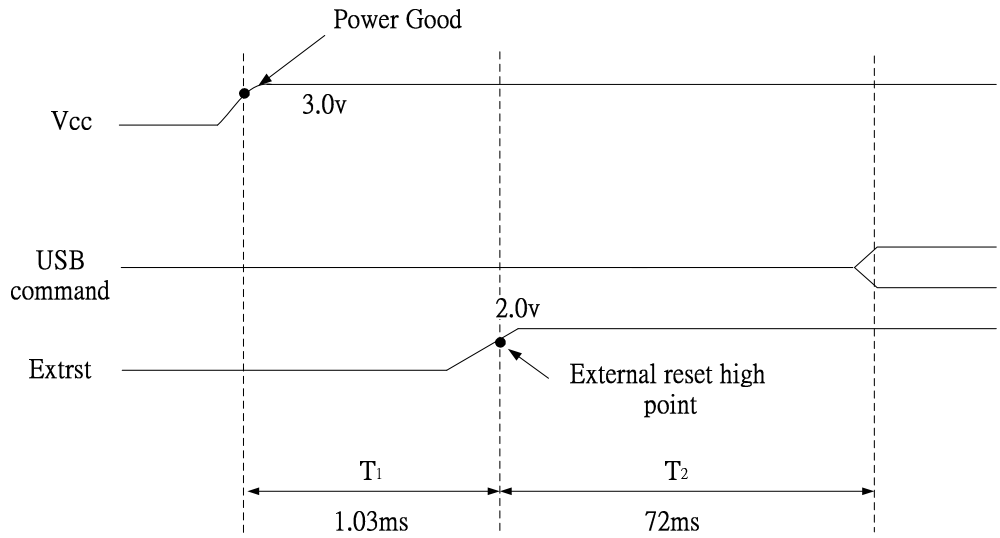


Figure 4.10－Timing Diagram of Power Good to USB command receive ready

Table 4.13－Reset Timing

Parameter	Description	Min.	Typ.	Max.	Unit
Trst	Chip reset sense timing width	2	-	-	us
T1	External reset valid from power up to high	1.03	-	-	ms
T2	Reset Deassertion to respond USB command ready	72	-	-	ms

4.13 AC Characteristics of Serial EEPROM

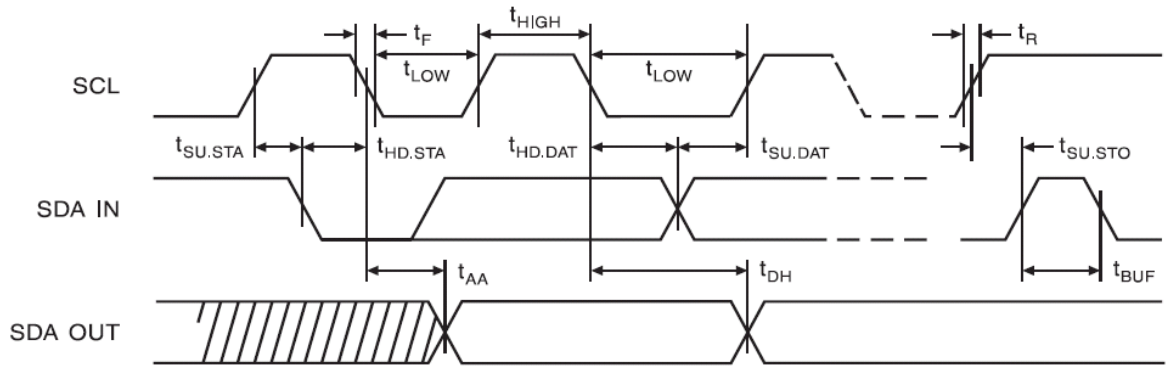
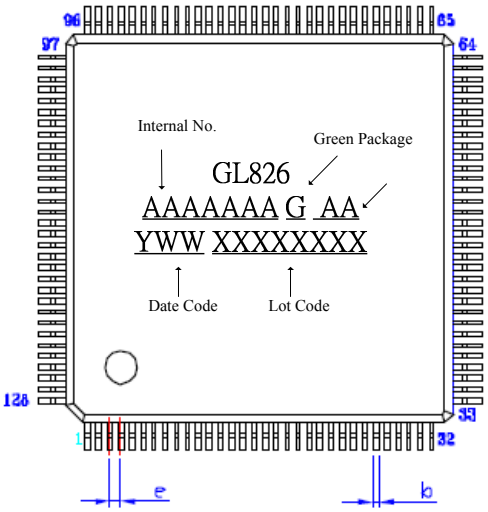


Figure 4.11－Timing Diagram of Serial EEPROM

Table 4.14－Serial EEPROM Timing

Parameter	Description	Min.	Type	Max.	Unit
f_{SCL}	SCL Frequency	-	100	400	KHz
t_{LOW}	SCL Pulse Low	1.2	5	-	us
t_{HIGH}	SCL Pulse High	0.6	5	-	us
t_{BUF}	Time the SDA must be free before a new transmission.	1.2	-	-	us
$t_{HD.STA}$	Start Hold Time	0.6	10	-	us
$t_{SU.STA}$	Start Setup Time	0.6	10	-	us
$t_{HD.DAT}$	Data In Hold Time	0	5	-	us
$t_{SU.DAT}$	Data In Setup Time	100	5	-	ns
$t_{SU.STO}$	Stop Setup Time	0.6	10	-	us
t_{AA}	SCL Low to SDA Out Valid	0.1	-	0.9	us
t_{DH}	Data Out Hold Time	50	-	-	ns

CHAPTER 5 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A			1.60 (63)
A1	0.05 (2)		0.15 (6)
A2	1.35 (53)	1.40 (55)	1.45 (57)
b	0.13 (5)	0.18 (7)	0.23 (9)
c	0.09 (4)		0.20 (8)
D	16.00 (630) BSC		
D1	14.00 (551) BSC		
E	16.00 (630) BSC		
E1	14.00 (551) BSC		
e	0.40 (16) BSC		
L	0.45 (18)	0.60 (24)	0.75 (30)
L1	1.00 (39) REF		
Y			0.10 (4)
θ	0°	3.5°	7°

NOTE: 1. REFER TO JEDEC MS-026/BEE REV.B
2. ALL DIMENSIONS IN MILLIMETERS.

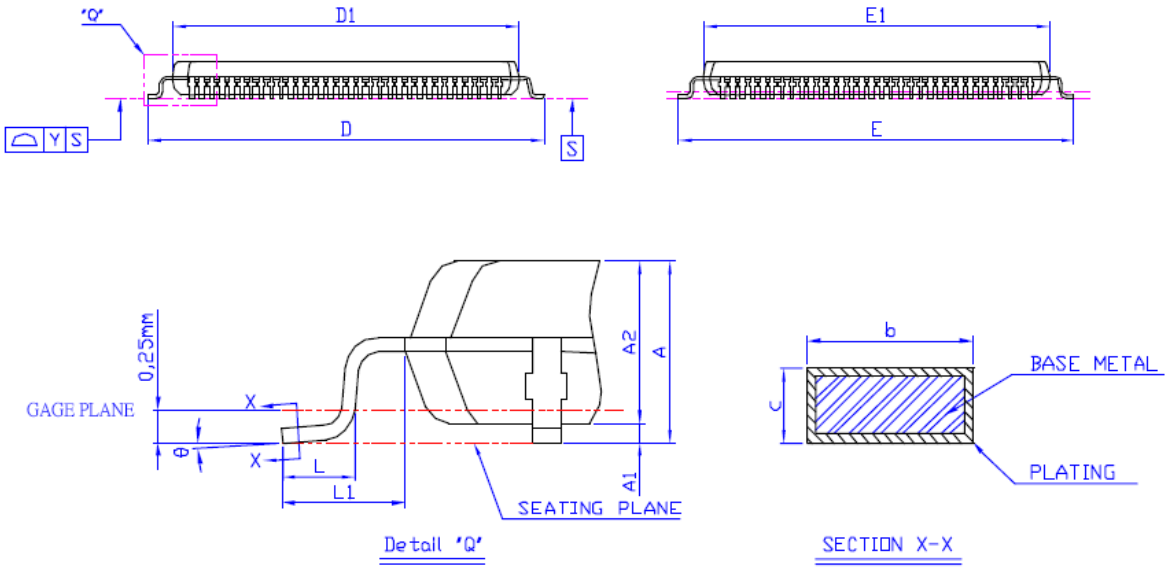
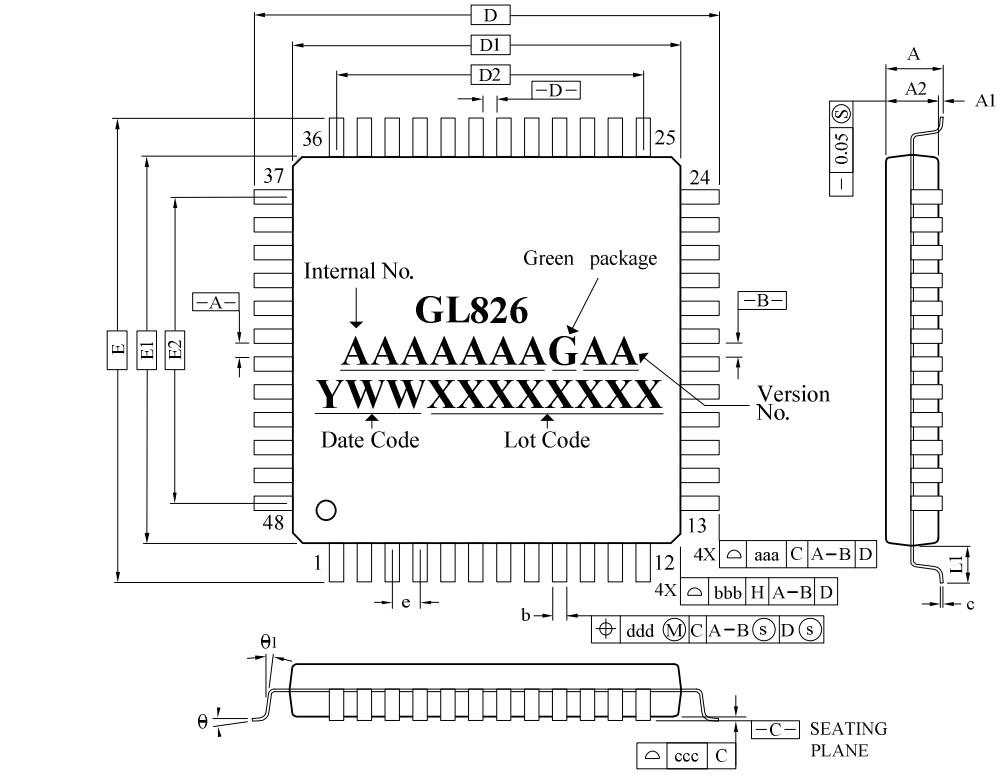
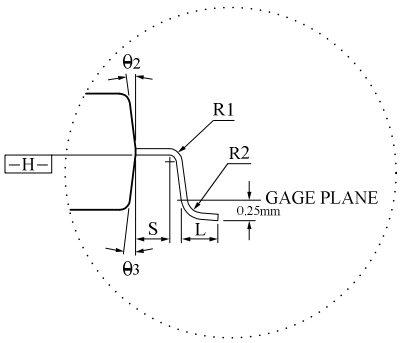


Figure 5.1－LQFP 128pin package





CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 5.2－LQFP 48pin package

CHAPTER 6 ORDERING INFORMATION

Table 6.1－Ordering Information

Part Number	Package	Green	Version	Status
GL826-MXG	128-pin LQFP	Green Package	XX	Available
GL826-MNG	48-pin LQFP	Green Package	XX	Available