Genesys Logic, Inc.

GL828

USB 2.0 SD/MMC Single Slot Card Reader Controller

Datasheet

Revision 1.02

Dec. 28, 2006

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Revision History

Revision	Date	Description
1.00	2006/10/11	First formal release
1.01	2006/11/01	Remove xD/MS/SM card description
1.02	2006/12/28	Delete ISP function

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CHAPTER 1 GENERAL DESCRIPTION

The GL828 is USB 2.0 Single Interface Flash Card Reader controller. It supports USB 2.0 high-speed transmission to Secure Digital™ (SD), Mini SD™, Micro SD™ , T-Flash , MultiMediaCard™ (MMC), RS MultiMediaCard™ (RS MMC), MMC Micro, HS-MMC, MMC-Mobile, on one chip. As a single chip solution for USB 2.0 flash card reader, the GL828 complies with Universal Serial Bus specification rev. 2.0, USB Storage Class specification ver.1.0, and flash card interface specification each.

The GL828 can support SD/MMC card interface in single slot. For the best performance consideration, the GL828 integrates high efficiency card interface hardware engine for data transfer.

The GL828 pin assignment design fits to card sockets to provide easier PCB layout. Package types are 48 Pin LQFP/LQFN (7mm x 7mm), the GL828 can fit your various design in standalone and PC embedded, MFP, TV … with USB 2.0 with SD/MMC single interface flash card reader/ writer applications.

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with 480Mbps Universal Serial Bus specification rev. 2.0.
  - Comply with USB Storage Class specification rev. 1.0.
  - Support 1 device address and up to 4 endpoints: Control (0)/ Bulk Read (1)/ Bulk Write (2)/Interrupt (3).
- Integrated USB building blocks
  - USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE), Build-in power-on reset (POR) and low-voltage detector (LVD)
- Embedded 8051 micro-controller
  - Operate @ 60 MHz clock, 12 clocks per instruction cycle
  - Embedded 48K Byte mask ROM and internal 256 byte SRAM
  - Embedded 4K Byte external SRAM
  - Support up to external 48K code ROM
- Secure Digital™ and MultiMediaCard™
  - Supports SD specification v1.0 / v1.1 / v2.0
  - Supports MMC specification v3.X / v4.0 / v4.1 / v4.2.
  - x1 / x4 / x8 data transmission.
  - Automatic CRC7 generation for command and CRC7 verification for response on CMD
  - Support automatic CRC16 generation and verification on DAT0:7
  - In addition to full packet transaction, optional single byte / bit operation on both CMD and DAT line / lines
  - Process data in block or byte
- On board 12 MHz Crystal driver circuit or 12/48 MHz Clock input.
- On-Chip 5V to 3.3V regulator. No external regulator required.
- On-Chip power MOSFETs for supplying flash media card power.
- Available in 48 Pin LQFP/LQFN (7x7 mm) package

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinout

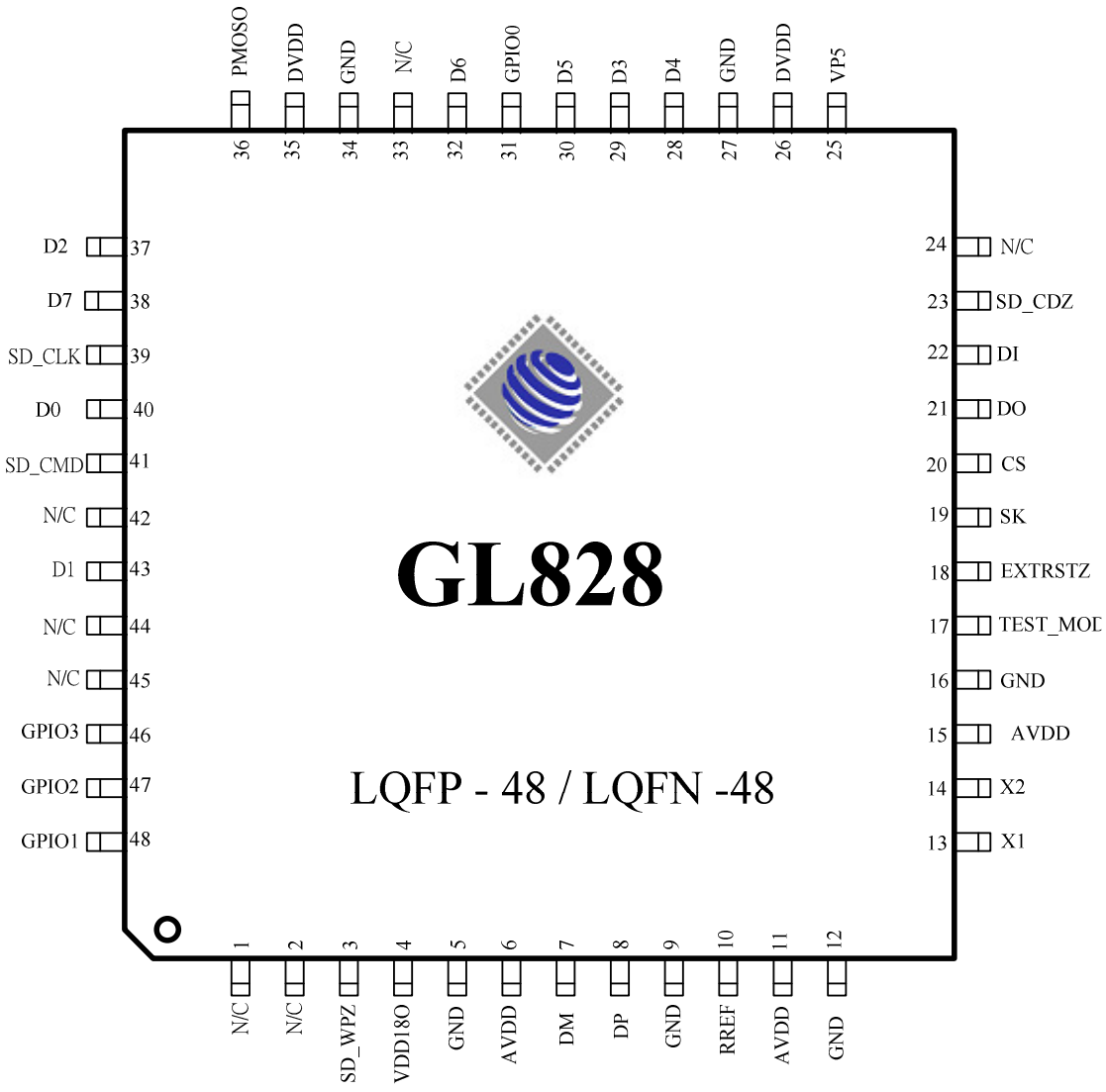


Figure 3.2 - 48 Pin LQFP/LQFN Pinout Diagram

3.2 Pin List

Table 3.1 – 48 Pin List

Pin #	GL828 Pin name	Type	Pin#	GL828 Pin name	Type	Pin#	GL828 Pin name	Type
1	N/C	–	17	TEST_MOD	I, pd	33	N/C	–
2	N/C	–	18	EXTRSTZ	I, pu	34	GND	Power
3	SD_WPZ	B/I, pu	19	SK	B/I, pd	35	DVDD	Power
4	VDD18O	Power	20	CS	B/I, pd	36	PMOSO	PMOS
5	GND	Power	21	DO	B/I, pd	37	D2	B/I, f
6	AVDD	Power	22	DI	B/I, pd	38	D7	B/I, f
7	DM	A	23	SD_CDZ	B/I, pd	39	SD_CLK	B/I, f
8	DP	A	24	N/C	–	40	D0	B/I, f
9	GND	Power	25	VP5	Power	41	SD_CMD	B/I, f
10	RREF	A	26	DVDD	Power	42	N/C	–
11	AVDD	Power	27	GND	Power	43	D1	B/I, f
12	GND	Power	28	D4	B/I, f	44	N/C	–
13	X1	OSC	29	D3	B/I, f	45	N/C	–
14	X2	OSC	30	D5	B/I, f	46	GPIO3	B/I, pd
15	DVDD	Power	31	GPIO0	B/I, pd	47	GPIO2	B/I, pd
16	GND	Power	32	D6	B/I, f	48	GPIO1	B/I, pd

3.3 Pin Descriptions

Table 3.2 - Pin Descriptions

Pin name	GL828 LQFP48 Pin	Type	Description
VDD18O	4	P	Internal regulator 1.8V output
GND	5,9,12	P	Analog ground
AVDD	6,11	P	Analog power
DM	7	A	USB D-
DP	8	A	USB D+
RREF	10	A	Reference resistor
X1	13	OSC	12MHz/48MHz input. This pin can be connected to one terminal of crystal or external 12MHz/48MHz clock source.
X2	14	OSC	12MHz/48MHz output. This is another terminal of the crystal or NC when using an external 12MHz/48MHz clock source is used to drive PLL.
DVDD	15,26,35	P	Digital power 3.3V
GND	16,27,34	P	Digital ground
VP5	25	P	Regulator 5V Input
PMOSO	36	PMOS	Power MOS 3.3V Output
TEST_MOD	17	I, pd	Test mode selection
EXTRSTZ	18	I, pu	External reset. It is active low. The low pulse should be 1 us width at least.
SD_CDZ	23	B/I, pd	SD& MMC Card detection. Normal High, active low.
D0~D7	40,43,37,29,28, 30,32,38	B/I, f	SD data 0~3 MMC data 0~7
SD_CLK	39	B/I, f	SD/MMC CLK
SD_WPZ	3	B/I, pu	SD Write Protect Detection. When no card is inserted, pull low. When SM or SD card is inserted, the pin is pull up and active low.
SD_CMD	41	B/I, f	SD/MMC CMD
GPIO0~3	41,48,47,46	B/I, pd	GPIO0~3 / GPIO3 : Power LED
SK	19	B/I, pd	93C46 Clock
CS	20	B/I, pd	93C46 CS
DO	21	B/I, pd	93C46 Data out
DI	22	B/I, pd	93C46 Data in / Access LED

Notation:

Type
- **A** Analog
- **B** Bi-directional
- **B/I** Bi-directional, default input
- **B/O** Bi-directional, default output
- **I** Input

O	Output
OSC	Oscillator
P	Power / Ground
f	Internal floating
pd	Internal pull down
pu	Internal pull up

CHAPTER 4 BLOCK DIAGRAM

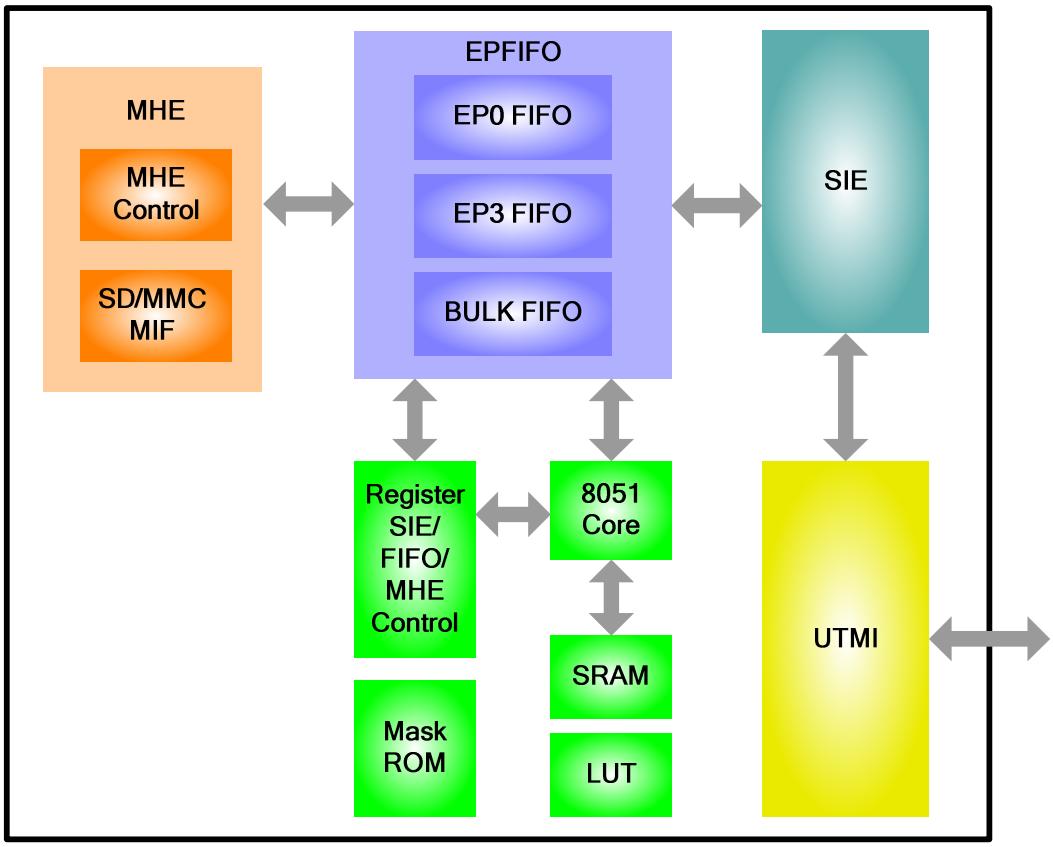


Figure 4.1 - Block Diagram

CHAPTER 5 FUNCTION DESCRIPTION

UTM

The USB 2.0 Transceiver Macrocell is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0), interrupt FIFO (FIFO3), Bulk In/Out FIFO (BULKFIFO)

- **Control FIFO** FIFO of control endpoint 0.
  It is 64-byte FIFO, and it is used for endpoint 0 data transfer.
- **Interrupt FIFO** 64-byte depth FIFO of endpoint 3 for status interrupt
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It contains ping-pong FIFO (512 bytes each bank) for transmit/receive data continuously.
  2. It can be directly accessed by Uc

MHE

It contains 1 MIF (Media Interface)

- **MIF**
  SD / MMC
- **Remote wakeup**
  Support Card insert wakeup while suspend.
- **External reset circuit**
  Non-inverting, Schmitt input with weak pull-up using DVDD power.

CLOCK Source Selection

It selects 12/48 MHz input by exterior pull resistor.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 6.1 - Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-65°C to +150 °C
Ambient Temperature	-40°C to +80 °C
Supply Voltage to Ground Potential	-0.5V to +4.0V
DC Input Voltage to Any Pin	-0.5V to +5.8V

6.2 Operating Conditions

Table 6.2 - Operating Conditions

Parameter	Value
Ta (Ambient Temperature Under Bias)	0°C to 70°C
Supply Voltage	+3.0V to +3.6V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	12 MHz ± 0.05% 12 MHz ± 0.25% (for USB full-speed only)

6.3 DC Characteristics

Table 6.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{REG}	Regulation Supply Voltage		4.5	-	5.5	V
V_{CC}	Supply Voltage		3.0	-	3.6	V
V_{IH}	Input High Voltage		2.0	-	3.6	V
V_{IL}	Input Low Voltage		-0.3	-	0.8	V
I_I	Input Leakage current	$0 < V_{IN} < V_{CC}$	-10	-	10	µA
V_{OH}	Output High Voltage		2.4	-	-	V
V_{OL}	Output Low Voltage		-	-	0.4	V
I_{OH}	Output Current High	VDD=3.3V V_{OH}=2.4V	-	8	-	mA
I_{OL}	Output Current Low	VDD=3.3V V_{OL}=0.4V	10	8	-	mA
C_{IN}	Input Pin Capacitance		-	5	-	pF
I_{SUSP}	Suspend current	1.5K external pull-up included	-	-	450	µA
I_{CC}	Supply current	Connect to USB with 8051 operating	-	-	60	mA

6.4 PMOS Characteristics

Table 6.4 - PMOS Driving Strength versus Junction Temperature

(Core Power=1.8V, IO Power=3.3V)

Junction Temperature	25 °C	80 °C	0 °C
Driving Strength (mA)	186.2 ± 10%	153.5 ± 10%	212.7 ± 10%
On-Resistance (ohm)	1.61 ± 10%	1.951 ± 10%	1.421 ± 10%

Note:
1. Driving strength is defined as the PMOS sinking current when Vio=3.3V, Vd=3.1V.
2. On-resistance is calculated by 0.2V divided by driving strength.

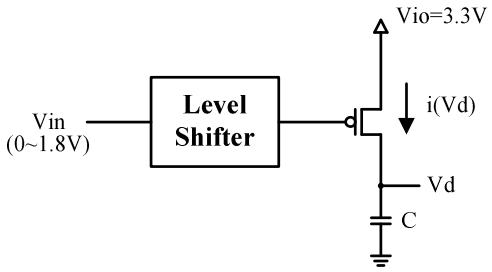


Figure 6.1 - Embedded PMOS Switch Architecture

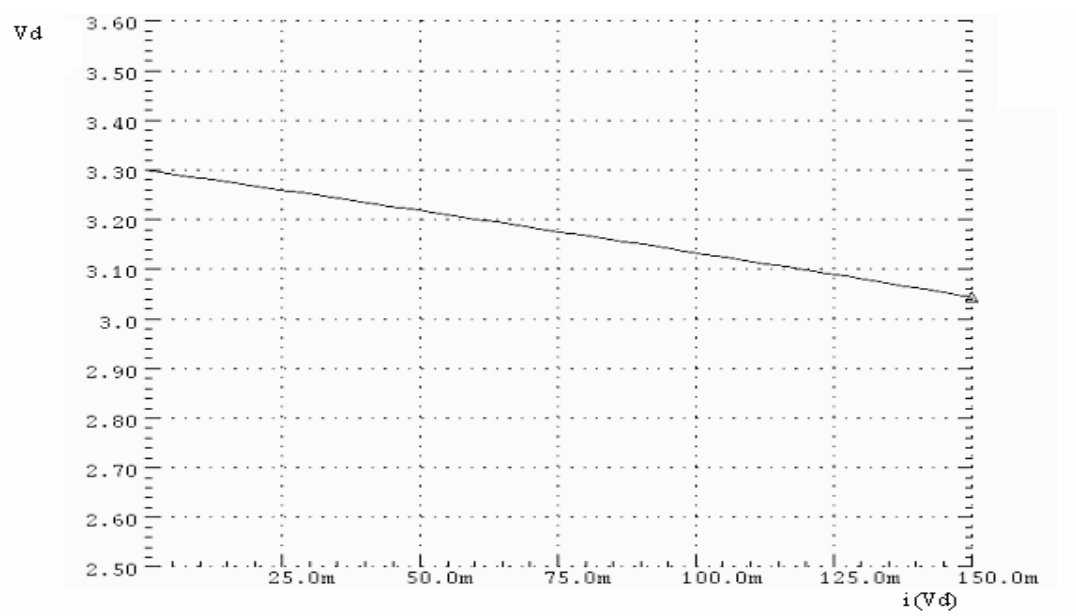


Figure 6.2 – V-I Curve of PMOS Switch @ 25 °C

6.5 5V to 3.3 V Regulator Characteristics

Table 6.5 – Regulator Output Current

Parameters	Description	Test Conditions	Min.	Type.	Max.	Units
Iq	Quiescent current	no loading	10	18	25	uA
Io_max	Output driving capability	Vout > 2.9V	200	500	600	mA
Vo_0mA	V33 voltage without loading	–	3.0	3.4	3.57	V
Vo_200mA	V33 voltage with 200mA load	–	2.9	3.34	3.52	V

6.6 AC Characteristics

6.6.1 UTMI Transceiver

The GL828 is fully compatible with Universal Serial Bus specification rev. 2.0 and USB 2.0 Transceiver Macercell Interface (UTMI) specification rev. 1.01. Please refer to the specifications for more information.

6.6.2 Secure Digital / MultiMediaCard

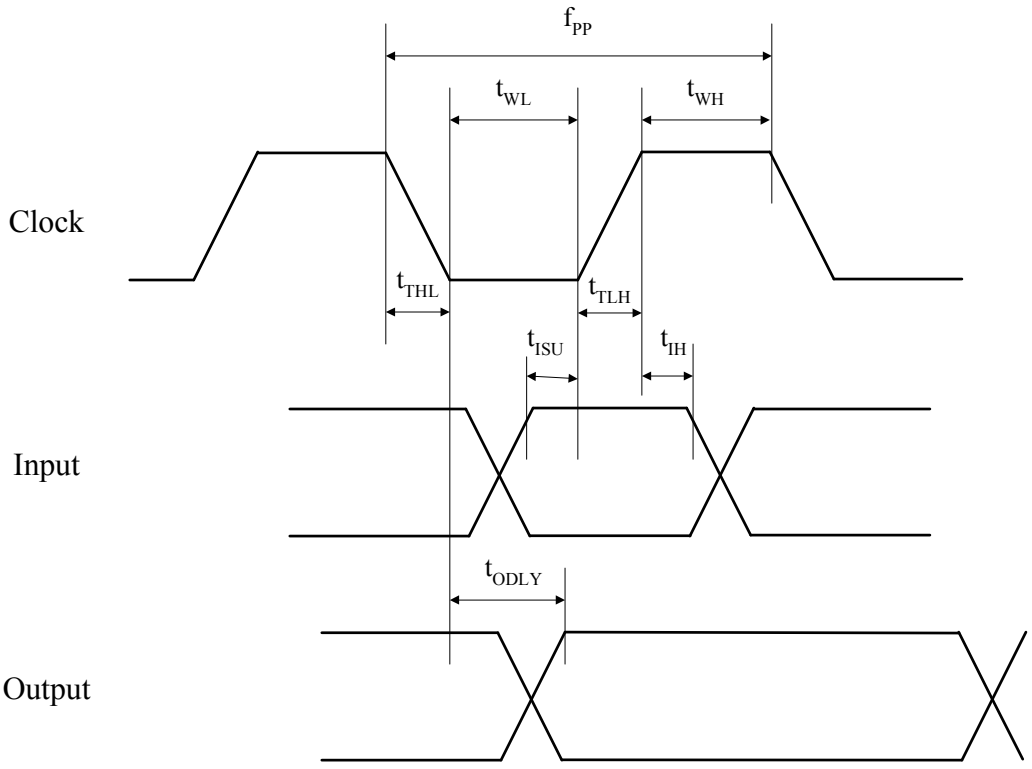


Figure 6.4 - Timing Diagram of Secure Digital / MultiMediaCard

SD Interface Timing (C_L = 30PF)

SYMBOL	PARAMETER	CLOCK RATE				UNIT
f_{PP}	Clock frequency Data Transfer Mode	48	20	15	6	MHz
f_{OD}	Clock frequency Identification Mode	375	375	375	375	KHz
t_{WL}	Clock low time (min)	7.4	22	30	80	ns
t_{WH}	Clock high time (min)	7.4	22	30	80	ns
t_{TLH}	Clock rise time (max)	3	3	3	3	ns
t_{THL}	Clock fall time (max)	3	3	3	3	ns
t_{ISU}	Input set-up time (min)	6.6	19.8	27	72	ns
t_{IH}	Input hold time (min)	6.6	19.8	27	72	ns
t_{ODLY}	Output delay time (max)	2	2	2	2	ns

6.6.3 Reset Timing

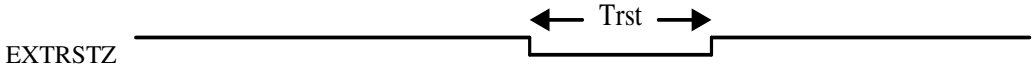


Figure 6.5 - Timing Diagram of Reset width

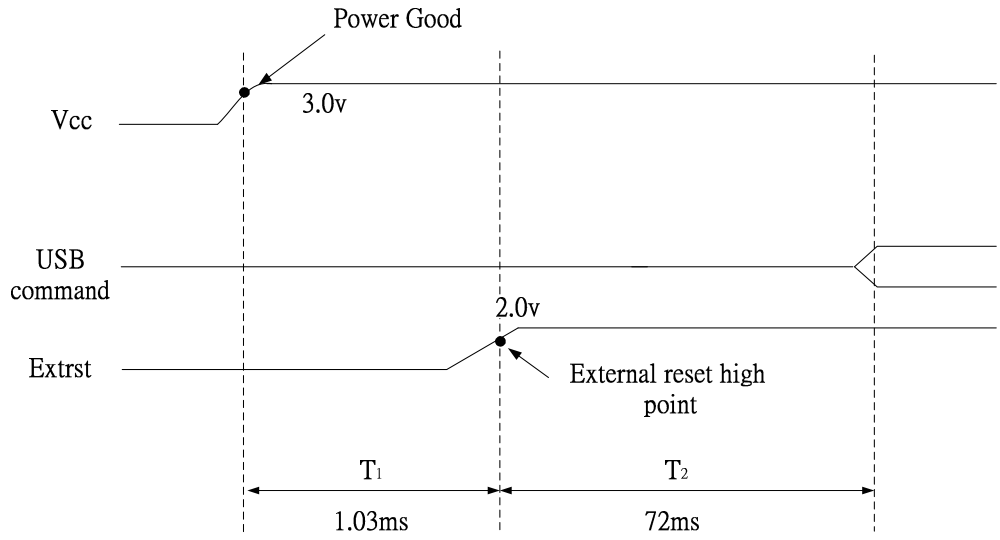


Figure 6.6 - Timing Diagram of Power Good to USB command receive ready

Parameter	Description	Min	Typ	Max	Unit
Trst	Chip reset sense timing width	2	—	—	us
T1	External reset valid from power up to high	1.03	—	—	ms
T2	Reset Deassertion to respond USB command ready	72	—	—	ms

6.6.4 EEPROM 93C46 Timing

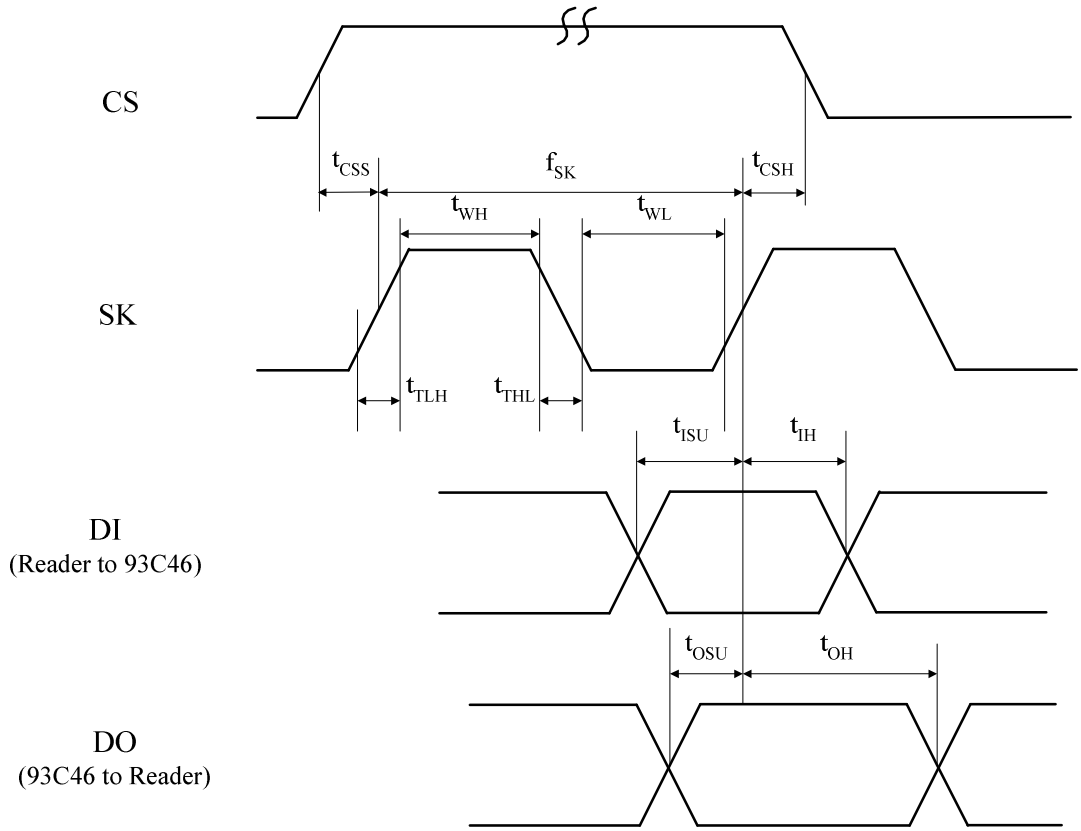


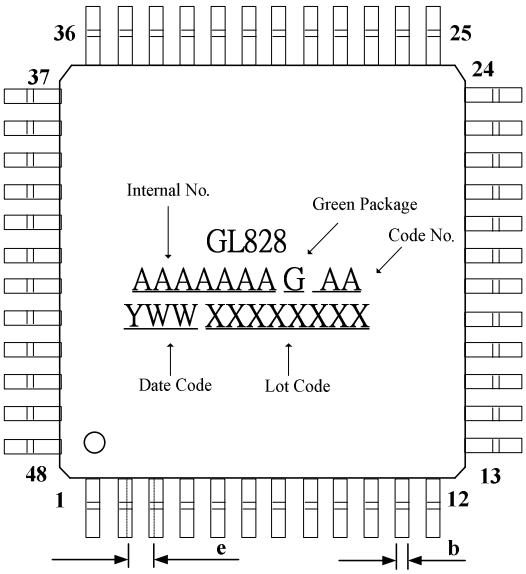
Figure 6.7 - Timing Diagram of EEPROM 93C46

AC Characteristics of 93C46 Interface (with C_{LOAD} = 15 pF)

PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNIT
f_{SK}	SK clock frequency	200k	400k	Hz
t_{WH}	SK H pulse length	500	—	ns
t_{WL}	SK L pulse length	500	5	ns
t_{TLH}	SK rise time	—	10	ns
t_{THL}	SK fall time	—	10	ns
t_{CSS}	CS setup time	1	—	µs

t_{CSH}	CS hold time	1	–	µs
t_{ISU}	DI setup time	1	–	µs
t_{IH}	DI hold time	1	–	µs
t_{OSU}	DO setup time	5	–	ns
t_{OH}	DO hold time	5	–	ns

CHAPTER 7 PACKAGE DIMENSION



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A			1.60(63)
A1	0.05(2)		0.15(6)
A2	1.35(53)	1.40(55)	1.45(57)
b	0.17(7)	0.22(9)	0.27(11)
c	0.09(4)		0.20(8)
D	9.00 (354) BSC		
D1	7.00 (276) BSC		
E	9.00 (354) BSC		
E1	7.00 (276) BSC		
e	0.50 (20) BSC		
L	0.45(18)	0.60(24)	0.75(30)
L1	1.00 (39) REF		
Y			0.10(4)
θ	0°	3.5°	7°

NOTE: 1.REFER TO JEDEC MS-026/BBC

2.ALL DIMENSIIONS IN MILLIMETERS.

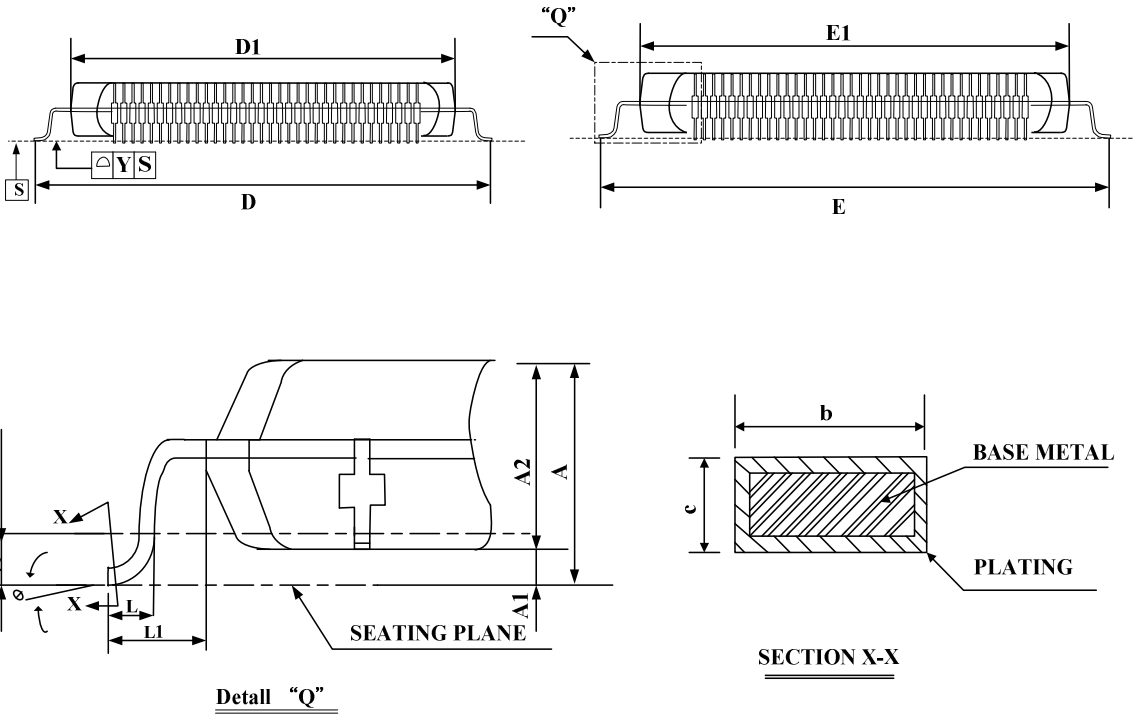


Figure 7.1 - GL828 48 Pin LQFP Package

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.61 (24)	0.66 (26)	0.70 (28)
A1	0.00 (0)	0.02 (0.8)	0.05 (2)
A3	0.13 (5) REF		
b	0.18 (7)	0.25 (10)	0.30 (12)
D	7.00 (276) BSC		
E	7.00 (276) BSC		
D2	5.10 (201)	5.20 (205)	5.30 (209)
E2	5.10 (201)	5.20 (205)	5.30 (209)
e	0.50 (20) BSC		
L	0.30 (12)	0.40 (16)	0.50 (20)
y	---	0.08 (3)	---
k	0.20 (8)	---	---

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.

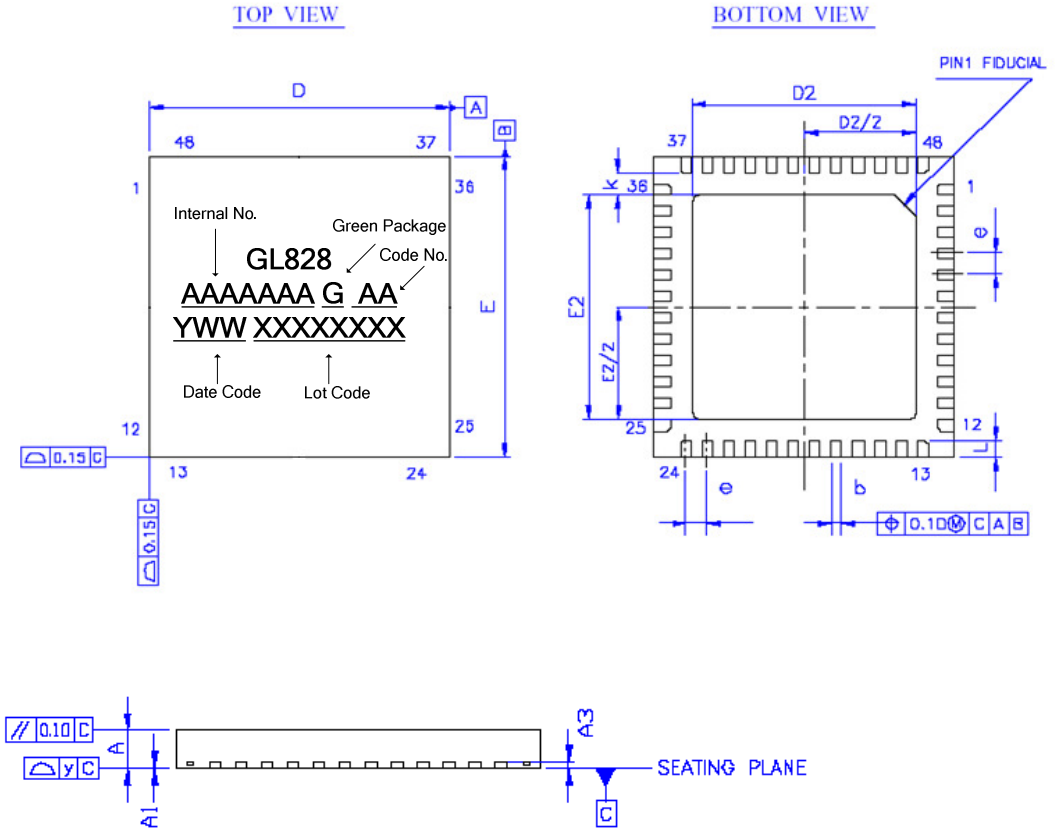


Figure 7.2 - GL828 48 Pin LQFN Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Normal/Green	Version	Status
GL828-MNG	48-pin LQFP	Green Package	XX	Available
GL828-PNG	48-pin LQFN	Green Package	XX	Available