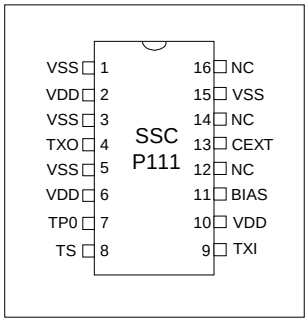
SSC P111

PL Media Interface IC, CEBus Compliant

Features

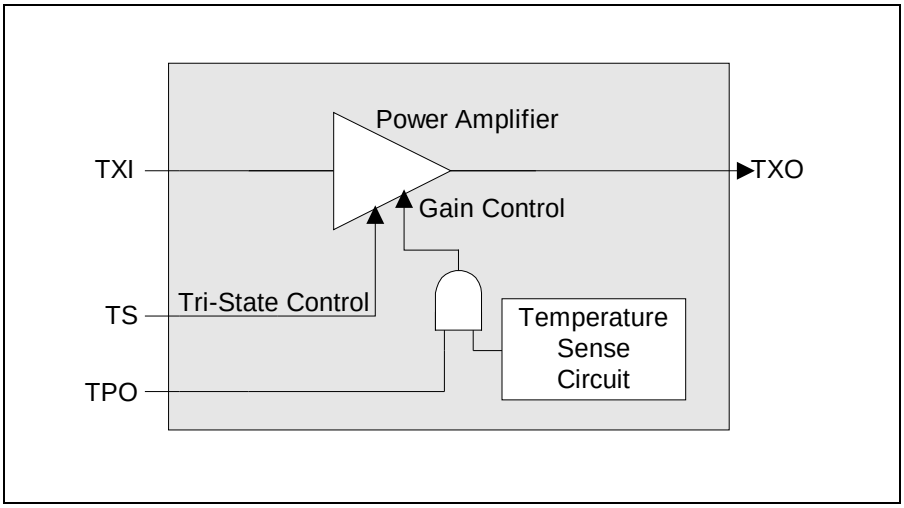
- Integrates Power Amplifier, and Tri-state functions for CEBus Power Line (PL) physical interfaces
- Replaces approximately 30 discrete components to save board space and increase reliability
- Implements high-drive Output Amplifier (6 Vp-p into 10 ohm load) to increase performance under low impedance conditions
- Output Amplifier is a Class AB configuration for increased efficiency and lower power consumption
- Incorporates built-in over temperature protection circuit for improved system reliability
- Serves as companion IC to Intellon SSC P300 and SSC P200 Network Controller ICs
- 16 pin SOIC package



Introduction

The SSC P111 PL Media Interface IC provides the functions of Output Power Amplifier and Output Tri-state Switch for power line transceiver products. The Output Power Amplifier meets the requirements specified by the EIA-600 (CEBus Standard) for output voltage levels into typical and low impedance power line loads and incorporates over-temperature protection for improved system reliability. The IC replaces approximately 30 of the discrete components normally used in support of PL transceivers and reduces required printed circuit board area by up to 50%.

SSC P111 Block Diagram



SSC P111 Description

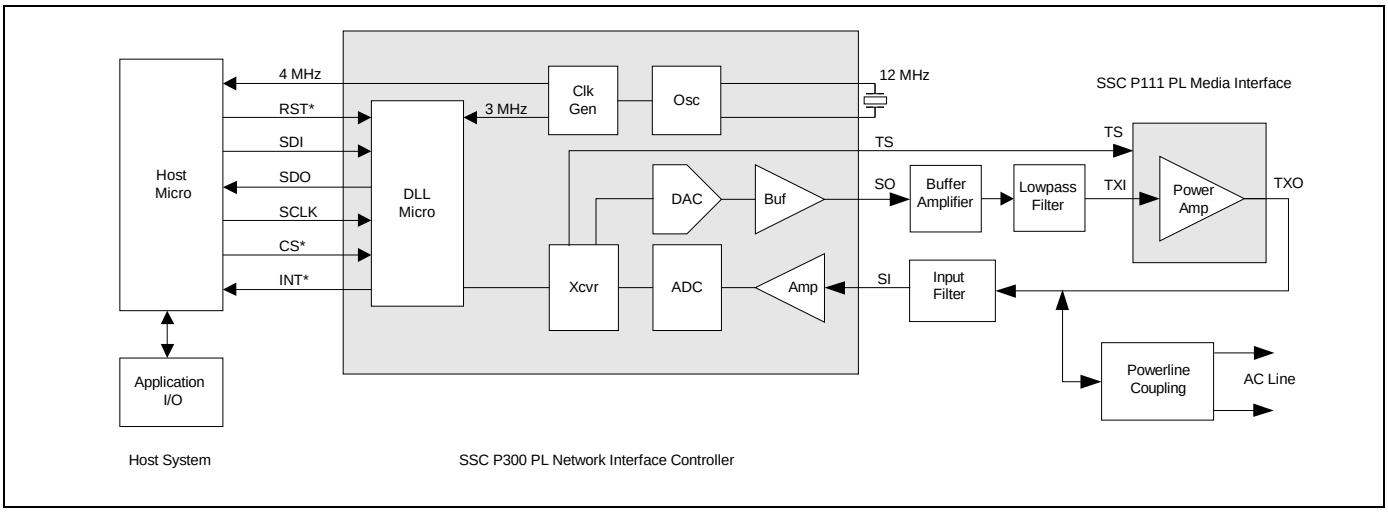
In an SSC P111 design the Signal Out (SO) from the SSC P300 or P200 is buffered and filtered before entering the P111 Power Amplifier. The output waveform is amplified by the Power Amplifier and then applied to the external Power Line Coupling/Filter network. Received power line analog signals pass through the external power line Coupling/Filter network to the Input Filter. This bandpass filter passes the chirp frequency band (100 to 400 kHz) to the SSC P300 or P200 SI input pin. The Tri-state (TS) signal from the SSC P300 or P200 disconnects the SSC P111 IC Power Amplifier from the coupling network when the system is in the receive mode and places the SSC P111 Power Amplifier in a power-down state. The Temp Sense circuitry reduces the Power Amplifier fixed gain from 2 to 1, which will lower the output transistor power dissipation under output overload conditions.

Specifications

Symbol	Parameter	Min	Typical	Max	Unit	Notes
Z_{IN}(PA)	Power Amplifier Input Resistance	1.4	2	2.7	KΩ	
A_V(PA)	Power Amplifier Voltage Gain	1.8	2	2.2	V/V	
V_{IN}(PA)	Input Voltage range of Power Amplifier		3	3.5	Vac	
PM(PA)	Phase Margin of Power Amplifier		78		Deg	
G_{BW}(PA)	Gain Bandwidth of Power Amplifier	1.1		2.1	MHz	
V_{IH}	Minimum High-level Input Voltage	4.0			V	(1)
V_{IL}	Maximum Low-level Input Voltage			0.5	V	(1)
I_{IL}	Maximum Input Leakage Current			+/-10	µA	(1)
Hys	Minimum Input Hysteresis	350			mV	(1)
T_{enbl}	TS to Power Amp output signal valid			500	ns	
T_{disabl}	TS to Power Amp output tristate			50	ns	
I_{DD} (TX)	Supply Current (Transmit)		140	250	mA	(2)
I_{DD} (RX)	Supply Current (Receive)		10	20	mA	
	Latchup	150			mA	(3)

Notes: 1) Input Signal TS 2) Typical value for driving 10 Ohm, AC coupled load 3) JEDEC JC-40.2

Typical Application Using SSC P111 IC with SSC P300



Ordering Information

Part No.	Description	Tube Qty.	Package
SSC P111	PL Media Interface IC, CEBus Compliant	45	16 pin SOIC