# AU6980

## USB2.0 Universal Flash Disk Controller

# Technical Reference Manual

# AU6980

USB2.0 Universal Flash Disk Controller

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## Revision History

| Date | Revision | Description |
|---|---|---|
| Mar 2006 | 1.00W | Official Release. |
| Aug 2006 | 1.01W | Modify "5.0 Electrical Characteristics" information |
| Oct 2006 | 1.02W | Add GHL bonding information |
| June 2007 | 1.03W | Modify 3.1 Pin Descriptions-P7(External 330 Resister to Ground) Modify 3.2 Pin Descriptions-P5(External 330 Resister to Ground) |

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**\<Memo\>**

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# 1. Introduction
## 1.1 Description

The AU6980 USB 2.0 Flash Disk Controller is one of the best solutions for all kinds of SLC (Single- Level Cell) and MLC (Multi-Level Cell) NAND and AG-AND with multiple dies data flashes. The ability to support new flash in the market is powerful and in time. Its high-speed read and write access performance enable users to transfer and backup data effectively. Besides, AU6980 is certified by USB-IF (USB Implementers Forum), WHQL (Window Hardware Quality Labs) and EMI tests to guarantee the quality and reliability for end-users.

The multi-function single chip AU6980 provides dual channel access and ISP (In-System Programming) technologies, which are the most important features to allow manufacturers building high performance UFD easily. In addition to being a removable storage device, AU6980 can also be configured as a bootable disk for system recovery..

To enhance the usefulness and manageability of UFD further, Alcor Micro develops a smart application program iStar (Partition/Password Operation Tool) as a handy utility in managing partition, password and security. Having iStar as the companion of UFD, not only the data in a UFD could be protected from unauthorized access, but also the PC computer could be completely locked out from people who do not have the specific UFD. This feature increases the value of a UFD and leads users to the new security generation at the same time.

## 1.2 Features

- Supports dual channel mode for high-speed transfer.
- Supports firmware upgrade mechanism (ISP, In-System Programming)
- Integrates hardware DMA engine to tune up the operation performance
- Integrates multi-bit ECC correction mechanism
- Complies with the standards defined in USB v2.0, USB Device Class Definition for Mass Storage and Bulk-Transport v1.0
- Works with default driver under the environments of Windows ME, Windows 2000, Windows XP, Mac 9.2, Mac OS X. Using Alcor Micro's vendor driver for the environment under Windows 98SE
- Concurrent bus operation using multiple FIFO for better performance
- Integrates into flash memory power control switch
- Supports bad block management
- Supports dynamic serial number modification via mass production software
- Supports software write protection
- Companion application program with UFD – iStar available for users
  - ➢ To have UFD partition management function
  - ➢ To do password protection for the security in data access
  - ➢ To guard data files with software write protection function
  - ➢ To lock up PC by UFD as the key
- Available in 48-pin LQFP package, 64-pin LQFP package to support 4CE pin flash

# 2. Application Block Diagram

The following figure shows the application diagram of a typical flash disk product with AU6980. By connecting the flash disk to a desktop or notebook PC through USB bus, AU6980 is then turned into a bus-powered, high speed USB disk, which can be used as a bridge for data transfer between Desktop PC and Notebook PC

## Figure 2.1 Block Diagram

PC with USB Host Controller

PC with USB Host Controller          Notebook  with USB Host Controller
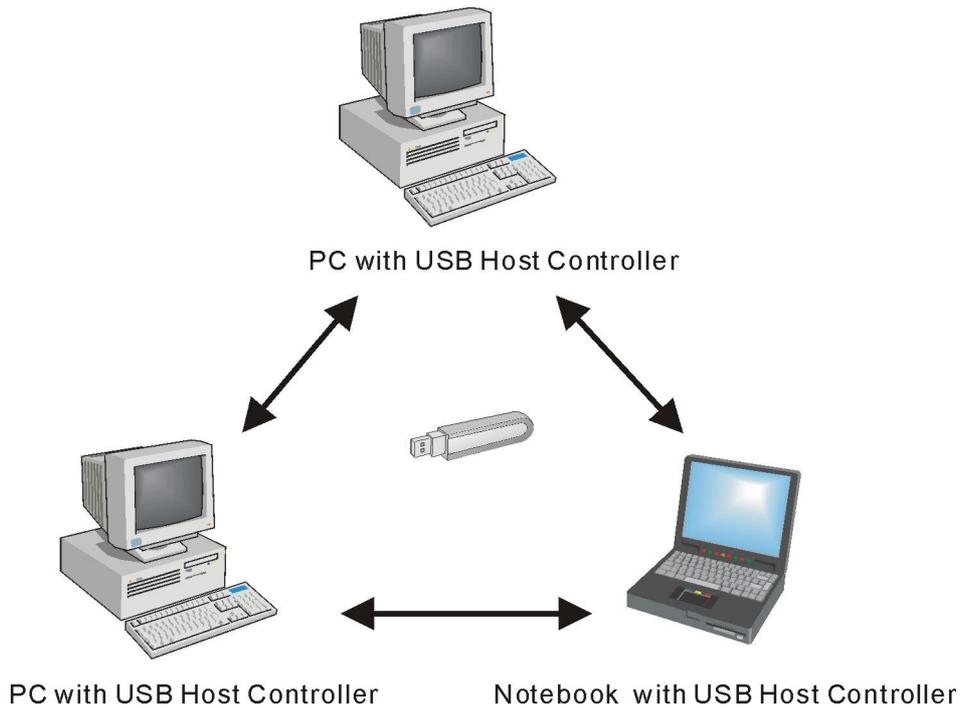
# 3. Pin Assignment

Depending on the application, the AU6980 is available in two different packages. Below figure shows signal name for each pin and the table in the page after describes each pin in detail.

**Figure 3.1 AU6980-GDL Pin Assignment Diagram**
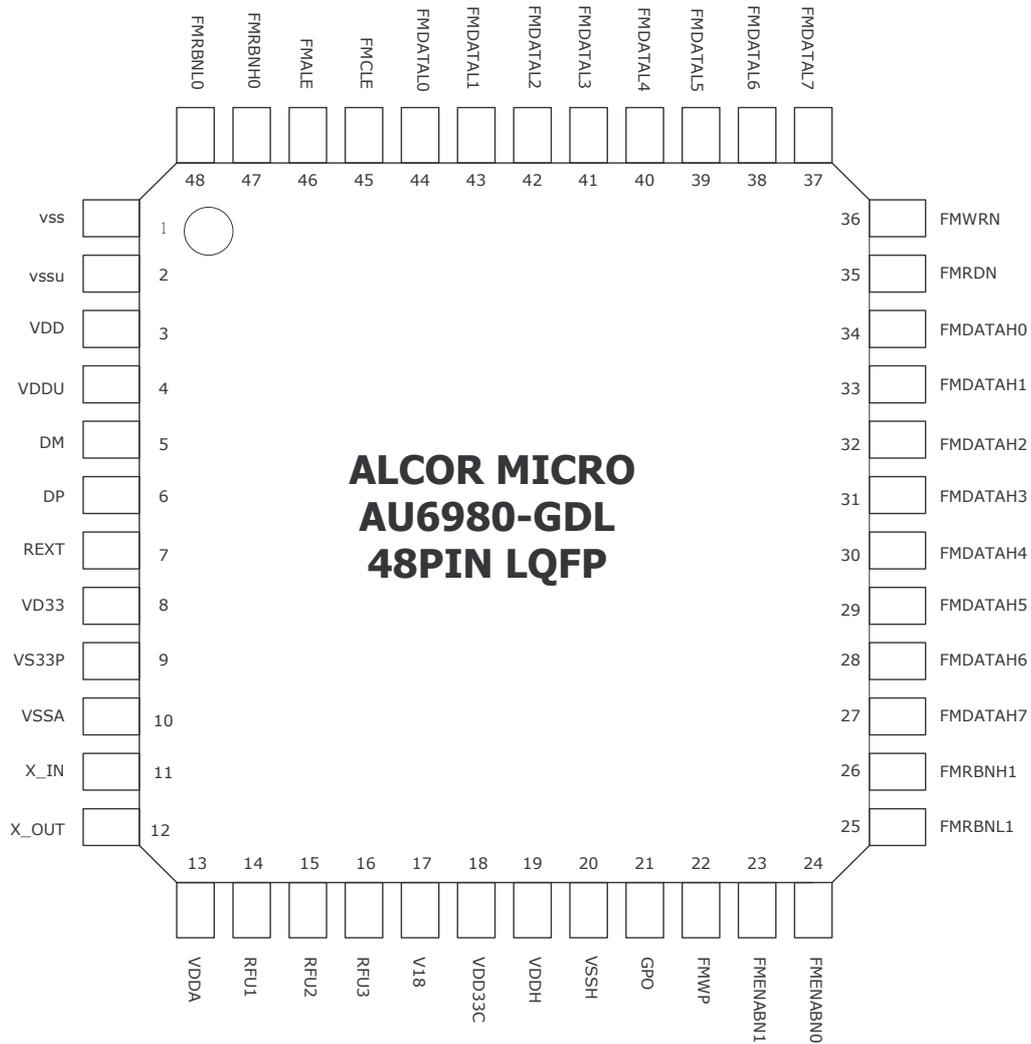
## Table 3.1 AU6980-GDL Pin Descriptions

| Pin # | Pin Name | I/O | Description |
|-------|----------|-----|-------------|
| 1 | VSS | GND | Ground |
| 2 | VSSU | GND | Ground |
| 3 | VDD | I | 1.8V Power Source for Core |
| 4 | VDDU | I | 1.8V Power Source for UTMI |
| 5 | DM | I/O | USB DM |
| 6 | DP | I/O | USB DP |
| 7 | REXT | I | External 330 Resister to Ground |
| 8 | VD33 | I | 3.3V Power Source for UTMI |
| 9 | VS33P | GND | Ground |
| 10 | VSSA | GND | Ground |
| 11 | X_IN | I | 12 MHz crystal input. |
| 12 | X_OUT | O | 12 MHz crystal output. |
| 13 | VDDA | I | 1.8V Power Source for PLL |
| 14 | RFU1 | | Reserved |
| 15 | RFU2 | | Reserved |
| 16 | RFU3 | | Reserved |
| 17 | V18 | O | 1.8V Power Out |
| 18 | VDD33C | O | 3.3V Power Out for Flash Memory |
| 19 | VDDH | I | 3.3V Power Source for IO pad |
| 20 | VSSH | GND | Ground |
| 21 | OPLED | O | General Purpose OutPut |
| 22 | FMWP | I | Flash Memory Write Protect; High Active |
| 23 | FMENABN1 | I/O | Flash Memory #1 Enable; Low Active |
| 24 | FMENABN0 | I/O | Flash Memory #0 Enable; Low Active |
| 25 | FMRBNL1 | I | Flash Memory(L1) Ready and Busy Signal (1=Ready ; 0=Busy) |
| 26 | FMRBNH1 | I | Flash Memory(H1) Ready and Busy Signal (1=Ready ; 0=Busy) |
| 27 | FMDATAH7 | I/O | Flash Memory DataH[7] |
| 28 | FMDATAH6 | I/O | Flash Memory DataH[6] |
| 29 | FMDATAH5 | I/O | Flash Memory DataH[5] |

| Pin # | Pin Name | I/O | Description |
|:---:|:---:|:---:|:---|
| 30 | FMDATAH4 | I/O | Flash Memory DataH[4] |
| 31 | FMDATAH3 | I/O | Flash Memory DataH[3] |
| 32 | FMDATAH2 | I/O | Flash Memory DataH[2] |
| 33 | FMDATAH1 | I/O | Flash Memory DataH[1] |
| 34 | FMDATAH0 | I/O | Flash Memory DataH[0] |
| 35 | FMRDN | I/O | Flash Memory Read Enable; Low Active |
| 36 | FMWRN | I/O | Flash Memory Write Enable; Low Active |
| 37 | FMDATAL7 | I/O | Flash Memory DataL[7] |
| 38 | FMDATAL6 | I/O | Flash Memory DataL[6] |
| 39 | FMDATAL5 | I/O | Flash Memory DataL[5] |
| 40 | FMDATAL4 | I/O | Flash Memory DataL[4] |
| 41 | FMDATAL3 | I/O | Flash Memory DataL[3] |
| 42 | FMDATAL2 | I/O | Flash Memory DataL[2] |
| 43 | FMDATAL1 | I/O | Flash Memory DataL[1] |
| 44 | FMDATAL0 | I/O | Flash Memory DataL[0] |
| 45 | FMCLE | O | Flash Memory Command Latch Enable ;High Active |
| 46 | FMALE | O | Flash Memory Address Latch Enable; High Active; |
| 47 | FMRBNH0 | I | Flash Memory(H0) Ready and Busy Signal (1=Ready ; 0=Busy) |
| 48 | FMRBNL0 | I | Flash Memory(L0) Ready and Busy Signal (1=Ready ; 0=Busy) |

The following figure shows signal name of each pin in 48-pin package and the table in the page after describes each pin in detail.

## Figure 3.2 AU6980-GHL Pin Assignment Diagram
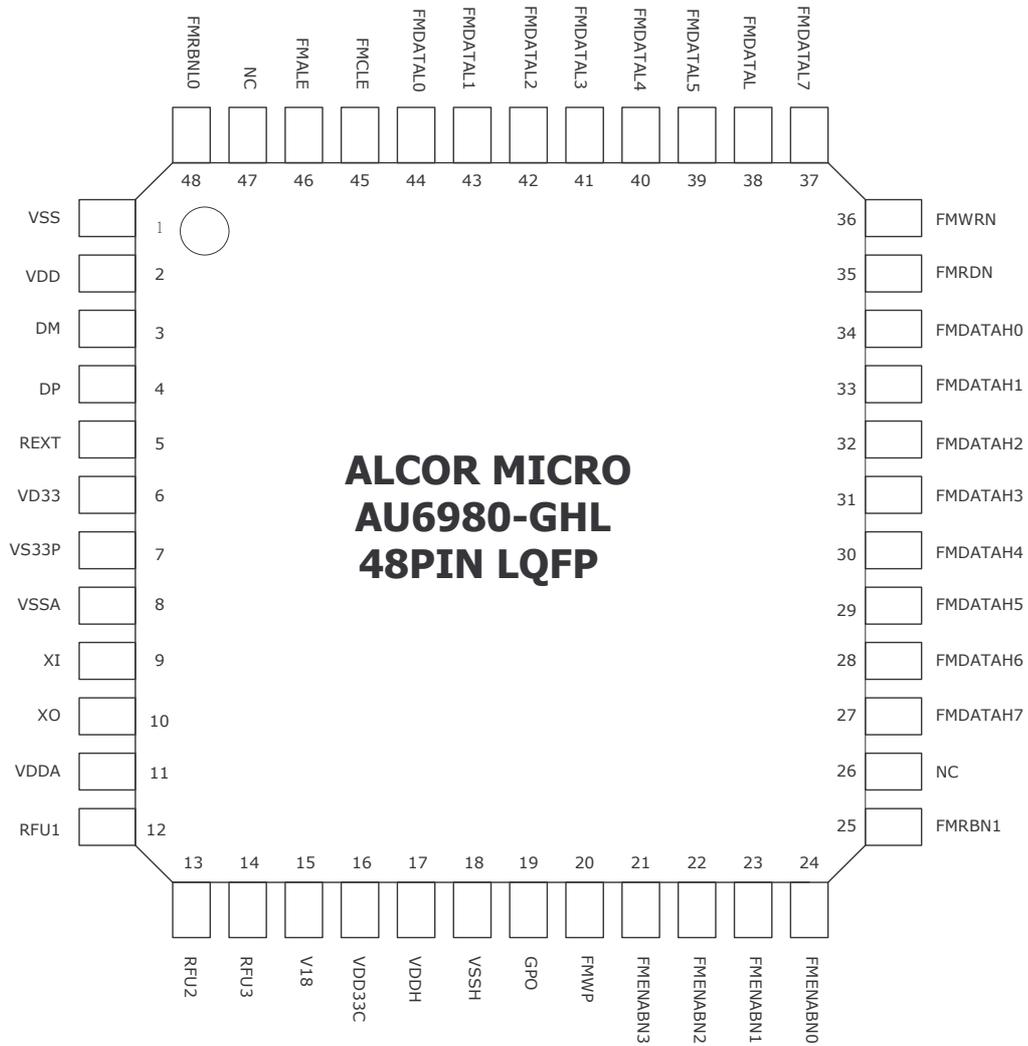
## Table 3.2 AU6980-GHL Pin Descriptions

| Pin # | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | VSS | GND | Ground |
| 2 | VDD | I | 1.8V Power Source for Core |
| 3 | DM | I/O | USB DM |
| 4 | DP | I/O | USB DP |
| 5 | REXT | I | External 330 Resister to Ground |
| 6 | VD33 | I | 3.3V Power Source for UTMI |
| 7 | VS33P | GND | Ground |
| 8 | VSSA | GND | Ground |
| 9 | XI | I | 12 MHz crystal input. |
| 10 | XO | O | 12 MHz crystal output. |
| 11 | VDDA | I | 1.8V Power Source for PLL |
| 12 | RFU1 | | Reserved |
| 13 | RFU2 | | Reserved |
| 14 | RFU3 | | Reserved |
| 15 | V18 | O | 1.8V Power Out for Core |
| 16 | VDD33C | O | 3.3V Power Out for Flash Memory |
| 17 | VDDH | I | 3.3V Power Source for IO pad |
| 18 | VSSH | GND | Ground |
| 19 | GPO | O | General Purpose OutPut |
| 20 | FMWP | I | Flash Memory Write Protect; High Active |
| 21 | FMENABN3 | I/O | Flash Memory #3 Enable; Low Active |
| 22 | FMENABN2 | I/O | Flash Memory #2 Enable; Low Active |
| 23 | FMENABN1 | I/O | Flash Memory #1 Enable; Low Active |
| 24 | FMENABN0 | I/O | Flash Memory #0 Enable; Low Active |
| 25 | FMRBN1 | I | Flash Memory(L1) Ready and Busy Signal (1=Ready ; 0=Busy) |
| 26 | NC | | |
| 27 | FMDATAH7 | I/O | Flash Memory DataH[7] |
| 28 | FMDATAH6 | I/O | Flash Memory DataH[6] |
| 29 | FMDATAH5 | I/O | Flash Memory DataH[5] |

| Pin # | Pin Name | I/O | Description |
|---|---|---|---|
| 30 | FMDATAH4 | I/O | Flash Memory DataH[4] |
| 31 | FMDATAH3 | I/O | Flash Memory DataH[3] |
| 32 | FMDATAH2 | I/O | Flash Memory DataH[2] |
| 33 | FMDATAH1 | I/O | Flash Memory DataH[1] |
| 34 | FMDATAH0 | I/O | Flash Memory DataH[0] |
| 35 | FMRDN | I/O | Flash Memory Read Enable; Low Active |
| 36 | FMWRN | I/O | Flash Memory Write Enable; Low Active |
| 37 | FMDATAL7 | I/O | Flash Memory DataL[7] |
| 38 | FMDATAL6 | I/O | Flash Memory DataL[6] |
| 39 | FMDATAL5 | I/O | Flash Memory DataL[5] |
| 40 | FMDATAL4 | I/O | Flash Memory DataL[4] |
| 41 | FMDATAL3 | I/O | Flash Memory DataL[3] |
| 42 | FMDATAL2 | I/O | Flash Memory DataL[2] |
| 43 | FMDATAL1 | I/O | Flash Memory DataL[1] |
| 44 | FMDATAL0 | I/O | Flash Memory DataL[0] |
| 45 | FMCLE | O | Flash Memory Command Latch Enable ;High Active |
| 46 | FMALE | O | Flash Memory Address Latch Enable; High Active; |
| 47 | NC | | |
| 48 | FMRBN0 | I | Flash Memory(L0) Ready and Busy Signal (1=Ready ; 0=Busy) |

# 4. System Architecture and Reference Design

## 4.1 AU6980 Block Diagram

**Figure 4.1 AU6980 Block Diagram**
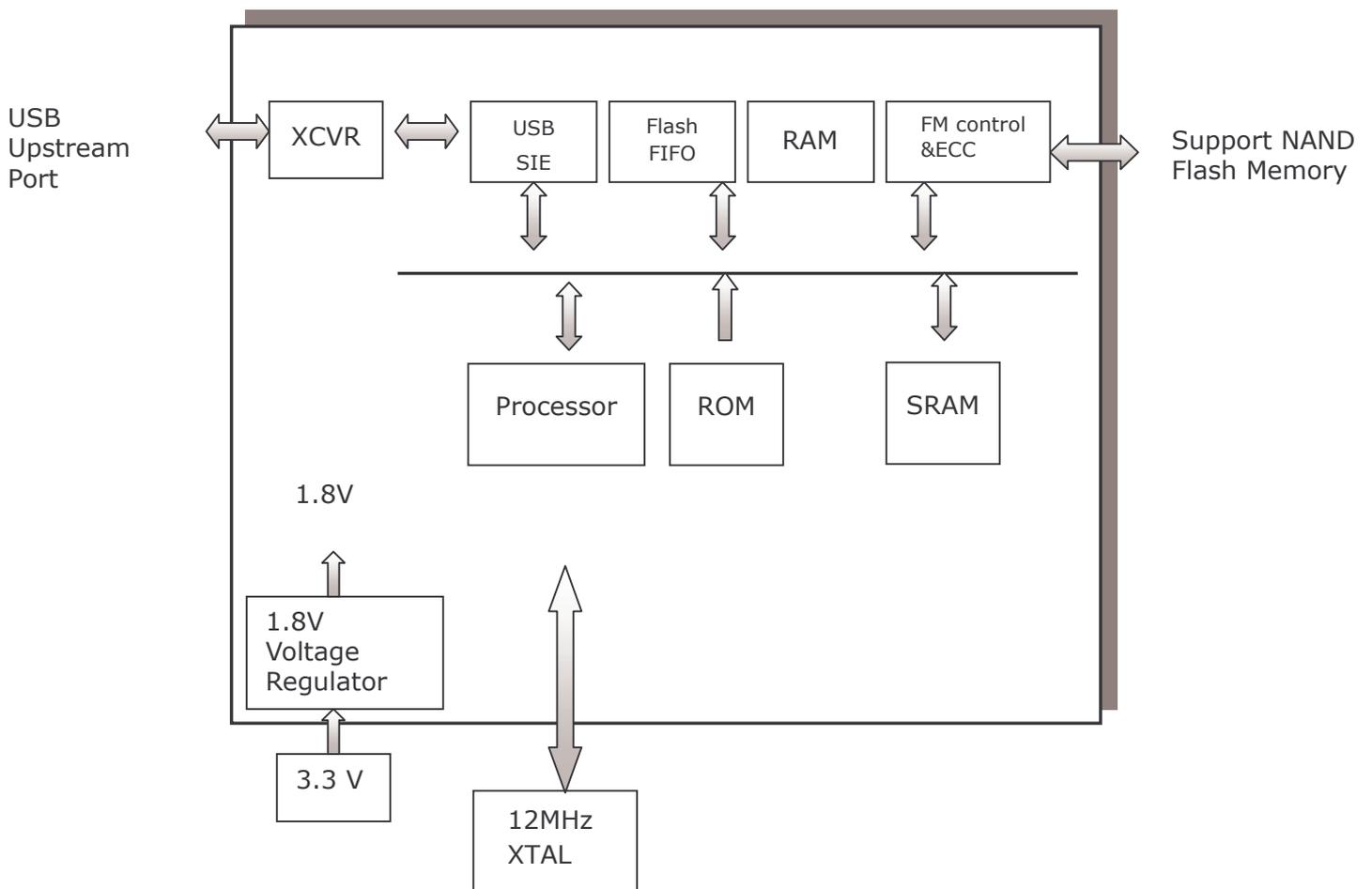
# 5. Electrical Characteristics

## 5.1 Absolute Maximum Ratings

### Table 5.1 Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units |
|---|---|---|---|
| $V_{DDH}$ | Power Supply | -0.3 to $V_{DDH}$ +0.3 | V |
| $V_{IN}$ | Input Signal Voltage | -0.3 to 3.6 | V |
| $V_{OUT}$ | Output Signal Voltage | -0.3 to $V_{DDH}$ +0.3 | V |
| $T_{STG}$ | Storage Temperature | -40 to 150 | $^{O}C$ |

## 5.2 Recommended Operating Conditions

### Table 5.2 Recommended Operating Conditions

| Symbol | Parameter | Min. | Tpy. | Max. | Units |
|---|---|---|---|---|---|
| $V_{DDH}$ | Power Supply | 3.0 | 3.3 | 3.6 | V |
| $V_{DD}$ | Digital Supply | 1.62 | 1.8 | 1.98 | V |
| $V_{IN}$ | Input Signal Voltage | 0 | 3.3 | 3.6 | V |
| $T_{OPR}$ | Operating Temperature | 0 | | 70 | $^{O}C$ |

## 5.3 General DC Characteristics

### Table 5.3 General DC Characteristics

| Symbol | Parameter | Conditions | Min. | Tpy. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IN}$ | Input current | No pull-up or pull-down | -10 | $\pm1$ | 10 | $\mu A$ |
| $I_{OZ}$ | Tri-state leakage current | | -10 | $\pm1$ | 10 | $\mu A$ |
| $C_{IN}$ | Input capacitance | Pad Limit | | 2.8 | | $\rho F$ |
| $C_{OUT}$ | Output capacitance | Pad Limit | | 2.8 | | $\rho F$ |
| $C_{BID}$ | Bi-directional buffer capacitance | Pad Limit | | 2.8 | | $\rho F$ |

## 5.4 DC Electrical Characteristics of 3.3V I/O Cells

### Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

| Symbol | Parameter | Conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{DDH}$ | Power supply | 3.3V I/O | 3.0 | 3.3 | 3.6 | V |
| $V_{il}$ | Input low voltage | LVTTL | | | 0.8 | V |
| $V_{ih}$ | Input high voltage | | 2.0 | | | V |
| $V_{ol}$ | Output low voltage | $\mid I_{ol}\mid$ =2~16mA | | | 0.4 | V |
| $V_{oh}$ | Output high voltage | $\mid I_{oh}\mid$ =2~16mA | 2.4 | | | V |
| $R_{pu}$ | Input pull-up resistance | PU=high, PD=low | 55 | 75 | 110 | K$\Omega$ |
| $R_{pd}$ | Input pull-down resistance | PU=low, PD=high | 40 | 75 | 150 | K$\Omega$ |
| $I_{in}$ | Input leakage current | $V_{in}$= $V_{DDH}$ or 0 | -10 | ±1 | 10 | $\mu$A |
| $I_{oz}$ | Tri-state output leakage current | | -10 | ±1 | 10 | $\mu$A |

## 5.5 USB Transceiver Characteristics

### Table 5.5 Electrical characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VD33 | Analog supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| VDDU VDDA | Digital supply Voltage | | 1.62 | 1.8 | 1.98 | V |
| $I_{CC}$ | Operating supply current | High speed operating at 480 MHz | | | 55 | mA |
| $I_{CC\ (susp)}$ | Suspend supply current | In suspend mode, current with 1.5k$\Omega$ pull-up resistor on pin RPU disconnected | | | 120 | µA |

### Table 5.6 Static characteristic：Digital pin

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|------------|------|------|------|------|
| | Input levels | | | | | |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | | 2.0 | | | V |
| | Output levels | | | | | |
| $V_{OL}$ | Low-level output voltage | | | | 0.2 | V |
| $V_{OH}$ | High-level output voltage | | VDDH-0.2 | | | V |

**VD33=3.0V~3.6V ； VDDU,VDDA=1.62V~1.98V ； Temp=0℃~70℃**

### Table 5.7 Static characteristic：Analog I/O pins（DP/DM）

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|------------|------|------|------|------|
| | USB2.0 Transceiver（HS） | | | | | |
| | Input Levels（differential receiver） | | | | | |
| $V_{HSDIFF}$ | High speed differential input sensitivity | ｜$V_{I（DP）}$-$V_{I（DM）}$｜ measured at the connection as application circuit | 300 | | | mV |
| $V_{HSCM}$ | High speed data signaling common mode voltage range | | -50 | | 500 | mV |
| $V_{HSSQ}$ | High speed squelch detection threshold | Squelch detected | | | 100 | mV |
| | | No squelch detected | 150 | | | mV |
| $V_{HSDSC}$ | High speed disconnection detection threshold | Disconnection detected | 625 | | | mV |
| | | Disconnection not detected | | | 525 | mV |
| | Output Levels | | | | | |
| $V_{HSOI}$ | High speed idle level output voltage(differential) | | -10 | | 10 | mV |
| $V_{HSOL}$ | High speed low level output voltage(differential) | | -10 | | 10 | mV |
| $V_{HSOH}$ | High speed high level output voltage(differential) | | -360 | | 400 | mV |
| $V_{CHIRPJ}$ | Chirp-J output voltage（differential） | | 700 | | 1100 | mV |
| $V_{CHIRPK}$ | Chirp-K output voltage（differential） | | -900 | | -500 | mV |
| | Resistance | | | | | |
| $R_{DRV}$ | Driver output impedance | Equivalent resistance used as internal chip only | 3 | 6 | 9 | Ω |

| | | Overall resistance including external resistor | 40.5 | 45 | 49.5 | |
|---|---|---|---|---|---|---|
| | | Termination | | | | |
| $V_{TERM}$ | Termination voltage for pull-up resistor on pin RPU | | 3.0 | | 3.6 | V |
| | | USB1.1 Transceiver（FS/LS） | | | | |
| | | Input Levels（differential receiver） | | | | |
| $V_{DI}$ | Differential input sensitivity | ｜$V_{I（DP）}$-$V_{I（DM）}$｜ | 0.2 | | | V |
| $V_{CM}$ | Differential common mode voltage | | 0.8 | | 2.5 | V |
| | | Input Levels（single-ended receivers） | | | | |
| $V_{SE}$ | Single ended receiver threshold | | 0.8 | | 2.0 | V |
| | | Output levels | | | | |
| $V_{OL}$ | Low-level output voltage | | 0 | | 0.3 | V |
| $V_{OH}$ | High-level output voltage | | 2.8 | | 3.6 | V |

**VD33=3.0V~3.6V；VDDU,VDDA=1.62V~1.98V；Temp=0℃~70℃**

### Table 5.8 Dynamic characteristic：Analog I/O pins（DP/DM）

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | | Driver Characteristics | | | | |
| | | High-Speed Mode | | | | |
| $t_{HSR}$ | High-speed differential rise time | | 500 | | | ps |
| $t_{HSF}$ | High-speed differential fall time | | 500 | | | ps |
| | | Full-Speed Mode | | | | |
| $t_{FR}$ | Rise time | CL=50pF；10 to 90% of｜$V_{OH}$-$V_{OL}$｜； | 4 | | 20 | ns |
| $t_{FF}$ | Fall time | CL=50pF；90 to 10% of｜$V_{OH}$-$V_{OL}$｜； | 4 | | 20 | ns |
| $t_{FRMA}$ | Differential rise/fall time matching（$t_{FR}$ / $t_{FF}$） | Excluding the first transition from idle mode | 90 | | 110 | ％ |
| $V_{CRS}$ | Output signal crossover voltage | Excluding the first transition from idle mode | 1.3 | | 2.0 | V |
| | | Low-Speed Mode | | | | |
| $t_{LR}$ | Rise time | CL=200pF-600pF；10 to 90% of｜$V_{OH}$-$V_{OL}$｜； | 75 | | 300 | ns |

| $t_{LF}$ | Fall time | CL=200pF-600pF; 90 to 10% of ｜$V_{OH}$-$V_{OL}$｜; | 75 | | 300 | ns |
|---|---|---|---|---|---|---|
| $t_{LRMA}$ | Differential rise/fall time matching（$t_{LR}$ / $t_{LF}$） | Excluding the first transition from idle mode | 80 | | 125 | ％ |
| $V_{CRS}$ | Output signal crossover voltage | Excluding the first transition from idle mode | 1.3 | | 2.0 | V |
| $V_{OH}$ | High-level output voltage | | 2.8 | | 3.6 | V |

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# 6. Mechanical Information

**Figure 6.1 Mechanical Information Diagram**



NOTES:

1. JEDEC OUTLINE MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS | MIN. | MAX. |
|---------|------|------|
| A | — | 1.6 |
| A1 | 0.05 | 0.15 |
| A2 | 1.35 | 1.45 |
| c1 | 0.09 | 0.16 |
| D | 9.00 BSC | |
| D1 | 7.00 BSC | |
| E | 9.00 BSC | |
| E1 | 7.00 BSC | |
| e | 0.5 BSC | |
| b | 0.17 | 0.27 |
| L | 0.45 | 0.75 |
| L1 | 1 REF | |

# 7. Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

| | |
|---|---|
| **DC Electrical** | Direct Current Electrical |
| **PLL** | Phase Lock Loop, which is a closed-loop frequency control system. |
| **ECC** | Error Checking and Correcting |
| **XTAL** | Crystal |
| **UFD** | USB Flash Disk |
| **iStar** | Partition/Password Operation Tool - the smart application program developed by Alcor Micro as a companion handy tool for managing the UFD. |

# About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.