# TOSHIBA

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

## TC74LCX05F,TC74LCX05FN,TC74LCX05FT,TC74LCX05FK

Low-Voltage HEX Inverter with 5-V Tolerant Inputs and Outputs (open-drain)

The TC74LCX05 is a high-performance CMOS inverter. Designed for use in 3.3-V systems, it achieves high-speed

operation while maintaining the CMOS low power dissipation. Pin configuration and function are the same as the

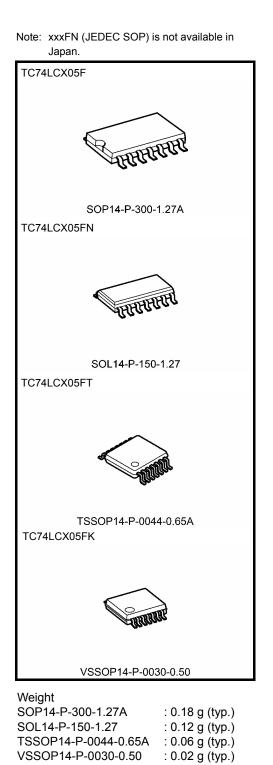
TC74LCX04, but the TC74LCX05F/FN/FT has high performance MOS N-channel transistor. (open-drain outputs)

The device is designed for low-voltage (3.3 V) VCC applications, but it could be used to interface to 5-V supply environment for inputs.

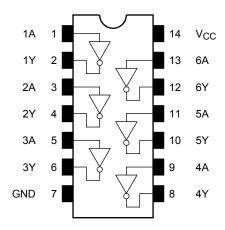
All inputs are equipped with protection circuits against static discharge.

## Features

- Low-voltage operation: V<sub>CC</sub> = 2.0 to 3.6 V
- High-speed operation:  $t_{pz} = 5.0 \text{ ns} (\text{max}) (V_{CC} = 3.0 \text{ to } 3.6 \text{ V})$
- Output current:  $I_{OL} = 24 \text{ mA} (min) (V_{CC} = 3.0 \text{ V})$
- Latch-up performance: -500 mA
- Available in JEDEC SOP, JEITA SOP, TSSOP and VSSOP (US)
- Open-drain outputs
- Power-down protection is provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 05 type



#### Pin Assignment (top view)



#### **Truth Table**

Inputs	Outputs
A	Y
L	Z
Н	L

Z: High impedance

## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit	
Power supply voltage	V <sub>CC</sub>	–0.5 to 7.0	V	
DC input voltage	V <sub>IN</sub>	-0.5 to 7.0	V	
		-0.5 to 7.0 (Note 2)		
DC output voltage	Vout	-0.5 to V <sub>CC</sub> + 0.5 (Note 3)	V	
Input diode current	I <sub>IK</sub>	-50	mA	
Output diode current	IOK	–50 (Note 4)	mA	
DC output current	IOUT	50	mA	
Power dissipation	PD	180	mW	
DC V <sub>CC</sub> /ground current	I <sub>CC</sub> /I <sub>GND</sub>	±100	mA	
Storage temperature	T <sub>stg</sub>	–65 to 150	°C	

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

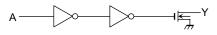
- Note 2: Output in OFF state
- Note 3: Low state.  $I_{\mbox{OUT}}$  absolute maximum rating must be observed.

Note 4:  $V_{OUT} < GND$ 

## **IEC Logic Symbol**

1A -	1 3	1 🖉		2	- 1Y - 2Y
2A -	5			6	- 3Y
3A -	9		/	8	- 3Y - 4Y
4A -	11			10	- 5Y
5A - 6 <b>A</b> -	13			12	- 6Y
07					01

#### System Diagram (per gate)



## **Operating Ranges (Note 1)**

Characteristics	Symbol	Rating	Unit	
Power supply voltage	V <sub>CC</sub>	2.0 to 3.6	V	
Power supply voltage	VCC	1.5 to 3.6 (Note 2)	v	
Input voltage	V <sub>IN</sub>	0 to 5.5	V	
Output valtage	V <sub>OUT</sub>	0 to 5.5 (Note 3)	V	
Output voltage		0 to $V_{CC}$ (Note 4)	v	
Output current	le.	24 (Note 5)	mA	
Output current	I <sub>OL</sub>	12 (Note 6)	ША	
Operating temperature	T <sub>opr</sub>	-40 to 85	°C	
Input rise and fall time	dt/dv	0 to 10 (Note 7)	ns/V	

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

- Note 2: Data retention only
- Note 3: Output in OFF state
- Note 4: Low state
- Note 5:  $V_{CC} = 3.0$  to 3.6 V
- Note 6:  $V_{CC} = 2.7$  to 3.0 V
- Note 7:  $V_{IN}=0.8$  to 2.0 V,  $V_{CC}=3.0$  V

#### **Electrical Characteristics**

#### DC Characteristics (Ta = -40 to $85^{\circ}C$ )

Character	istics	Symbol	٢	Test Condition		Min	Max	Unit
	H-level	V <sub>IH</sub>		—		2.0	_	V
Input voltage	L-level	VIL		_	2.7 to 3.6		0.8	v
				I <sub>OL</sub> = 100 μA	2.7 to 3.6		0.2	- V
Output voltage		Mai		I <sub>OL</sub> = 12 mA	2.7	_	0.4	
Oulput voltage	Output voltage L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub>	I <sub>OL</sub> = 16 mA	3.0	_	0.4	
				I <sub>OL</sub> = 24 mA	3.0	_	0.55	
Input leakage curre	ent	l <sub>IN</sub>	$V_{IN} = 0$ to 5.5 V	/ <sub>IN</sub> = 0 to 5.5 V		_	±5.0	μA
Output OFF state of	current	I <sub>OZ</sub>	$V_{IN} = V_{IL}, V_{OUT} =$	= 0 to 5.5 V	2.7 to 3.6	_	±5.0	μA
Power-off leakage	current	I <sub>OFF</sub>	$V_{IN}/V_{OUT} = 5.5 V$		0	_	10.0	μA
Quiescent supply current	laa	$V_{IN} = V_{CC}$ or GND		2.7 to 3.6	_	10.0		
	Icc	$V_{IN}/V_{OUT} = 3.6 \text{ to } 5.5 \text{ V}$		2.7 to 3.6		±10.0	μA	
Increase in Icc per	input	Δlcc	$V_{IH} = V_{CC} - 0.6 V$	1	2.7 to 3.6		500	

#### AC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition		Min	Max	Unit
	2		$V_{CC}(V)$			
Output enable time	t	Figure 1 Figure 2	2.7	1.0	6.0	- ns
	t <sub>pZL</sub>	Figure 1, Figure 2	$\textbf{3.3}\pm\textbf{0.3}$	0.8	5.0	
Output dischle time	t <sub>pLZ</sub>	Figure 1, Figure 2	2.7	1.0	6.0	20
Output disable time			$\textbf{3.3}\pm\textbf{0.3}$	0.8	5.0	ns
Output to output skew	+	(Neto)	2.7	_		
	t <sub>osZL</sub>	(Note)	$\textbf{3.3}\pm\textbf{0.3}$		1.0	ns

Note: Parameter guaranteed by design.  $(t_{osZL} = |t_{pZLm} - t_{pZLn}|)$ 

#### Dynamic Switching Characteristics (Ta = 25°C, input: $t_r = t_f = 2.5$ ns, $C_L = 50$ pF, $R_L = 500$ $\Omega$ )

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Quiet output maximum dynamic $V_{OL}$	V <sub>OLP</sub>	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	0.8	V
Quiet output minimum dynamic $V_{OL}$	V <sub>OLV</sub>	$V_{IH} = 3.3 \text{ V}, V_{IL} = 0 \text{ V}$	3.3	0.8	V

#### **Capacitive Characteristics (Ta = 25°C)**

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Тур.	Unit
Input capacitance	C <sub>IN</sub>		3.3	7	pF
Output capacitance	C <sub>OUT</sub>		3.3	8	pF
Power dissipation capacitance	C <sub>PD</sub>	f <sub>IN</sub> = 10 MHz (Note	) 3.3	5	pF

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 $I_{CC}$  (opr) =  $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$  (per gate)

## **AC Test Circuit**

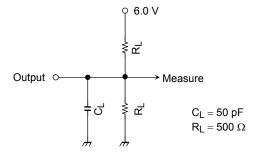


Figure 1

## AC Waveform

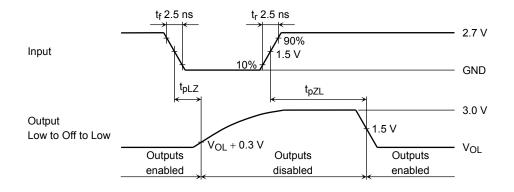


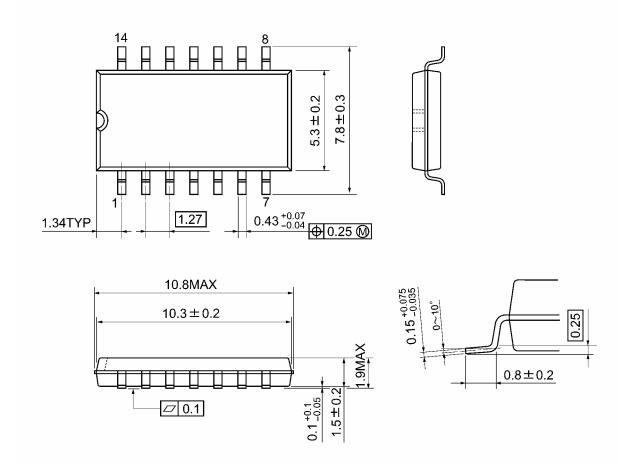
Figure 2 t<sub>pLZ</sub>, t<sub>pZL</sub>



## **Package Dimensions**

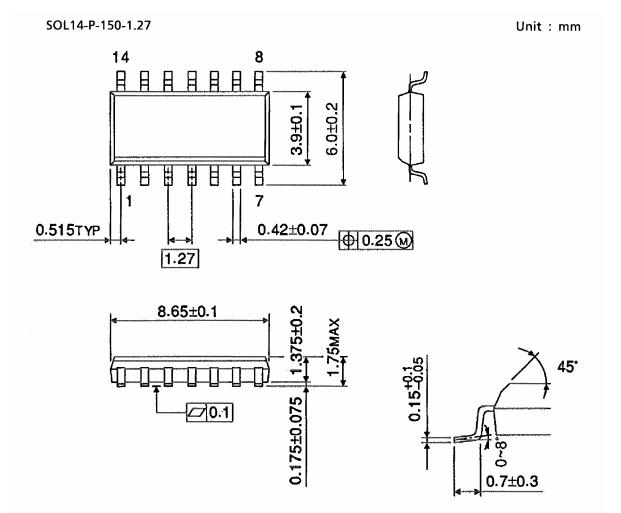
SOP14-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

## Package Dimensions (Note)



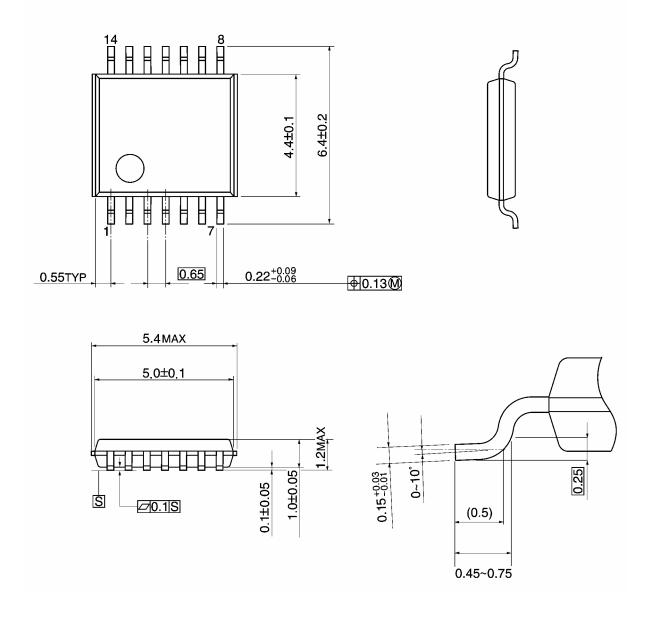
Note: This package is not available in japan.

Weight: 0.12 g (typ.)

## Package Dimensions

TSSOP14-P-0044-0.65A

Unit: mm



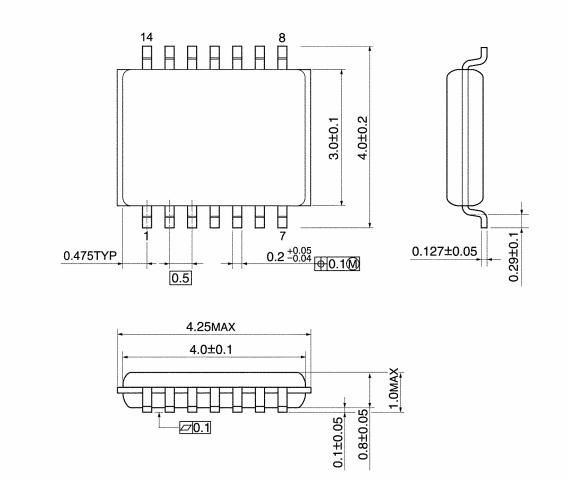
Weight: 0.06 g (typ.)

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## **Package Dimensions**

VSSOP14-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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20070701-EN GENERAL

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