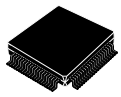
TDA7546

Multichip module for TMC tuner applications

Features

- High-performance FM receiver
- SW-Controlled world tuning
- Variable bandwidth IF filter (ISS, intelligent selectivity system)
- Programmable quality detectors
- High-speed PLL for RDS operation
- Full electronic alignment
- High-performance fully digital RDS/RBDS demodulator
- Integrated group and block synchronization
- Error detection and correction
- Full I^2C-Bus control



LQFP80

The following two devices are included

- **TDA7512F,** high performance car-radio FM tuner with high-speed on-chip PLL and variable-bandwidth IF filter (ISS)
- **TDA7333N**, fully digital RDS data decoder with with on-chip group and block synchronization and error detection/correction.

Both chips are I^2C-bus controlled.

Description

The TDA7546 multichip module combines in a single compact (14X14mm) 80-pin package the functionalities of a state-of-the-art FM receiver and RDS processor, exploiting one single 10.25MHz crystal reference.

Order codes

Part number	Package	Packing
TDA7546	LQFP80	Tray
TDA7546TR	LQFP80	in Tape & Reel

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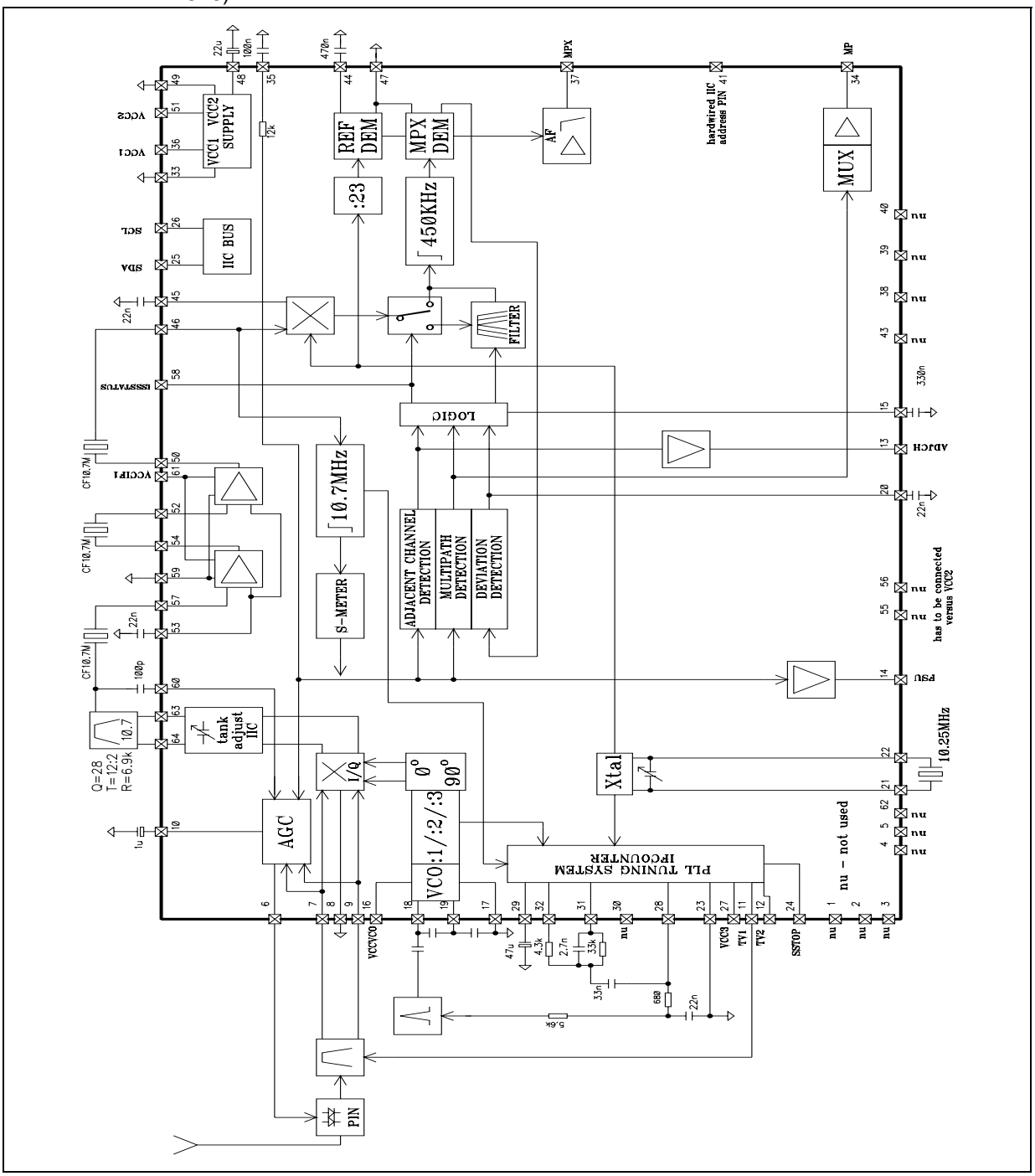
1 Block diagrams

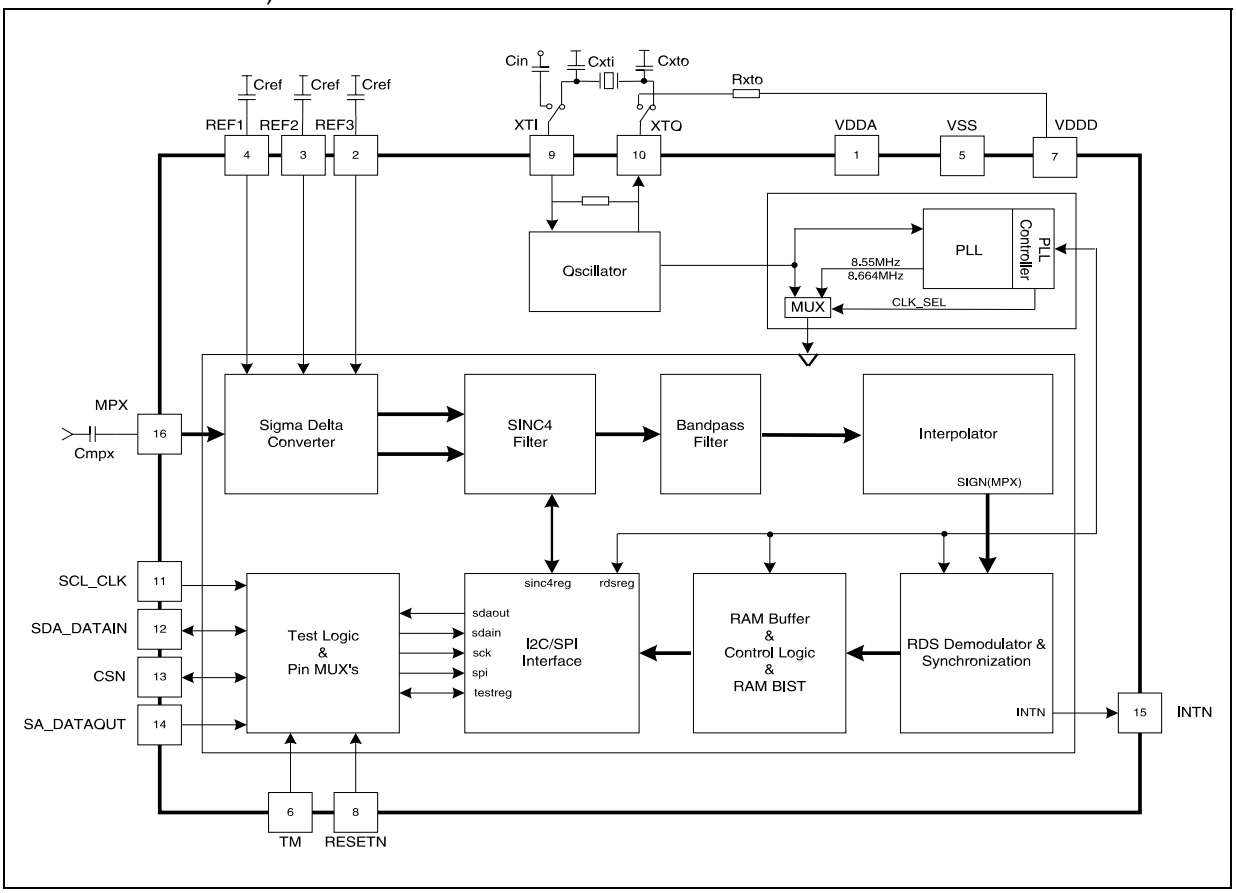
1.1 TDA7512F

Figure 1. Tuner block diagram
(Pin numbers are referred to the stand-alone device. Refer to *Table 1* for correspondance to TDA7546).



1.2 TDA7333N

Figure 2. RDS decoder block diagram
(Pin numbers are referred to the stand-alone device. Refer to *Table 1* for correspondance to TDA7546).



2 Pin description

Table 1. Pin configuration

TDA7546	FM Tuner	RDS Decoder	Name	Function
	TDA7512F	TDA7333N		
1				Not Connected
2	6		PINDR	PIN Diode Driver Output
3	7		MIX1IN1	Input1 Mixer1
4	8		GNDRF	RF Ground
5	9		MIX1IN2	Input2 Mixer1
6	10		AGCTC	AGC Time Constant
7	11		TV1	Tuning Voltage Preselection 1
8	12		TV2	Tuning Voltage Preselection 2
9	13		ADJCH	Adjacent Channel Detector Output
10	14		FSU	Unweighted Field Strength Output
11	15		ISSTC	Time Constant for ISS Ffilter Switch
12				Not Connected
13				Not Connected
14	16		VCCVCO	VCO Supply
15	17		GNDVCO	VCO Ground
16	18		VCOB	VCO Input (base)
17	19		VCOE	VCO Output (emitter)
18	20		DEVTC	Deviation Detector Time Constant
19	21		XTALG	Crystal Oscillator Input (gate)
20	22		XTALD	Crystal Oscillator Output (drain)
21	23		GNDVCC3	VCC3 Ground
22	24		SSTOP	Search Stop Output
23	25		SDA	I^2C Data
24	26		SCL	I^2C Clock
25	27		VCC3	Tuning Section Supply
26	28		LPOUT	PLL Loop Filter Output
27	29		VREF2	PLL Loop Filter Reference
28	31		LPF	PLL Loop Filter Input
29				Not Connected
30				Not Connected
31				Not Connected

Table 1. Pin configuration (continued)

TDA7546	FM Tuner	RDS Decoder	Name	Function
	TDA7512F	TDA7333N		
32		8	RESETN	Reset
33		9	XTI	Oscillator Input
34				Not Connected
35		10	XTO	Oscillator Output
36		11	SCL_CLK	I^2C/SPI Clock
37		12	SDA_DATAIN	I^2C Data/SPI Data Input
38		13	SA_DATAOUT	I^2C Slave Address/SPI Data Output
39		14	CSN	SPI Chip Select
40		15	INTN	Interrupt Output
41		16	MPX	Multiplex Input
42				Not Connected
43				Not Connected
44		1	VDDA	Analog Supply
45				Not Connected
46				Not Connected
47		2	REF3	2.65V Reference
48		3	REF2	1.65V Reference
49		4	REF1	0.65V Reference
50		5	VSS	Ground
51		6	TM	Test Mode
52		7	VDDD	Digital Supply
53	32		LPHC	PLL Loop Filter High Current Input
54	33		GNDVCC1	Digital Ground
55	34		MP	Multipath Detector Output
56	35		FSW	Weighted Field Strength Output
57	36		VCC1	Digital Supply
58	37		MPX	Multiplex Output
59				Not Connected
60				Not Connected
61	44		REFDEMC	Demodulator Reference
62	45		MIX2IN2	Mixer2 Input 2
63	46		MIX2IN1	Mixer2 Input 1
64	47		GNDDEM	Demodulator Ground

Table 1. Pin configuration (continued)

TDA7546	FM Tuner	RDS Decoder	Name	Function
	TDA7512F	TDA7333N		
65	48		VREF1	5V Reference
66	49		GNDVCC2	Analog Ground
67				Not Connected
68	50		IF1AMP2OUT	IF1 Amplifier 2 Output
69	51		VCC2	Analog Supply
70	52		IF1AMP2IN	IF1 Amplifier 2 Input
71	53		IF1REF	IF1 Amplifier Reference
72	54		IF1AMP1OUT	IF1 Amplifier 1 Output
73	55-56		VCC	Supply
74	57		IF1AMP1IN	IF1 Amplifier 1 Input
75	58		ISS	ISS Filter Status
76	59		GNDIF1	FM IF1 Ground
77	60		IFAGCIN	IF AGC Input
78	61		VCCIF1	IF1 Supply
79	63		MIX1OUT2	Mixer1 Ouput 2
80	64		MIX1OUT1	Mixer1 Ouput 1

Note: All NC pins can be connected to Ground.

2.1 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Units
$R_{Th\ j\text{-}amb}$	Thermal Resistance junction to ambient – IC soldered on multilayer PCB	53	°C/W

3 Electrical specification

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter		Value	Units
V_{CC}	Supply Voltage (Tuner)		10.5	V
V_{DD}	Supply Voltage (RDS)		4	V
T_{amb}	Ambient Operating Temperature		-40 to 85	°C
T_{stg}	Storage Temperature		-55 to 150	°C
V_{ESD}	ESD Withstand Voltage	Human Body Model	≥ ±2000	V
		Machine Model	≥ ±200	V
		Charged Device Model, all pins	≥ ±250	V
		Charged Device Model, all pins except #3 and #5	≥ ±500	V
		Charged Device Model, corner pins	≥ ±750	V

3.2 Electrical characteristics

Table 4. General parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Units
F_{RF}	RF input frequency		76		108	MHz
AS	Audio Sensitivity	f_c = 98.1MHz, ; f_{dev} = 22.5KHz; f_{mod} = 1KHz; dummy antenna; SNR = 26dB; CCIR filter; external pre-emphasis = 50ms			17	dBµV
RS	RDS Sensitivity	f_c = 98.1MHz, ; f_{dev} = 2KHz; no audio modulation; dummy antenna; Block Error Rate = 50%			23	dBµV
S/N_{max}	Maximum Audio (S+N)/N	f_c = 98.1MHz, ; f_{dev} = 22.5KHz; f_{mod} = 1KHz; dummy antenna; mono signal; CCIR filter; external pre-emphasis = 50µs	55	60		dB

3.3 Tuner

Table 5. Tuner

(T_{amb} = -40 to +85°C, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1} = V_{CCIF1}$=8.5V, f_{RF} = 98.1MHz, dev. = 40KHz, f_{MOD} = 1KHz, f_{IF1} = 10.7MHz, f_{IF2} = 450KHz, f_{Xtal} = 10.25MHz, in application circuit, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply						
V_{CC1}	Digital supply voltage		7.7	8.5	10	V
V_{CC2}	Analog supply voltage		7.7	8.5	10	V
V_{CC3}	Tuning section voltage		7.7	8.5	10	V
V_{CCVCO}	VCO supply voltage		7.7	8.5	10	V
V_{CCMIX1}	MIX1 supply voltage		7.7	8.5	10	V
V_{CCIF1}	IF1 supply voltage		7.7	8.5	10	V
I_{CC1}	Supply current			7.5	10	mA
I_{CC2}	Supply current			60	70	mA
I_{CC3}	Supply current			2	3	mA
I_{CCVCO}	Supply current			9.5	12	mA
I_{CCMIX1}	Supply current			8	10.5	mA
I_{CCIF1}	Supply current			6	7.5	mA
Reference Voltages						
V_{REF1}	Internal reference voltage	I_{REF1} = 0mA	4.8	5	5.2	V
V_{REF2}	Internal reference voltage	I_{REF2} = 0mA	2.3	2.5	2.7	V
Wide Band RF AGC						
V_{3-5}	Lower threshold start	V_6 = 2.5V	78	82	86	dBµV
	Upper threshold start	V_6 = 2.5V	90	94	98	dBµV
Narrow Band IF & Keying AGC						
V_{77}	Lower threshold start	KAGC = off, V_{3-5} = 0mV_{RMS}	82	86	90	dBµV
	Upper threshold start	KAGC = off, V_{3-5} = 0mV_{RMS}	94	98	102	dBµV
	Lower threshold start with KAGC	KAGC = max, V_{3-5} = 0mV_{RMS}, Δf_{IF}=300KHz	94	98	102	dBµV
V_{56}	Startpoint KAGC	KAGC = max, V_{3-5} = 0mV_{RMS}, Δf_{IF}=300KHz f_{IF1} generate FSW level at V_{56}		3.6		V
Δ	Control range KAGC	ΔV_{56} = +0.4V		16		dB
R_{IN}	Input resistance		10	13	16	kΩ

Table 5. Tuner (continued)
(T_{amb} = -40 to +85°C, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1} = V_{CCIF1}$=8.5V, f_{RF} = 98.1MHz, dev. = 40KHz, f_{MOD} = 1KHz, f_{IF1} = 10.7MHz, f_{IF2} = 450KHz, f_{Xtal} = 10.25MHz, in application circuit, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AGC Time Constant Output						
V_6	Max. AGC output voltage	V_{3-5} = 0mV$_{RMS}$			V_{REF1} +V_{BE}	V
	Min. AGC output voltage	V_{3-5} = 50mV$_{RMS}$			0.5	V
I_6	Min. AGC charge current	V_{3-5} = 0mV$_{RMS}$,V_{10} = 2.5V	-16.5	-12.5	-8.5	µA
	Max. AGC discharge current	V_{3-5} = 50mV$_{RMS}$,V_{10} = 2.5V	0.9	1.25	1.6	mA
AGC PIN Diode Driver Output						
I_2	AGC OUT, current min.	V_{3-5} = 0mV$_{RMS}$, V_2 = 2.5V	9	12	15	µA
	AGC OUT, current max.	V_{3-5} = 50 mV$_{RMS}$, V_2 = 2.5V	-22	-17	-13	mA
I/Q Mixer1 (10.7MHz)						
R_{IN}	Input resistance	differential		10		kΩ
R_{OUT}	Output resistance	differential	100			kΩ
V_{3-5}	Input dc bias		2.4	2.65	2.9	V
g_m	Conversion transconductance			17		ms
F	Noise figure	400Ω generator resistance (1)		3		dB
CP_{1dB}	1dB compression point	referred to diff. mixer input		100		dBµV
IIP3	3rd order intermodulation	(1)		122		dBµV
IQG	I/Q gain adjust	G	-1		+1	%
IQP	I/Q phase adjust	PH	-7		+8	°
IRR	Image rejection ratio	with gain and phase adjust	40			dB
IF1 Amplifier1,2 (10.7MHz)						
$G1_{min}$	Min. gain	IFG, referred to 330Ω	7.5	9	10.5	dB
$G1_{max}$	Max. gain	IFG, referred to 330Ω	13.5	15	16.5	dB
$G2_{min}$	Min. gain	IFG, referred to 330Ω	7.5	9	10.5	dB
$G2_{max}$	Max. gain	IFG, referred to 330Ω	9.5	11	13.5	dB
R_{IN}	Input resistance		250	330	400	Ω
R_{OUT}	Output resistance		250	330	400	Ω
CP_{1dB}	1dB compression point	referred to 330Ω input (1)		105		dBµV
IIP3	3rd order Intermodulation	referred to 330Ω input (1)		126		dBµV
Demodulator, Audio Output						
THD	Total Harmonic Distortion	dev. = 75kHz, V = Mix2 = 10 mVrms			0.1	%

Table 5. Tuner (continued)
(T_{amb} = -40 to +85°C, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1} = V_{CCIF1}$=8.5V, f_{RF} = 98.1MHz, dev. = 40KHz, f_{MOD} = 1KHz, f_{IF1} = 10.7MHz, f_{IF2} = 450KHz, f_{Xtal} = 10.25MHz, in application circuit, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	dev. = 75kHz	400	500	600	mVrms
R_{OUT}	Output resistance		15	40	65	Ω
$\|\Delta V\|_{min}$	DC offset fine adjust	DEM, MENA=1		8.5		mV
$\|\Delta V\|_{max}$	DC offset fine adjust	DEM, MENA=1		264		mV
QUALITY DETECTION						
S-meter, Unweighted Fieldstrength						
V_{14}	Fieldstrength output	$V_{46} = 0V_{RMS}$		0.1		V
	Fieldstrength output	$V_{46} = 1V_{RMS}$		4.9		V
ΔV_{14}	voltage per decade	SMSL = 0	0.75	1	1.25	V
	voltage per decade	SMSL = 1	1.1	1.5	1.9	V
	S-meter offset	SL, SMSL=1	-15		15	dB
R_{OUT}	Output resistance		300	450	650	Ω
S-meter, Weighted Fieldstrength						
V_{35}	Fieldstrength output	$V_{46} = 0V_{RMS}$		2.5		V
	Fieldstrength output	$V_{46} = 1V_{RMS}$		4.9		V
R_{OUT}	Output resistance		12	13.5	15	kΩ
Adjacent Channel Output						
V_{13}	Output voltage low			0.1	0.2	V
	Output voltage high		4.4	4.9		V
R_{OUT}	Output resistance		3.5	4.5	5.5	kΩ
Multipath Output						
V_{34}	Output voltage low			0.1	0.2	V
	Output voltage high		4.4	4.9		V
R_{OUT}	Output resistance		2	3.5	5	kΩ
ISS (Intelligent Selectivity System)						
Filter 450KHz						
f_{centre}	Centre frequency	f_{REF_intern} = 450KHz		450		KHz
BW 3dB	Bandwidth, -3dB	ISS80 = 1	70	80	80	KHz
BW 20dB	Bandwidth, -20dB	ISS80 = 1	135	150	165	KHz
BW 3dB	Bandwidth, -3dB	ISS80 = 0	105	120	135	KHz
BW 20dB	Bandwidth, -20dB	ISS80 = 0	220	250	280	KHz

Table 5. Tuner (continued)
(T_{amb} = -40 to +85°C, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1} = V_{CCIF1}$=8.5V, f_{RF} = 98.1MHz, dev. = 40KHz, f_{MOD} = 1KHz, f_{IF1} = 10.7MHz, f_{IF2} = 450KHz, f_{Xtal} = 10.25MHz, in application circuit, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ISS Filter Time Constant						
I_{15}	Charge current low mid	TISS, ISSCTL = 1		-74		µA
	Charge current high mid	TISS, ISSCTL = 1	-80	-60	-40	µA
	Charge current low narrow	TISS, ISSCTL = 1		-124		µA
	Charge current high narrow	TISS, ISSCTL = 1	-140	-110	-80	µA
	Discharge current low	TISS, ISSCTL = 0	0.5	1	2	µA
	Discharge current high	TISS, ISSCTL = 0	10	15	20	µA
V_{15}	Low voltage	ISSCTL = 0		0.1	0.2	V
	High voltage	ISSCTL = 1	4.6	4.9		V

1. Guaranteed by design

3.3.1 Additional parameters

Table 6. Additional parameters

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Output of Tuning Voltages (TV1,TV2)						
V_{OUT}	Output voltage	TVO	0.5		V_{CC3}-0.5	V
R_{OUT}	Output impedance		18	21.5	25	kΩ
Xtal Reference Oscillator						
f_{LO}	Reference frequency	C_{Load} = 15pF		10.25		MHz
C_{Step}	Min. cap step	XTAL		0.75		pF
C_{max}	Max. cap	XTAL		23.25		pF
Δf/f	Deviation versus VCC2	ΔV_{CC2} = 1V (1)		1.5		ppm/V
Δf/f	Deviation versus temp	-40°C < T < +85°C (1)		0.2		ppm/K
I^2C-Bus interface						
f_{SCL}	Clock frequency				400	KHz
V_{IL}	Input low voltage				1	V
V_{IH}	Input high voltage		2.5			V
I_{IN}	Input current		-5		5	µA
V_O	Output acknowledge voltage	I_O = 1.6mA			0.4	V
Loop Filter Input/Output						

Table 6. Additional parameters (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$-I_{IN}$	Input leakage current	V_{IN} = GND, PD_{OUT} = Tristate	-0.1		0.1	µA
I_{IN}	Input leakage current	V_{IN} = VREF1 PD_{OUT} = Tristate	-0.1		0.1	mA
V_{OL}	Output voltage Low	I_{OUT} = -0.2mA		0.05	0.5	V
V_{OH}	Output voltage High	I_{OUT} = 0.2mA	V_{CC3}-0.5	V_{CC3}-0.05		V
I_{OUT}	Output current, sink	V_{OUT} = 1V to V_{CC3}-1V			10	mA
	Output current, source	V_{OUT} = 1V to V_{CC3}-1V	-10			mA
Voltage Controlled Oscillator (VCO)						
f_{VCOmin}	Minimum VCO frequency (2)		50			MHz
f_{VCOmax}	Maximum VCO frequency (2)				260	MHz
C/N	Carrier to Noise	f_{VCO}= 200MHz, ∆f=1KHz, B=1Hz, closed loop		80		dBc
SSTOP Output (Open Collector)						
V_{24}	Output voltage low	I_{24} = -200µA		0.2	0.5	V
	Output voltage high				5	V
$-I_{24}$	Output leakage current	V_{24} = 5V	-0.1		0.1	µA
I_{24}	Output current, sink	V_{24} = 0.5V-5V			1	mA
ISSSTATUS Output (Open Drain)						
V_{58}	Output voltage low, ISS-Filter “ON”	I_{24} = -200µA		0.2	0.5	V
	Output voltage high, ISS-Filter “OFF”				5	V
$-I_{58}$	Output leakage current	V_{24} = 5V	-0.1		0.1	µA
I_{58}	Output current, sink	V_{24} = 0.5V-5V			300	µA

1. Guaranteed by design
2. Depending on external application circuit.

3.4 RDS decoder

3.4.1 General interface electrical characteristics

Table 7. General interface electrical characteristics

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{il}	Low Level Input Current	V_i =0V			1	µA
I_{ih}	High Level Input Current	V_i =V_{DD}			1	µA
I_{ozFT}	Five Volt tolerant Tri-State Output Leakage Without Pull Up/Down Device	V_o =0V or V_{DD}			1	µA
		V_o =5.5V		1	3	µA

3.4.2 Electrical characteristics

Table 8. Electrical characteristics
(T_{amb} = -40 to +85 °C, V_{DDA}/V_{DDD} = 3.0 to 3.6 V,f_{osc} = 10.25 MHz, unless otherwise specified V_{DDD} and V_{DDA} must not differ more than 0.15V).

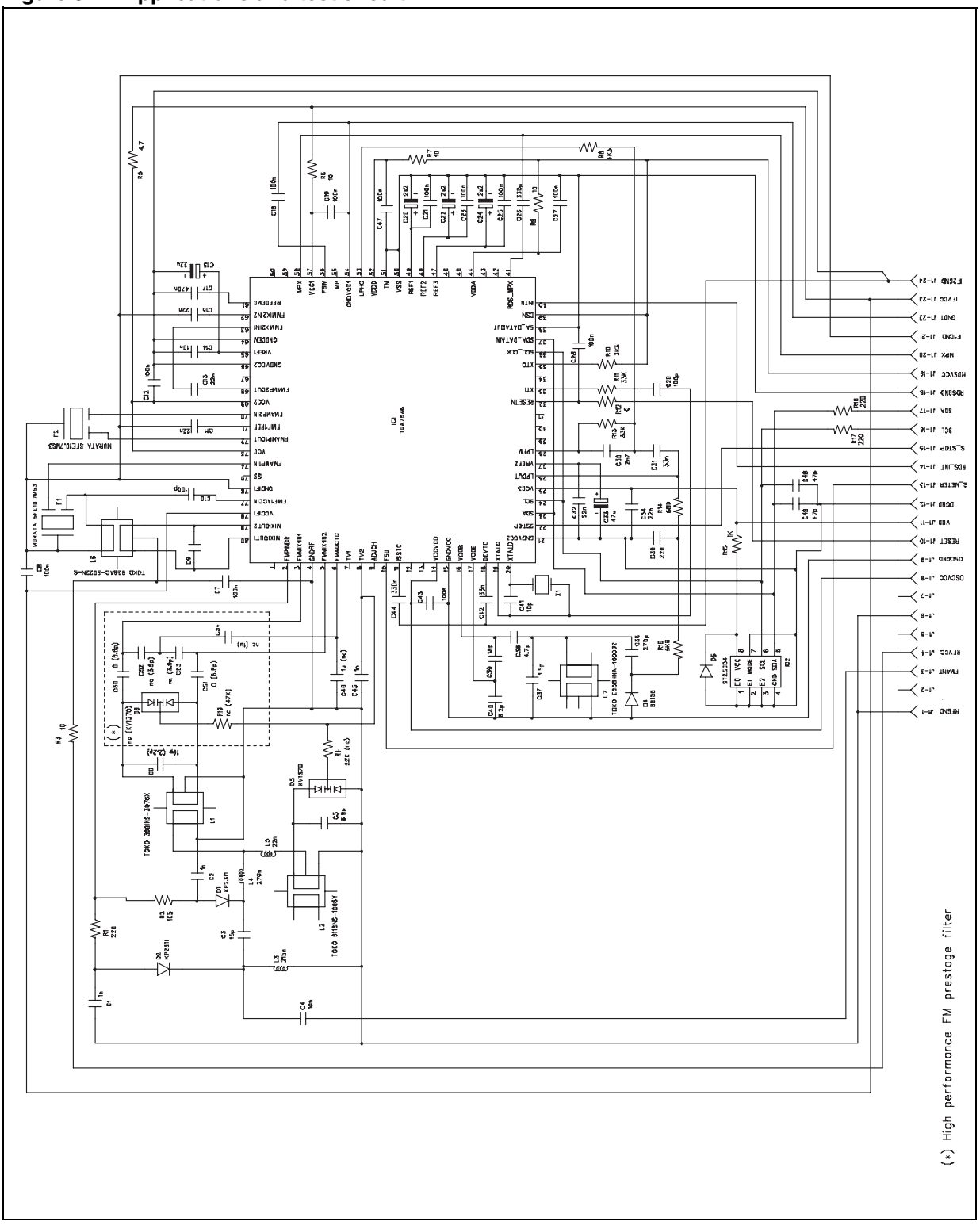
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply (pin 44, 50, 52)						
V_{DDD}	Digital Supply Voltage		3.0	3.3	3.6	V
V_{DDA}	Analog Supply Voltage		3.0	3.3	3.6	V
I_{DDD}	Digital Supply Current	Normal mode		14	16	mA
		Power down mode		<1		µA
I_{DDA}	Analog Supply Current	Normal mode		11	14	mA
		Power down mode		<1		mA
Digital Inputs (pin 51, 32, 36, 37, 38, 39)						
V_{il}	Low level input voltage				0.8	V
V_{ih}	High level input voltage		2.0			V
V_{ilhyst}	Low level threshold input falling		1.0		1.15	V
V_{ihhyst}	High level threshold input rising		1.5		1.7	V
V_{hst}	Schmitt trigger hysteresis		0.4		0.7	V
Digital Outputs (pin 37,38,40) are open drains						
V_{ol}	Low level output Voltage	I_{ol} =4mA, takes into account 200mV drop in the supply voltage			0.4	V

Table 8. Electrical characteristics (continued)
(T_{amb} = -40 to +85 °C, V_{DDA}/V_{DDD} = 3.0 to 3.6 V,f_{osc} = 10.25 MHz, unless otherwise specified V_{DDD} and V_{DDA} must not differ more than 0.15V).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Analog Inputs (pin 41)						
V_{MPX}	Input Range of MPX Signal				0.75	Vrms
	Input Impedance of MPX pin		45k	55k	65k	Ohm
V_{REF1}	Internal Reference Voltage		0.5		0.9	V
	Internal Reference Impedance		1.3		2	kΩ
V_{REF2}	Internal Reference Voltage		1.5		2.1	V
	Internal Reference Impedance		2.15		2.95	kΩ
V_{REF3}	Internal Reference Voltage		2.6		3.2	V
	Internal Reference Impedance		1.3		2.0	kΩ
PLL parameters						
f_{vco}	VCO Range		150		250	MHz
f_{vin}	VCO Input Range		4		21	MHz
t_{lock}	PLL Lock Time				500	µs
I_{DF}	Input Divide Factor		1		32	
O_{DF}	Output Divide Factor		2		32	
M_F	Integer Multiplication Factor		9		128	
FRA	Fractional Multiplication Factor	$FRA/2^{14}$	0	-	2^{14}	
I^2C (@ fsys = 8.55/8.664MHz)						
f_{I2C}	clock frequency in I^2C mode				400	KHz
SPI (@ fsys = 8.55/8.664MHz)						
f_{SPI}	clock frequency in SPI mode				1	MHz
t_{ch}	clock high time		450			ns
t_{cl}	clock low time		450			ns
t_{csu}	chip select setup time		500			ns
t_{csh}	chip select hold		500			ns
t_{odv}	output data valid				250	ns
t_{oh}	output hold		0			ns
t_d	deselect time		1000			ns
t_{su}	data setup time		200			ns
t_h	data hold time		200			ns

4 Applications and test circuit

Figure 3. Applications and test circuit



5 Functional description

5.1 Tuner

5.1.1 Mixer1, AGC and 1.IF

The FM quadrature I/Q-mixer converts RF to IF1 of 10.7MHz. The mixer provides inherent image rejection and wide dynamic range with low noise and large input signal performance. The mixer1 tank can be adjusted by software (IF1T). For accurate image rejection the gain- and phase-error generated as well in mixer as VCO stage can be compensated by software (G,PH)

It is capable of tuning the US FM, US weather, Europe FM, Japan FM and East Europe FM bands

- US FM = 87.9 to 107.9 MHz
- US weather = 162.4 to 162.55 MHz
- Europe FM = 87.5 to 108 MHz
- Japan FM = 76 to 91 MHz
- East Europe FM = 65.8 to 74 MHz

The AGC operates on different sensitivities and bandwidths in order to improve the input sensitivity and dynamic range. AGC thresholds are programmable by software (RFAGC,IFAGC,KAGC). The output signal is a controlled current for double pin diode attenuator. Two 10.7MHz programmable amplifiers (IFG1, IFG2) correct the IF ceramic insertion loss and the costumer level plan application.

5.1.2 Mixer2, limiter and demodulator

In this 2. mixer stage the first 10.7MHz IF is converted into the second 450KHz IF. A multi-stage limiter generates signals for the complete integrated demodulator without external tank. MPX output DC offset versus noise DC level is correctable by software (DEM).

5.1.3 Quality detection and ISS

Fieldstrength

Parallel to mixer2 input a 10.7MHz limiter generates a signal for digital IF counter and a fieldstrength output signal. This internal unweighted fieldstrength is used for keying AGC, adjacent channel and multipath detection and is available at PIN14 (FSU) after +6dB buffer stage. The behaviour of this output signal can be corrected for DC offset (SL) and slope (SMSL). The internal generated unweighted fieldstrength is filtered at PIN35 and used for softmute function and generation of ISS filter switching signal for weak input level (sm).

Adjacent channel detector

The input of the adjacent channel detector is AC coupled from internal unweighted fieldstrength. A programmable highpass or bandpass (ACF) and amplifier (ACG) as well as rectifier determines the influences. This voltage is compared with adjustable comparator1 thresholds (ACWTH, ACNTH). The output signal of this comparator generates a DC level at PIN15 by programmable time constant. Time control (TISS) for a present adjacent channel is made by charge and discharge current after comparator1 in an external capacitance. The

charge current is fixed and the discharge current is controlled by I^2C Bus. This level produces digital signals (ac, ac+) in an additional comparator4. The adjacent channel information is available as analog output signal after rectifier and +8dB output buffer.

Multipath detector

The input of the multipath detector is AC coupled from internal unweighted fieldstrength. A programmable bandpass (MPF) and amplifier (MPG) as well as rectifier determines the influences. This voltage is compared with an adjustable comparator2 thresholds (MPTH). The output signal of this comparator2 is used for the "Milano" effect. In this case the adjacent channel detection is switched off. The "Milano" effect is selectable by I^2C Bus (MPOFF). The multipath information is available as analog output signal after rectifier and +8dB output buffer.

450KHz IF narrow bandpass filter (ISS filter)

The device gets an additional second IF narrow bandpass filter for suppression of noise and adjacent channel signal influences. This narrow filter has three switchable bandwidthes, narrow range of 80KHz, mid range of 120KHz and 30KHz for weather band information.

Without ISS filter the IF bandwidth (wide range) is defined only by ceramic filter chain. The filter is switched in after mixer2 before 450KHz limiter stage. The centre frequency is matching to the demodulator center frequency.

Deviation detector

In order to avoid distortion in audio output signal the narrow ISS filter is switched OFF for present overdeviation. Hence the demodulator output signal is detected.

A lowpass filtering and peak rectifier generates a signal that is defined by software controlled current (TDEV) in an external capacitance. This value is compared with a programmable comparator3 thresholds (DWTH, DTH) and generates two digital signals (dev, dev+). For weak signal condition deviation threshold is proportinal to FSU.

ISS switch logic

All digital signals coming from adjacent channel detector, deviation detector and softmute are acting via switching matrix on ISS filter switch. The IF bandpass switch mode is controlled by software (ISSON, ISS30, ISS80, CTLOFF).

The switch ON of the IF bandpass is also available by external manipulation of the voltage at PIN15.

Two application modes are available (APPM). The conditions are described in *Table 50*.

5.1.4 PLL and IF counter section

PLL frequency synthesizer block

This part contains a frequency synthesizer and a loop filter for the radio tuning system. Only one VCO is required to build a complete PLL system for FM world tuning . For auto search stop operation an IF counter system is available.

The counter works in a two stages configuration. The first stage is a swallow counter with a two modulus (32/33) precounter. The second stage is an 11-bit programmable counter.

The circuit receives the scaling factors for the programmable counters and the values of the reference frequencies via an I^2C-Bus interface.The reference frequency is generated by an adjustable internal (XTAL) oscillator followed by the reference divider. The main reference and step-frequencies are free selectable (RC, PC).

Output signals of the phase detector are switching the programmable current sources. The loop filter integrates their currents to a DC voltage.

The values of the current sources are programmable by 6 bits also received via the I^2C Bus (A, B, CURRH).

To minimize the noise induced by the digital part of the system, a special guard configuration is implemented. The loop gain can be set for different conditions by setting the current values of the chargepump generator.

Frequency generation for phase comparison

The RF signals applies a two modulus counter (32/33) pre-scaler, which is controlled by a 5-bit A-divider. The 5-bit register (PC0 to PC4) controls this divider. In parallel the output of the prescaler connects to an 11-bit B-divider. The 11-bit PC register (PC5 to PC15) controls this divider

Dividing range:

$f_{VCO} = [33 \times A + (B + 1 - A) \times 32] \times f_{REF}$

$f_{VCO} = (32 \times B + A + 32) \times f_{REF}$

Important: For correct operation: $A \leq 32$; $B \geq A$

Three state phase comparator

The phase comparator generates a phase error signal according to phase difference between f_{SYN} and f_{REF}. This phase error signal drives the charge pump current generator.

Charge pump current generator

This system generators signed pulses of current. The phase error signal decides the duration and polarity of those pulses. The current absolute values are programmable by A register for high current and B register for low current.

Inlock detector

Switching the chargepump in low current mode can be done either via software or automatically by the inlock detector, by setting bit LDENA to "1".

After reaching a phase difference about lower than 40nsec the chargepump is forced in low current mode. A new PLL divider alternation by I^2C-Bus will switch the chargepump in the high current mode.

Low noise CMOS op-amp

An internal voltage divider at pin VREF2 connects the positive input of the low noise op-amp. The charge pump output connects the negative input. This internal amplifier in cooperation with external components can provide an active filter.

While the high current mode is activated LPHC output is switched on.

IF counter block

The aim of IF counter is to measure the intermediate frequency of the tuner. The input signal is the 10.7MHz IF level after limiter.

The grade of integration is adjustable by eight different measuring cycle times. The tolerance of the accepted count value is adjustable, to reach an optimum compromise for search speed and precision of the evaluation.

Sampling timer

A sampling timer generates the gate signal for the main counter. The basically sampling time are in FM mode 6.25KHz (t_{TIM}=160µs).

This is followed by an asynchronous divider to generate several sampling times.

Intermediate frequency main counter

This counter is a 11 - 21-bit synchronous autoreload down counter. Five bits (CF) are programmable to have the possibility for an adjust to the centre frequency of the IF-filter. The counter length is automatic adjusted to the chosen sampling time.

At the start the counter will be loaded with a defined value which is an equivalent to the divider value (t_{Sample} x f_{IF}).

If a correct frequency is applied to the IF counter frequency input at the end of the sampling time the main counter is changing its state from 0h to 1FFFFFh.

This is detected by a control logic and an external search stop output is changing from LOW to HIGH. The frequency range inside which a successful count result is adjustable by the EW bits.

$$CNT = \frac{CF + 1696}{f_{IF}}$$

Counter result succeeded:
$t_{TIM} \geq t_{CNT} - t_{ERR}$
$t_{TIM} \leq t_{CNT} + t_{ERR}$
Counter result failed:
$t_{TIM} > t_{CNT} + t_{ERR}$
$t_{TIM} < t_{CNT} - t_{ERR}$

t_{TIM} = IF timer cycle time (sampling time)

t_{CNT} = IF counter cycle time

t_{ERR} = discrimination window (controlled by the EW registers)

The IF counter is only started by inlock information from the PLL part. It is enabled by software (IFENA).

Adjustment of the measurement sequence time

The precision of the measurements is adjustable by controlling the discrimination window. This is adjustable by programming the control registers EW.

The measurement time per cycle is adjustable by setting the registers IFS.

Adjust of the frequency value

The center frequency of the discrimination window is adjustable by the control registers CF.

5.1.5 I²C-bus interface

The TDA7512F supports the I²C-Bus protocol. This protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device that controls the transfer is a master and device being controlled is the slave. The master will always initiate data transfer and provide the clock to transmit or receive operations.

Data transition

Data transition on the SDA line must only occur when the clock SCL is LOW. SDA transitions while SCL is HIGH will be interpreted as START or STOP condition.

Start condition

A start condition is defined by a HIGH to LOW transition of the SDA line while SCL is at a stable HIGH level. This "START" condition must precede any command and initiate a data transfer onto the bus.

The device continuously monitors the SDA and SCL lines for a valid START and will not response to any command if this condition has not been met.

Stop condition

A STOP condition is defined by a LOW to HIGH transition of the SDA while the SCL line is at a stable HIGH level. This condition terminates the communication between the devices and forces the bus-interface of the device into the initial condition.

Acknowledge

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bits of data. During the 9th clock cycle the receiver will pull the SDA line to LOW level to indicate it receive the eight bits of data.

Data transfer

During data transfer the device samples the SDA line on the leading edge of the SCL clock. Therefore, for proper device operation the SDA line must be stable during the SCL LOW to HIGH transition.

Device addressing

To start the communication between two devices, the bus master must initiate a start instruction sequence, followed by an eight bit word corresponding to the address of the device it is addressing.

The most significant 6 bits of the slave address are the device type identifier.

The TDA7512F device type is fixed as "110001".

The next significant bit is used to address a particular device of the previous defined type connected to the bus.

The state of the hardwired PIN 41 defines the state of this address bit. So up to two devices could be connected on the same bus. When PIN 41 is connected to VCC2 the address bit “1” is selected. When PIN 41 is left open the address bit “0” is selected. Therefor a double FM tuner concept is possible.

The last bit of the start instruction defines the type of operation to be performed:

- When set to "1", a read operation is selected
- When set to "0", a write operation is selected

The TDA7512F connected to the bus will compare their own hardwired address with the slave address being transmitted, after detecting a START condition. After this comparison, the TDA7512F will generate an "acknowledge" on the SDA line and will do either a read or a write operation according to the state of R/W bit.

Write operation

Following a START condition the master sends a slave address word with the R/W bit set to "0". The device will generate an "acknowledge" after this first transmission and will wait for a second word (the word address field). This 8-bit address field provides an access to any of the 32 internal addresses.

Upon receipt of the word address the TDA7512F slave device will respond with an "acknowledge". At this time, all the following words transmitted to the TDA7512F will be considered as Data.

The internal address will be automatically incremented. After each word receipt the TDA7512F will answer with an "acknowledge".

Read operation

If the master sends a slave address word with the R/W bit set to "1", the TDA7512F will transit one 8-bit data word. This data word includes the following informations:

bit0 (ISS filter, 1 = ON, 0 = OFF)

bit1 (ISS filter bandwidth, 1 = 80KHz, 0 = 120KHz)

bit2 (MPOUT,1 = multipath present, 0 = no multipath)

bit3 (1 = PLL is locked in , 0 = PLL is locked out).

bit4 (fieldstrength indicator, 1 = lower as softmute threshold, 0 = higher as softmute threshold)

bit5 (adjacent channel indicator, 1 = adjacent channel present, 0 = no adjacent channel)

bit6 (deviation indicator, 1 = strong overdeviation present, 0 = no strong overdeviation)

bit7 (deviation indicator, 1 = overdeviation present, 0 = no overdeviation)

5.2 RDS decoder

5.2.1 Overview

The new RDS/RBDS processor contains all RDS/RBDS relevant functions on a single chip. It recovers the inaudible RDS/RBDS information which are transmitted on most FM radio broadcasting stations.

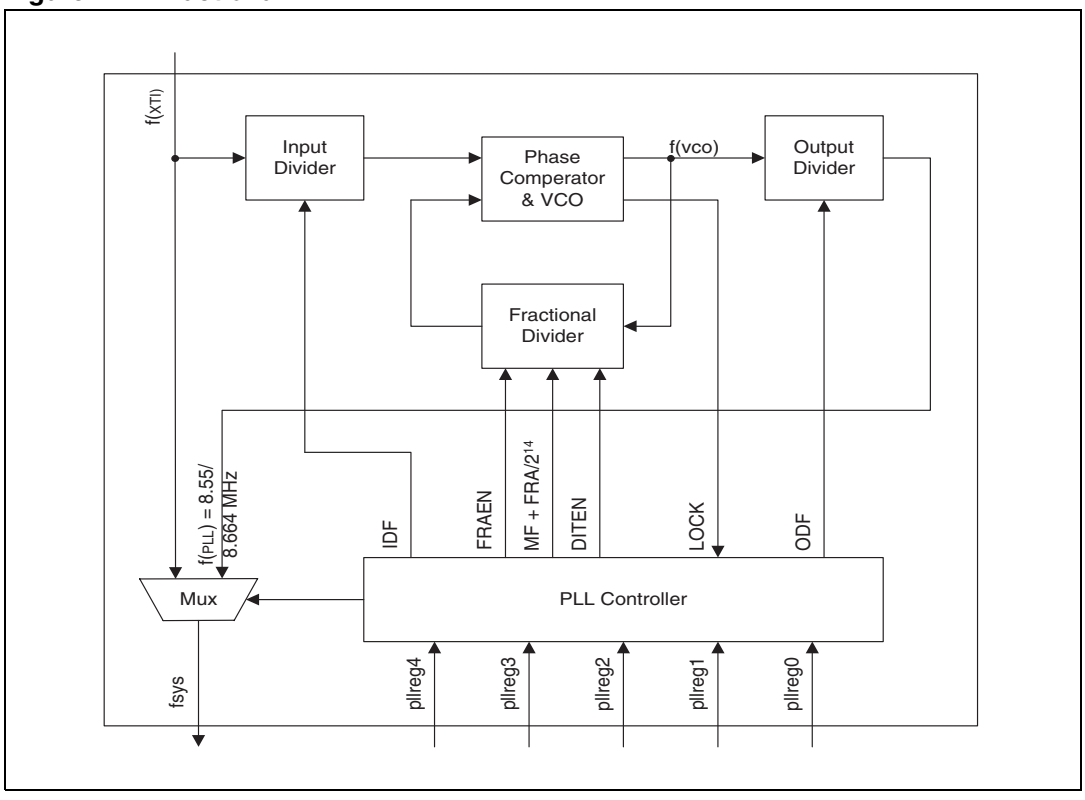
The oscillator frequency is 10.25MHz and is derived from the tuner. The fractional PLL must be initialized through I^2C/SPI interface to generate the internal 8.55 MHz or 8.664 MHz reference clock (toll).

Due to an integrated 3rd order sigma delta converter, which samples the MPX signal, all further processing is done in the digital. After filtering the highly over sampled output of the A/D converter, the RDS/RBDS demodulator extracts the RDS data clock, RDS data signal and the quality information. A next RDS/RBDS decoder will synchronize the bit wise RDS stream to a group and block wise information. This processing includes an error detection and error correction algorithm. In addition, an automatic flywheel control avoids overheads in the data exchange between the RDS/RBDS processor and the host.

The device operates in accordance with the CENELEC Radio Data System (RDS) specification EN50067.

5.2.2 Fractional PLL

Figure 4. Fractional PLL



The fractional PLL (*Figure 4*) is used to generate from the XTI input clock one of the two possible system clocks (fsys) 8.55 MHz or 8.664 MHz. For this a setting for the input diver

factor (IDF), output divider factor (ODF), multiplication factor (MF) and fractional factor (FRA) must be found (max. fsys tolerance ±0.7KHz). For fractional mode an additional dither can be enabled (DITEN) to eliminate tones in the PLL output clock. The fractional mode can be disabled (FRAEN) if not needed.

The system clock (fsys) is equal to the XTI input clock after reset. After the PLL is locked, the system clock will switch automatically to the PLL output clock. Then the SPI/I^2C can be used at the maximum speed of 400kbits/s.

The initialization of the PLL must be done only once after hardware reset. After PLL locking the RDS functionality can be used regardless of the PLL.

It is possible to disabled all clock for power down mode, which can be external hardware reset .

5.2.3 Sigma delta converter

The sigma delta modulator is a 3rd order (second order-first order cascade) structure. Therefore a multi bit output (2 bit streams) represents the analog input signal. A next digital noise canceller will take the 2 bit streams and calculates a combined stream which is then fed to the decimation filter. The modulator works at a sampling frequency of fsys/2. The over sampling factor in relation to the band of interest (57KHz ± 2.4KHz) is 38.

5.2.4 Demodulator

The demodulator includes:

- RDS quality indicator with selectable sensitivity
- Selectable time constant of 57KHz PLL
- Selectable time constant of bit PLL
- Time constant selection done automatically or by software

The demodulator is fed by the 57KHz bandpass filter and interpolated multiplex signal. The input signal passes a digital filter extracting the sinus and cosinus components, to be used for further processing.

The sign of both channels are used as input for the ARI indicator and for the 57KHz PLL.

A fast ARI indicator determines the presence of an ARI carrier. If an ARI carrier is present, the 57KHz PLL is operating as a normal PLL, else it is operating as a Costas loop.

One part of the PLL is compensating the integral offset (frequency deviation between oscillator and input signal).

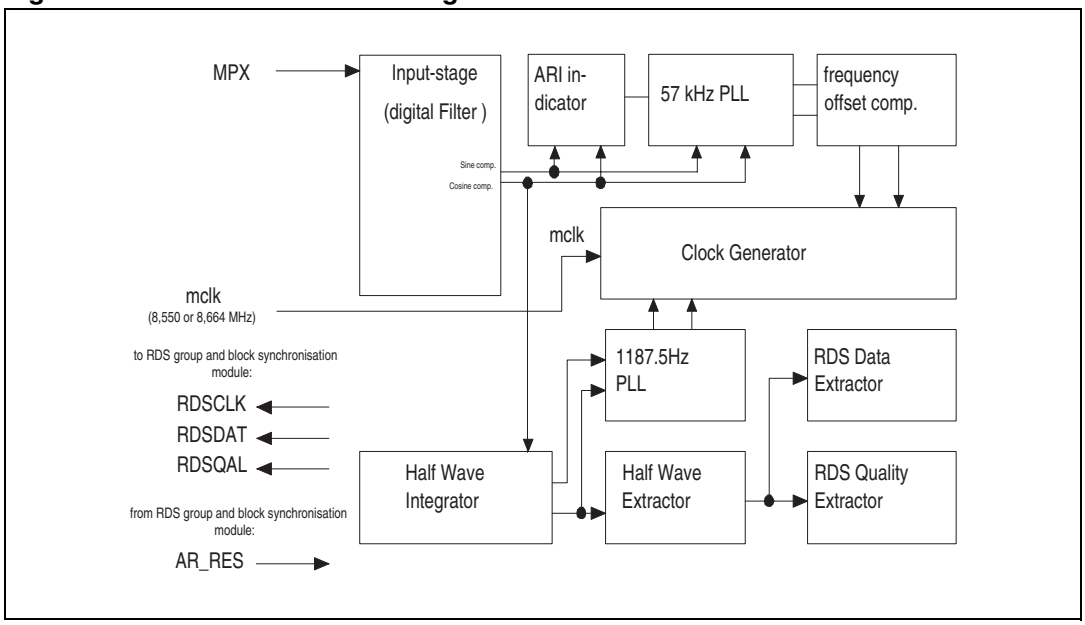
One channel of the filter is fed into the half wave integrator. Two half waves are created, with a phase deviation of 90 degrees. One wave represents the RDS component, whereas the other wave represents the ARI component.

The sign of both waves are used as reference for the bit PLL (1187.5 Hz).

The RDS wave is then fed into the half wave extractor. This leads into an RDS signal, which after integration and differential decoding represents the RDS data.

In a similar way a quality bit can be calculated. This is useful to optimize error correction.

Figure 5. Demodulator block diagram



The module needs a fixed clock of 8.55MHz. Optionally an 8.664MHz clock may be used by setting the corresponding bit in rds_bd_ctrl register (refer to *Table 42*).

In order to optimize the error correction in the group and block synchronization module, the sensitivity level of the quality bit can be adjusted in four steps with “qsens” bits rds_bd_ctrl[5:4]. Only bits marked as bad by the quality bit are allowed to be corrected in the group and block synchronization module. If an error correction is done on a good marked RDS bit, the “data_ok” bit rds_corrp[1] will not be set .

The RDS bit demodulator can be controlled by the bits 1-6 of rds_bd_ctrl register for example to select 57KHz PLL and 1187.5Hz PLL time constant. This is useful in order to achieve a fast synchronization after a program resp. frequency change (fast time constant) and to get a maximum of noise immunity after synchronization (slow time constant).

The user may choose between 2 possibilities via bit rds_bd_ctrl[1]:

a) Hardware selected time constant - In this case both pll time constants are reset to the fastest one, with a reset from the group and block synchronization module, or if the software decides to resynchronize by setting “ar_res” rds_int[5] . Then both PLLs increase automatically to the slowest time constant. This is done in four steps within a total time of 215.6 ms (256 RDS clocks).

b) Software selected time constant - In this case the time constant of both PLL can be selected individually by software (rds_bd_ctrl[4:2]). Four time constants (5 ms, 15 ms, 35 ms, 76 ms) can be set independently for 1187.5 Hz PLL and two time constants (2 ms, 10 ms) for the 57 KHz PLL.

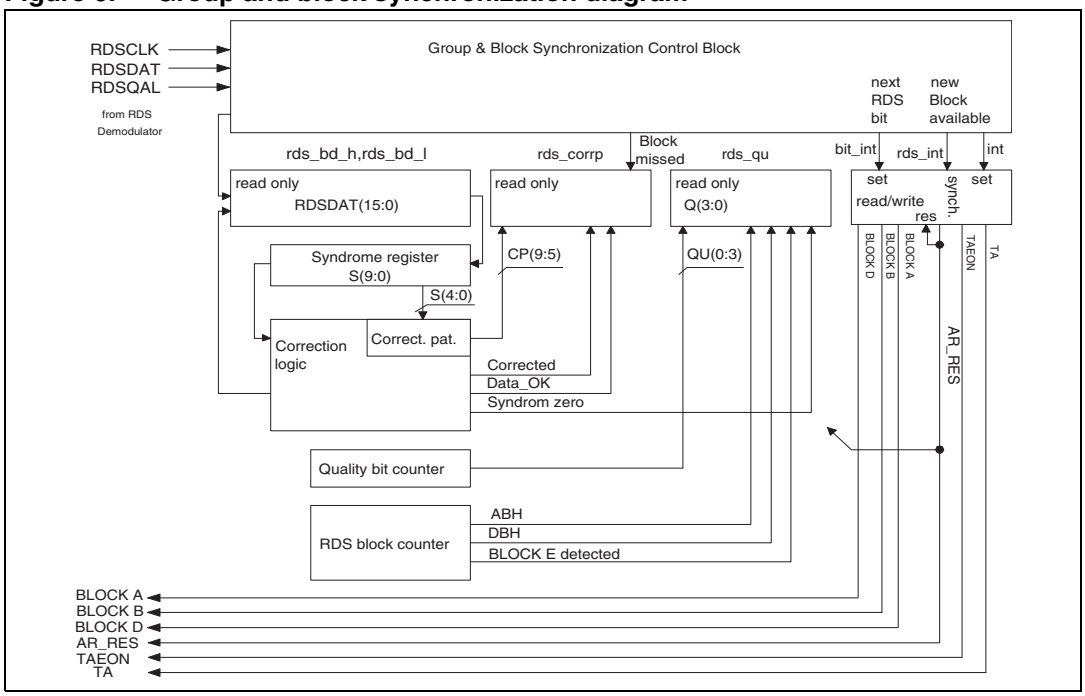
The sensitivity of the quality bit can be adjusted to four levels with the “qsens1” and “qsens0” rds_bd_ctrl[6:5] bits. “qsens1 = 0” and “qsens0 = 0” means minimum sensitivity, “qsens1 = 1” and “qsens0 = 1” maximum sensitivity.

5.2.5 Group and block synchronization module

The group and block synchronization module has the following features:

- Hardware group and block synchronization
- Hardware error detection
- Hardware error correction, using quality bit information to indicate bad corrections
- Hardware synchronization flywheel
- TA, TAEON information extraction
- Reset by software “ar_res”, which resets also RAM buffer addresses and RDS demodulator

Figure 6. Group and block synchronization diagram



This module is used to acquire group and block synchronization of the received RDS data stream, which is provided in a modified shortened cyclic code. For theory and implementation of modified shortened cyclic code and error correction, please refer to CENELEC Radio Data System (RDS) specification EN50067.

Group and block synchronization module can detect and correct five bit error burst in the data stream. If an error correction is done on a good quality marked RDS bit, the “data_ok” bit rds_corrp[1] won’t be set (refer to page 49). Before error correction, the five MSBs of the syndrome register are stored in the “cp” bits rds_corrp[7:3].

If the five LSBs of the syndrome register are zero, the “cp” pattern is used for error correction. After that operation the syndrome must become zero for valid RDS data. The type of error can be measured with the five “cp” bits in order to classify the reliability of the correction. Each bit set within “cp” means that one bit was corrected.

The two RDS data bytes rds_bd_h[7:0] and rds_bd_l[7:0] are available at the I^2C/SPI interface together with status bits rds_corrp[7:0] and rds_qu[7:0] giving reliability information of the data (refer to Figure 5). rds_int[7:0] bits are used for interrupt and group and block

synchronization control. A software reset “ar_res” rds_int[5] can be used to force resynchronization.

An endless 2 bit block counter (A, B, C or C’, D, A, B...) increments one step if a new RDS block was received. During synchronization the block counter is set to the first identified valid RDS block. Then every next RDS block must be of that type which is indicated by the block counter “blk” rds_qu[3:2]. If this is not true, then the syndrome becomes not zero (indicated by “synz” bit rds_qu[0]) and the “data_ok” bit rds_corrp[1] is not set. In case of USA BRDS, four consecutive E blocks can be received which are indicated by the “e” bit rds_qu[1].

The quality bit counter rds_qu[7:4] counts the bad quality marked RDS bits within a RDS block.

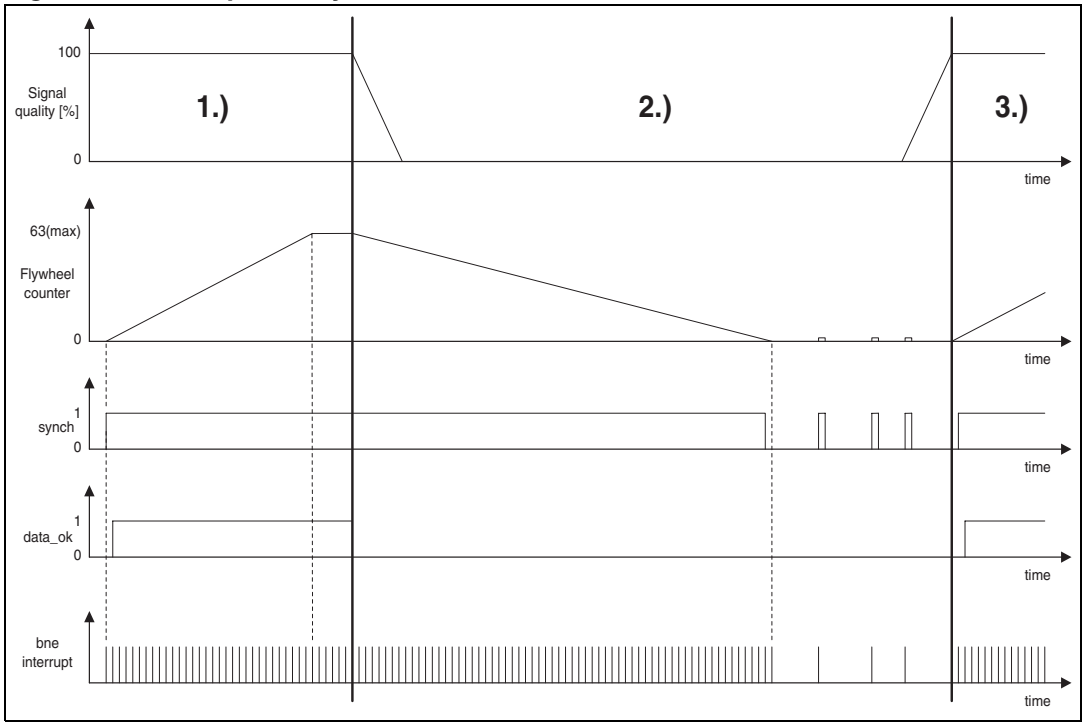
The group and block synchronization module extracts also TA, TAEON information and detects blocks types A, B, D (refer to *Table 37*) which can be used as interrupt sources.

The TA interrupt is performed in two cases: If within block B the group 0A or 0B is indicated and the TA bit is set or if within block B group 15B is indicated and the TA bit is set. The TAEON interrupt is performed, if within block B group 14B is indicated and the TA bit is set.

The interrupts can be recognized on the interrupt flag “int” rds_int[0] (refer to *Table 37*). The external open drain pin INTN (15) is the inverted version of the “int” flag.

5.2.6 Flywheel mechanism

Figure 7. Example for flywheel mechanism



Within group and block synchronization control block a 6 bit (64 states) flywheel counter is implemented to control RDS synchronization. After reset or a forced resynchronization by setting “ar_res” bit rds_int[5], this counter increments from zero to one, if a valid RDS block was detected. Valid means the syndrome has to be zero (“synz” = 1 rds_qu[0]) without any

error corrections done on good quality marked RDS bits. Then the RDS module is synchronized. This is indicated by “synch” bit rds_int[4] which is set if the flywheel counter is greater than zero. Every valid consecutive RDS block (A, B, C or C’, D, A, B...) increments the flywheel counter by two.

If the next consecutive RDS block has its syndrome not zero, or corrections are done on good quality marked RDS bits, then the flywheel counter decrements by one. If the flywheel counter becomes zero, then a new RDS block synchronization will be performed. If blocks of type E are detected (indicated by “e” bit rds_qu[1]), then the flywheel counter will be not modified, because in case of European RDS, block E is an error but not in case of USA BRDS. This means E blocks are treated as neutral in this RDS/BRDS implementation.

The “data_ok” bit rds_corrp[1] is set only, if the flywheel counter is greater than two, the syndrome of the detected RDS block is zero and if no error corrections are done on good quality marked RDS bits.

Figure 7 shows an example for the flywheel mechanism.

The first diagram shows the relative signal quality of 26 received RDS bits. 100% means that the last received 26 RDS bits are all marked as good by the demodulator and 0% that all are marked as bad.

The second diagram gives information about the flywheel counter status. The counter value could be between 0 and 63.

The next two charts showing the bits “synch” rds_int[4] and “data_ok” rds_corrp[1]

The last graph indicates every generated buffer not empty (bne) interrupt. After each interrupt the RDS data will be read out from the RAM buffer (within 22 ms), before next RDS block is written into. This is done to reset the interrupt flag “int” rds_int[0] each time. Further the “syncw” bit rds_bd_ctrl[0] is set to one, to store only synchronized RDS blocks .

The following case is considered now: First the receiving condition is good (section 1), then it is going to be worse (section 2) because of entering a tunnel, after leaving it is going to be better again (section 3).

Section 1:

After power up or resynchronization (“ar_res”, rds_int[5]), the first recognized RDS block is stored in the RAM buffer and generates an “bne” interrupt. At the same time “synch” bit rds_int[4] is set to one. With the next stored RDS block the “data_ok” bit rds_corrp[1] is set, because the flywheel counter becomes greater than two.

With every next RDS block the flywheel counter increments by two, until the upper margin of 63 is reached.

Section 2:

Because of entering a tunnel, the demodulator increases bad marked RDS bits until all are marked as bad. The flywheel counter decrements by one after each new RDS block because of error corrections done on good marked RDS bits or because the syndrome of the expected block was not zero after error correction. The “data_ok” bit rds_corrp[1] is set to zero whenever the flywheel counter decrements. Note that the synchronization flag “synch” rds_int[4] is set and the interrupt is performed after every expected RDS block, until the flywheel counter is zero.

Then the RDS is desynchronized. Now spurious interrupts could occur because of random RDS blocks detected during resynchronization process. If the time of

receiving bad signal is shorter than the decreasing time of the flywheel counter, then the RDS will keep its synchronization and stores RDS data every 22ms.

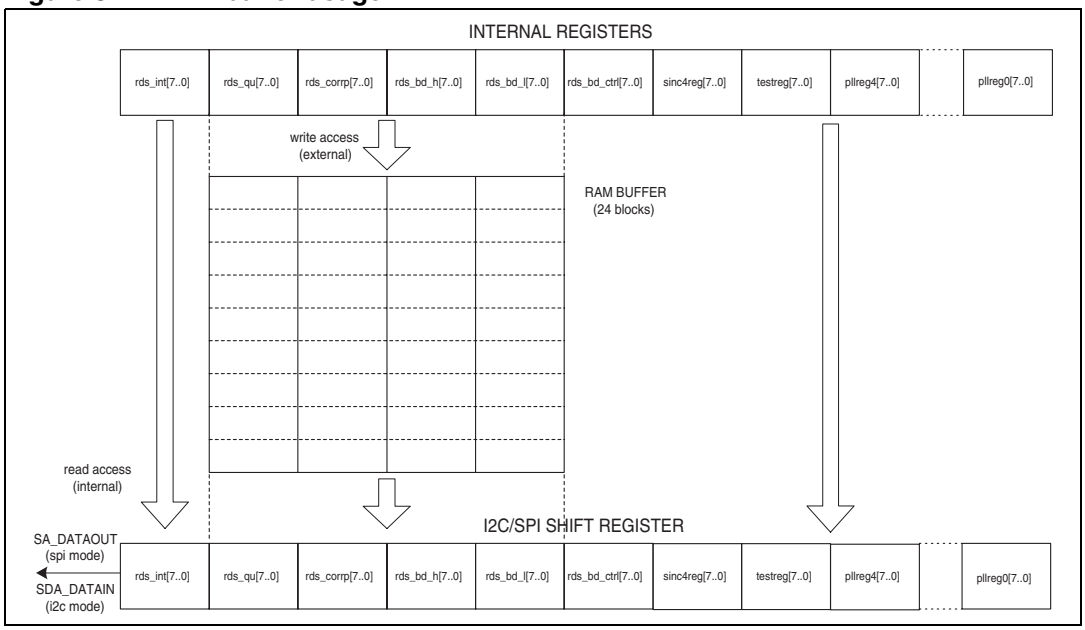
Section 3:

After leaving the tunnel, the signal is getting better and the RDS will be synchronized again as described in section 1.

5.2.7 RAM buffer

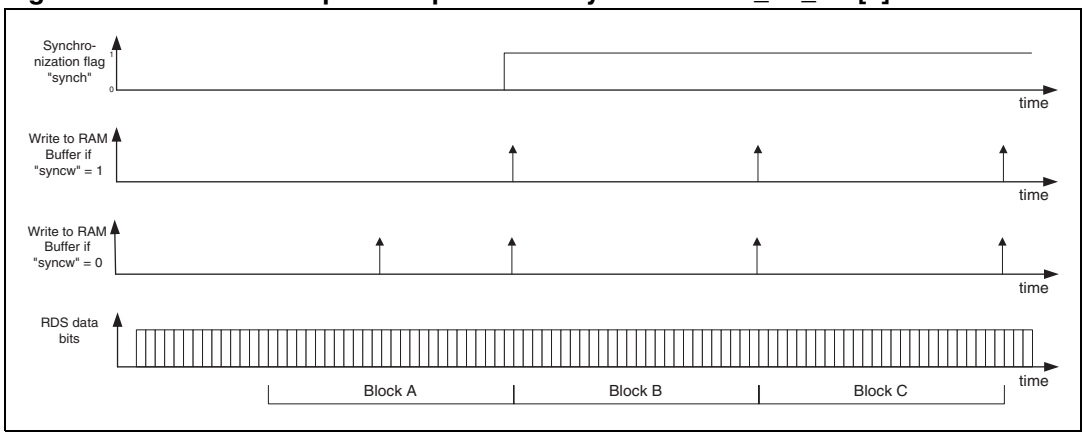
The RAM buffer can store up to 24 RDS blocks (rds_bd_h[7:0] and rds_bd_l[7:0]) with their related information (rds_qu[7:0] and rds_corrp[7:0]) (*Figure 7*):

Figure 8. RAM buffer usage



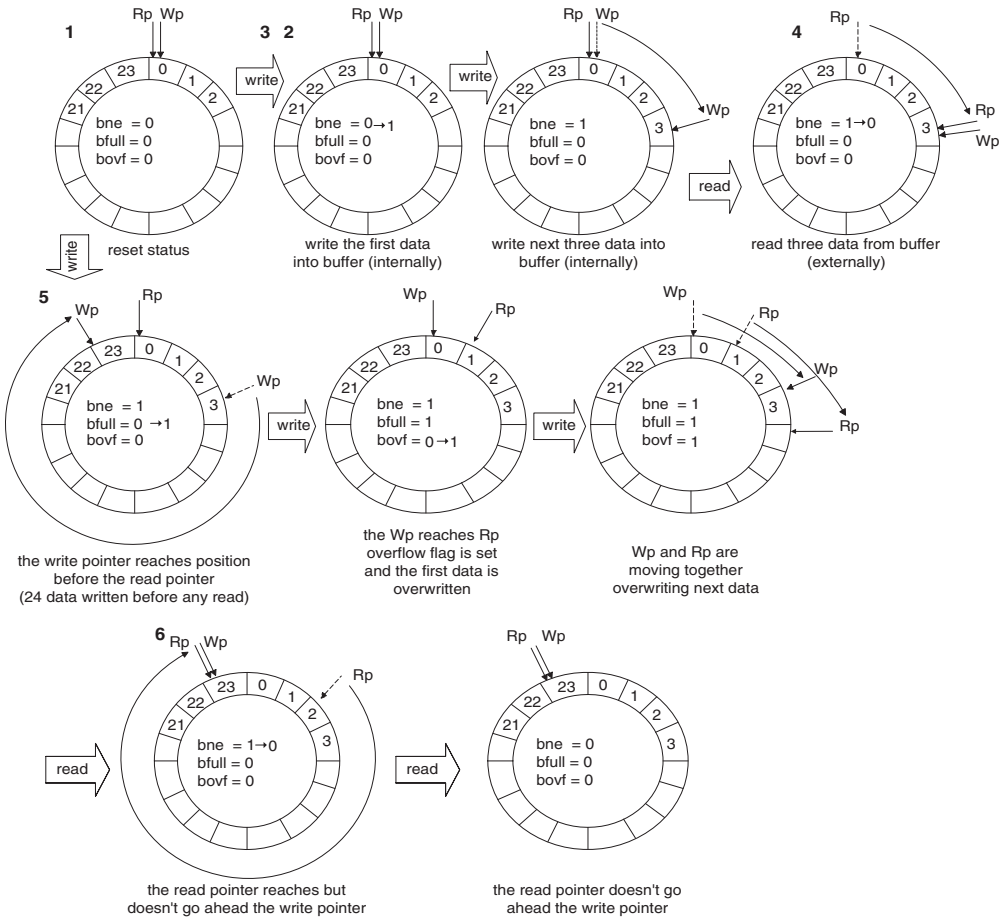
After power up, or after resynchronization by setting “ar_res” rds_int[5] to one, incoming RDS blocks are stored in the RAM buffer when synchronization has been established (*Figure 8.*). But if the bit “syncw” rds_bd_ctrl[0] (refer to page 50) is cleared, every received RDS block is stored, also without synchronization. This means if the RDS is not synchronized, every received consecutive 26 RDS data bits are treated as a RDS block.

Figure 9. RAM buffer update depends on “syncw” bit rds_bd_ctrl[0]



The RAM buffer is used as a circular FIFO (*Figure 9*). If more than 24 blocks are written, the oldest data will be overwritten. One level of the buffer consists of 4 bytes (2 information bytes, 2 RDS data bytes). If less than 4 bytes of the RAM buffer are read out from the master via the SPI or I^2C interface, the buffer address will not be incremented.

Figure 10. RAM buffer states



Note : The read pointer Rp is driven externally through micro read access, and the write pointer Wp is driven internally on every incoming block.

The different states of the buffer are indicated with the help of following flags:

- "bne", buffer not empty. It is set as soon as one RDS block is written in the buffer, and reset when reading rds_int register. This flag is a bit of rds_int register, it is also an interrupt source .
- "bfull", buffer full. It is set when 24 RDS blocks have been written, that is to say that there is about 20 ms to read out the buffer content before an overflow occurs. This flag is an interrupt source.
- "bovf", buffer overflow. It is set if more than 24 RDS blocks are written. This flag is a bit of register rds_corrp (refer to *Table 39*) and is cleared only by reading the whole buffer (24 blocks).

An address reset of the RAM buffer can be performed by writing a 1 to “ar_res” bit in rds_int register, it also forces a resynchronization.

Figure 10 describes the different states of the buffer with corresponding flags values:

1. This is the reset state, read (Rp) and write pointer (Wp) pointing at the same location 0. The buffer is empty.
2. After the first buffer write operation, Wp points to the last written data (0, it is not incremented) and the flag “bne” (buffer not empty) is set.
3. After next buffer write operation, Wp points to the last written data (3, incremented address).
4. After buffer read operation, Rp points to incremented address (data to be read on the next read cycle), following the Wp. As soon as Rp reaches the Wp (of value 3), it is not incremented to 4 and flag “bne” is reset. Rp never goes ahead the Wp.
5. If the buffer is full (i.e. 24 blocks have been written before any read), flag “bfull” is set. If no read operation is performed, on next write operation “bovf” (buffer overflow) is set, and each subsequent write operation will overwrite the oldest data of the RAM buffer. Rp is moved in front of the Wp.
6. If the whole content of the buffer has already been read, subsequent read operation will always read the last written location - Rp never goes ahead the Wp.

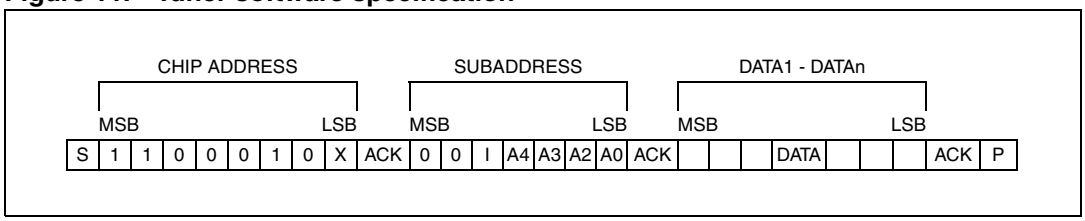
6 Software specifications

6.1 Tuner software specification

The interface protocol comprises:

- start condition (S)
- chip address byte
- subaddress byte
- sequence of data (N bytes + Acknowledge)
- stop condition (P)

Figure 11. Tuner software specification



S = Start

P = Stop

ACK = Acknowledge

D = Device Address

X = R/W bit

I = Pagemode

A = Subaddress

Table 9. Address organization

Function	Addr	7	6	5	4	3	2	1	0
CHARGEPUMP	0	LDENA	CURRH	B1	B0	A3	A2	A1	A0
PLL COUNTER	1	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
	2	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
TV1	3	TV1O7	TV1O6	TV1O5	TV1O4	TV1O3	TV1O2	TV1O1	TV1O0
TV2	4	TV2O7	TV2O6	TV2O5	TV2O4	TV2O3	TV2O2	TV2O1	TV2O0
IFC CTRL 1	5	LM	CASF	-	-	IFENA	IFS2	IFS1	IFS0
IFC CTRL 2	6	EW2	EW1	EW0	CF4	CF3	CF2	CF1	CF0
not valid	7	-	-	-	-	-	-	-	-
QUALITYISS	8	TISS2	TISS1	TISS0	TVWB	ISS30	ISS80	ISSON	CTLOFF
QUALITY AC	9	ACNTH1	ACNTH0	ACWTH2	ACWTH1	ACWTH0	ACG	ACF	-
QUALITY MP	10	MPAC	APPM2	APPM1	MPTH1	MPTH0	MPG	MPF	MPOFF
QUALITYDEV	11	BWCTL	DTH1	DTH0	DWTH1	DWTH0	TDEV2	TDEV1	TDEV0

Table 9. Address organization (continued)

Function	Addr	7	6	5	4	3	2	1	0
MUTE1	12	0	-	-	-	-	-	-	-
MUTE2	13	-	1	1	1	1	-	-	SMCTH
VCO/PLLREF	14	-	-	RC2	RC1	RC0	VCOD2	VCOD1	VCOD0
FMAGC	15	-	KAGC2	KAGC1	KAGC0	IFAGC1	IFAGC0	RFAGC1	RFAGC0
not valid	16	-	-	-	-	-	-	-	-
DEM ADJ	17	DNB1	DNB0	DEM5	DEM4	DEM3	DEM2	DEM1	DEM0
LEVEL	18	ODSW	-	SMSL	SL4	SL3	SL2	SL1	SL0
IF1/XTAL	19	XTAL4	XTAL3	XTAL2	XTAL1	XTAL0	IFG11	IFG10	IFG2
TANK ADJ	20	IF1T3	IF1T2	IF1T1	IF1T0	-	-	-	-
I/Q ADJ	21	ODCUR	-	G1	G0	PH3	PH2	PH1	PH0
TESTCTRL1	22	-	ISSIN	TOUT	TIN	CLKSEP	TEST3	TEST2	TEST1
TESTCTRL2	23	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
TESTCTRL3	24	-	TINACM	TINMP	TINAC	OUT11	OUT10	OUT9	OUT8
TESTCTRL4	25	-	-	-	OUT16	OUT15	OUT14	OUT13	OUT12

Table 10. Control register function

Register Name	Function
A	Charge pump high current
ACF	Adjacent channel filter select
ACG	Adjacent channel filter gain
ACM	Threshold for startpoint adjacent channel mute
ACMD	Adjacent channel mute depth
ACNTH	Adjacent channel narrow band threshold
ACWTH	Adjacent channel wide band threshold
APPM	Application mode quality detection
B	Charge pump low current
BWCTL	ISS filter fixed bandwith (ISS80) in automatic control
CASF	Check alternative station frequency
CF	Center frequency IF counter
CLKSEP	Clock separation (only for testing)
CTLOFF	Switch off automatic control of ISS filter
CURRH	Set current high charge pump
DEM	Demodulator offset
DNB	Demodulator noise spike blanking
DTH	Deviation detector threshold for ISS filter “OFF”

Table 10. Control register function (continued)

Register Name	Function
DWTH	Deviation detector threshold for ISS filter narrow/wide
EW	Frequency error window IF counter
F100K	Corner frequency of AC-mute high pass filter
G	I/Q mixer gain adjust
IF1T	Miixer1 tank adjust
IFAGC	IF AGC
IFENA	IF counter enable
IFG	IF1 amplifier gain (10.7MHz)
IFS	IF counter sampling time
ISSIN	Test input for ISS filter
ISSON	ISS filter “ON”
ISS30	ISS filter 30KHz weather band
ISS80	ISS filter narrow/mid switch
KAGC	Keying AGC
LDENA	Lock detector enable
LM	Local mode seek stop
MENA	Softmute enable
MPAC	Adjacent channel control by multipath
MPF	Multipath filter frequency
MPG	Multipath filter gain
MPOFF	Multipath control “OFF”
MPTH	Multipath threshold
ODCUR	Current for overdeviation-correction
ODSW	Overdeviation-correction enable
OUT	Test output (only for testing)
PC	Counter for PLL (VCO frequency)
PH	I/Q mixer phase adjust
RC	Reference counter PLL
RFAGC	RF AGC
SL	S meter slider
SMCTH	Softmute capacitor threshold for ISS “ON”
SMD	Softmute depth threshold
SMSL	S meter slope
SMTH	Softmute startpoint threshold
TDEV	Time constant for deviation detector

Table 10. Control register function (continued)

Register Name	Function
TEST	Testing PLL/IFC (only for testing)
TIN	Switch FSU PIN to TEST input (only for testing)
TINAC	Test input adjacent channel (only for testing)
TINACM	Test input adjacent channel mute (only for testing)
TINMP	Test input multipath(only for testing)
TISS	Time constant for ISS filter “ON”/”OFF”
TOUT	Switch FSU PIN to Test output (only for testing)
TVO	Tuning voltage offset for prestage
TVWB	Tuning voltage offset for prestage (weather band mode)
VCOD	VCO divider
XTAL	Xtal frequency adjust

Table 11. Subaddress

MSB							LSB	Function
		I	A4	A3	A2	A1	A0	
			0	0	0	0	0	Charge pump control
			0	0	0	0	1	PLL lock detector
			-	-	-	-	-	-
			1	0	1	0	1	I/Q ADJ
		0						Page mode “OFF”
		1						Page mode enable

6.2 Data byte specification

Table 12. Addr 0 charge pump control

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
				0	0	0	0	High current = 0mA
				0	0	0	1	High current = 0.5mA
				0	0	1	0	High current = 1mA
				0	0	1	1	High current = 1.5mA
				-	-	-	-	-
				1	1	1	1	High current = 7.5mA
		0	0					Low current = 0µA
		0	1					Low current = 50µA
		1	0					Low current = 100µA
		1	1					Low current = 150µA
	0							Select low current
	1							Select high current
0								Lock detector disable
1								Lock detector enable

Table 13. Addr 1 PLL counter 1 (LSB)

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
0	0	0	0	0	0	0	0	LSB = 0
0	0	0	0	0	0	0	1	LSB = 1
0	0	0	0	0	0	1	0	LSB = 2
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	LSB = 252
1	1	1	1	1	1	0	1	LSB = 253
1	1	1	1	1	1	1	0	LSB = 254
1	1	1	1	1	1	1	1	LSB = 255

Table 14. Addr 2 PLL counter 2 (MSB)

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
0	0	0	0	0	0	0	0	MSB = 0
0	0	0	0	0	0	0	1	MSB = 256
0	0	0	0	0	0	1	0	MSB = 512

Table 14. Addr 2 PLL counter 2 (MSB) (continued)

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	MSB = 64768
1	1	1	1	1	1	0	1	MSB = 65024
1	1	1	1	1	1	1	0	MSB = 65280
1	1	1	1	1	1	1	1	MSB = 65536

Swallow mode: f_{VCO}/f_{SYN} = LSB + MSB + 32

Table 15. Addr 3,4 TV1,2 (offset refered to tuning voltage PIN 28)

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
	0	0	0	0	0	0	0	Tuning Voltage Offset = 0
	0	0	0	0	0	0	1	TVO = 25mV
	0	0	0	0	0	1	0	TVO = 50mV
-	-	-	-	-	-	-	-	-
	1	1	1	1	1	1	1	TVO = 3175mV
0								-TVO
1								+TVO

Table 16. Addr 5 IF counter control 1

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
					0	0	0	t_{Sample} = 20.48ms (FM)128ms (AM)
					0	0	1	t_{Sample} = 10.24ms (FM)64ms (AM)
					0	1	0	t_{Sample} = 5.12ms (FM)32ms (AM)
					0	1	1	t_{Sample} = 2.56ms (FM)16ms (AM)
					1	0	0	t_{Sample} = 1.28ms (FM)8ms (AM)
					1	0	1	t_{Sample} = 640µs (FM)4ms (AM)
					1	1	0	t_{Sample} = 320µs (FM)2ms (AM)
					1	1	1	t_{Sample} = 160µs (FM)1ms (AM)
				0				IF counter disable / stand by
				1				IF counter enable
		0	1					has to be set
	0							Disable mute & AGC on hold

Table 16. Addr 5 IF counter control 1 (continued)

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
	1							Enable mute & AGC on hold
0								Disable local mode
1								Enable local mode (PIN diode current = 0.5mA) “ON”

Table 17. Addr 6 IF counter control 2

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
			0	0	0	0	0	f_{Center} = 10.60625MHz
			0	0	0	0	1	f_{Center} = 10.61250MHz
-	-	-	-	-	-	-	-	-
			0	1	0	1	1	f_{Center} = 10.67500MHz
			0	1	1	0	0	f_{Center} = 10.68125MHz
			0	1	1	0	1	f_{Center} = 10.68750MHz
			0	1	1	1	0	f_{Center} = 10.69375MHz
			0	1	1	1	1	f_{Center} = 10.70000MHz
-	-	-	-	-	-	-	-	-
			1	1	1	1	1	f_{Center} = 10.80000MHz
0	0	0						Not valid
0	0	1						Not valid
0	1	0						Not valid
0	1	1						Δf = 6.25KHz
1	0	0						Δf = 12.5KHz
1	0	1						Δf = 25KHz
1	1	0						Δf = 50KHz
1	1	1						Δf = 100KHz

Table 18. Addr 7 not valid

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
0	0	0	0	0	0	0	0	has to be set

Table 19. Addr 8 quality ISS filter

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
							0	ISS filter control “ON”
							1	ISS filter control “OFF”
						0		Switch ISS filter “OFF”
						1		Switch ISS filter “ON”
					0			Switch “OFF” ISS filter 120KHz
					1			Switch “ON” ISS filter 80KHz
				0				Switch “OFF” ISS filter 30KHz for weatherband
				1				Switch “ON” ISS filter 30KHz for weatherband
			0					Disable TV offset for weather band
			1					Enable TV offset for weather band (+4V)
0	0	0						discharge current1µA, charge current mid 74µA narrow124µA
0	0	1						discharge current3µA, charge current mid 72µA narrow122µA
0	1	0						discharge current 5µA, charge current mid 70µA narrow 120µA
0	1	1						discharge current 7µA, charge current mid 68µA narrow 118µA
-	-	-						-
1	1	1						discharge current 15µA,charge current mid 60µA narrow 110µA

Table 20. Addr 9 quality detection adjacent channel

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
							0/1	Not valid
						0		AC highpass frequency 100KHz
						1		AC bandpass frequency 100KHz
					0			AC gain 32dB
					1			AC gain 38dB
		0	0	0				AC wide band threshold 0.25V
		0	0	1				AC wide band threshold 0.35V
		0	1	0				AC wide band threshold 0.45V
		-	-	-				-
		1	1	1				AC wide band threshold 0.95V
0	0							AC narrow band threshold 0.0V
0	1							AC narrow band threshold 0.1V
1	0							AC narrow band threshold 0.2V
1	1							AC narrow band threshold 0.3V

Table 21. Addr 10 quality detection multipath

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
							0	Multipath control “ON”
							1	Multipath control “OFF”
						0		MP bandpass frequency 19KHz
						1		MP bandpass frequency 31KHz
					0			MP gain 12dB
					1			MP gain 23dB
			0	0				MP threshold 0.50V
			0	1				MP threshold 0.75V
			1	0				MP threshold 1.00V
			1	1				MP threshold 1.25V
	0	0						Application mode 1
	0	1						Application mode 2
0								Multipath eliminates ac
1								Multipath eliminates ac and ac+

Table 22. Addr 11 quality deviation detection

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
					0	0	0	charge current 34µA, discharge current 6µA
					0	0	1	charge current 32µA, discharge current 8µA
					0	1	0	charge current 30mA, discharge current 10µA
					0	1	1	charge current 28µA, discharge current 12µA
					-	-	-	-
					1	1	1	charge current 20µA, discharge current 20µA
			0	0				DEV threshold for ISS narrow/wide 30KHz
			0	1				DEV threshold for ISS narrow/wide 45KHz
			1	0				DEV threshold for ISS narrow/wide 60KHz
			1	1				DEV threshold for ISS narrow/wide 75KHz
	0	0						DEV threshold for ISS filter “OFF” ratio 1.5
	0	1						DEV threshold for ISS filter “OFF” ratio 1.4
	1	0						DEV threshold for ISS filter “OFF” ratio 1.3
	1	1						DEV threshold for ISS filter “OFF” ratio 1

Table 22. Addr 11 quality deviation detection (continued)

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
0								Disable ISS filter to fixed bandwith (ISS80) in automatic control
1								Enable ISS filter to fixed bandwith (ISS80) in automatic control

Table 23. Addr 14 VCODIV/PLLREF

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
						0	0	not valid (only for testing)
						0	1	VCO frequency divided by 2
						1	0	VCO frequency divided by 3
						1	1	original VCO frequency
					0			VCO" I" signal 0°C
					1			VCO "I" signal 180°C
		1	0	0				PLL reference frequency 50KHz
		1	0	1				PLL reference frequency 25KHz
		1	1	0				PLL reference frequency 10KHz
		1	1	1				PLL reference frequency 9KHz
		0	0	0				PLL reference frequency 2KHz
0	0							has to be set

Table 24. Addr 15 FM AGC

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
						0	0	RFAGC threshold $V_{3\text{-}5TH}$ = 82(74 ANT)dBµV
						0	1	RFAGC threshold $V_{3\text{-}5TH}$ = 88(80 ANT)dBµV
						1	0	RFAGC threshold $V_{3\text{-}5TH}$ = 92(84 ANT)dBµV
						1	1	RFAGC threshold $V_{3\text{-}5TH}$ = 94(86 ANT)dBµV
				0	0			IFAGC threshold V_{77TH} = 86(60 ANT)dBµV
				0	1			IFAGC threshold V_{77TH} = 92(66 ANT)dBµV
				1	0			IFAGC threshold V_{77TH} = 96(70 ANT)dBµV
				1	1			IFAGC threshold V_{77TH} = 98(72 ANT)dBµV
	0	0	0					KAGC threshold 80dBµV
	0	0	1					KAGC threshold 82dBµV
	0	1	0					KAGC threshold 84dBµV

Table 24. Addr 15 FM AGC (continued)

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
	0	1	1					KAGC threshold 86dBµV
	1	0	0					KAGC threshold 88dBµV
	1	0	1					KAGC threshold 90dBµV
	1	1	0					KAGC threshold 92dBµV
	1	1	1					Keying AGC “OFF”
0								has to be “0”

Table 25. Addr 16 not valid

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
1	1	1	1	1	1	1	1	has to be set

Table 26. Addr 17 FM demodulator fine adjust

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
		0	0	0	0	0	0	0mV
		0	0	0	0	0	1	+8.5mV
		0	0	0	0	1	0	+17mV
		-	-	-	-	-	-	-
		0	1	1	1	1	1	+263.5mV
		1	0	0	0	0	0	0mV
		1	0	0	0	0	1	-8.5mV
		1	0	0	0	1	0	-17mV
		-	-	-	-	-	-	-
		1	1	1	1	1	1	-263.5mV
0	0							Spike cancelation ”OFF”
0	1							Threshold for spike cancelation 270mV
1	0							Threshold for spike cancelation 520mV
1	1							Threshold for spike cancelation 750mV

Table 27. Addr 18 s-meter slider

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
				0	0	0	0	S meter slider offset SL=0dB
				0	0	0	1	S meter offset SL=1dB
				0	0	1	0	S meter offset SL=2dB
				-	-	-	-	-
				1	1	1	1	S meter offset SL=15dB
			0					S meter offset -SL
			1					S meter offset +SL
		0						S Meter slope 1V/decade
		1						S meter slope 1.5V/decade
	1							has to be set
0								Overdeviation correction “ON”
1								Overdeviation correction “OFF”

Table 28. Addr 19 IF gain/xtal adjust

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
							0	IF1 gain2 9dB
							1	IF1 gain2 11dB
					0	0		IF1 gain1 9dB
					0	1		IF1 gain1 11dB
					1	0		IF1 gain1 12dB
					1	1		IF1 gain1 15dB
0	0	0	0	0				C_{Load} 0pF
0	0	0	0	1				C_{Load} 0.75pF
0	0	0	1	0				C_{Load} 1.5pF
0	0	0	1	1				C_{Load} 2.25pF
0	0	1	0	0				C_{Load} 3pF
-	-	-	-	-				-
1	1	1	1	1				C_{Load} 23.25pF

Table 29. Addr 20 tank adjust

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
				0	0	0	0	has to be set
0	0	0	0					10.7MHz 0pF
0	0	0	1					10.7MHz 0.55pF
0	0	1	0					10.7MHz 1.1pF
0	0	1	1					10.7MHz 1.65pF
-	-	-	-					-
1	1	1	1					10.7MHz 8.25pF

Table 30. Addr 21 I/Q mixer1 adjust

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
				0	0	0	0	-7°
				0	0	0	1	-6°
				0	0	1	0	-5°
				-	-	-	-	-
				0	1	1	1	0°
				1	0	0	0	+1°
				1	0	0	1	+2°
				-	-	-	-	-
				1	1	1	1	+8°
		0	0					0%
		0	1					-1%
		1	0					+1%
		1	1					0%
	x							not used
0								Overdeviation correction current max=45µA
1								Overdeviation correction current max=90µA

Table 31. Addr 22 test control 1

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
x	x	x	x	x	x	x	x	Only for testing (have to be set to 0)

Table 32. Addr 23 test control 2

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
x	x	x	x	x	x	x	x	Only for testing (have to be set to 0)

Table 33. Addr 24 test control 3

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
x	x	x	x	x	x	x	x	Only for testing (have to be set to 0)

Table 34. Addr25 test control 4

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
x	x	x	x	x	x	x	x	Only for testing (have to be set to 0)

6.3 RDS decoder software specification

6.3.1 Programming through serial bus interface

The serial bus interface is used to access the different registers of the chip. It is able to handle both I^2C and

SPI transfer protocols, the selection between the two modes is done thanks to the pin CSN:

- if the pin CSN is high, the interface operates as an I^2C bus.
- if the pin CSN is asserted low, the interface operates as a SPI bus.

In both modes, the device is a slave, i.e the clock pin SCL_CLK is only an input for the chip.

Depending on the transfer mode, external pins have alternate functions as following:

Table 35. External pins alternate functions

pin	function in SPI mode (CSN=0)	function in I^2C mode (CSN=1)
SCL_CLK	CLK (serial clock)	SCL (serial clock)
SDA_DATAIN	DATAIN (data input)	SDA (data line)
SA_DATAOUT	DATAOUT (data output)	SA (slave address)

13 registers are available with read or read/write access:

Table 36. Registers description

register	access rights	function
rds_int[7:0]	read/write	interrupt source setting, synch., bne information
rds_qu[7:0]	read	quality counter, actual block name
rds_corrp[7:0]	read	error correction status, buffer ovf information
rds_bd_h[7:0]	read	high byte of current RDS block
rds_bd_l[7:0]	read	low byte of current RDS block
rds_bd_ctrl[7:0]	read/write	frequency, quality sensitivity, demodulator pll settings
sinc4reg[7:0]	read/write	sinc4 filter settings (for internal use only)
testreg[7:0]	read/write	test modes (for internal use only)
pllreg4[7:0]	read/write	PLL control register 4
pllreg3[7:0]	read/write	PLL control register 3
pllreg2[7:0]	read/write	PLL control register 2
pllreg1[7:0]	read/write	PLL control register 1
pllreg0[7:0]	read/write	PLL control register 0

The meaning of each bit is described below:

Table 37. rds_int register

rds_int	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	0
bit name	write	bne	ar_res	synch	itsrc2	itsrc1	itsrc0	int
access	r/w	r	r/w	r	r/w	r/w	r/w	r

Interrupt bit. It is set to one on every programmed interrupt. It is reset by reading rds_int register. The inverted version is also externally available on RDSINT pin.
itsrc[2:0] selects interrupt source (1). Block A, B, D and TA, TA EON interrupts only if "synch" =1.
Synchronization information (refer to pages 28-29). 1: The module is already synchronized. 0: The module is synchronizing.
It is used to force a resynchronization. If it is set to one, the RDS modules are forced to resynchronization state and the RAM buffer address is reset. This bit is reset automatically. It is read always as zero.
Buffer not empty. 1: At least one block is present in the RAM buffer. 0: The RAM buffer is empty.
rds_int, rds_bd_ctrl and pllreg4-0 write order. **This bit is only used in SPI mode and is read always as zero**. 1: Update of rds_int, rds_bd_ctrl and pllreg4-0 with data shifted in. 0: No update of rds_int, rds_bd_ctrl and pllreg4-0.

(1)

interrupt source	itsrc2	itsrc1	itsrc0
no interrupt	0	0	0
buffer not empty	0	0 1	
buffer full	0	1 0	
block A	0	1 1	
block B	1	0 0	
block D	1	0 1	
TA	1	1 0	
TA EON	1	1 1	

(1) If the interrupt source is changed form block A, B, D, TA, TA EON to another one "no interrupt" must be set before to clear the previous interrupt acknowledge.

Table 38. rds_qu register

rds_qu	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	0
bit name	qu3	qu2	qu1	qu0	blk1	blk0	e	synz
access	r	r	r	r	r	r	r	r

It indicates if error correction was successful. 1: The syndrome was zero after error correction. 0: The syndrome did not become zero and therefore the error correction was not successful.
1: Block E is detected. This indicates a paging block which is deÞned in the RBDS speciÞcation used in the United States of America. 0: An ordinary RDS block A, B, C, C« or D is detected, or no valid syndrome was found.
Bit 0 of block counter (2).
bit 1 of block counter (2).
bit 0 of quality counter (3).
bit 1 of quality counter (3).
bit 2 of quality counter (3).
bit 3 of quality counter (3).

(2)

block name	blk1	blk0
block A	0	0
block B	0	1
block C,C'	1	0
block D	1	1

(2) If "syncw" =1 of rds_bd_ctrl register, the block counter indicates the expected RDS block.

(3) qu[3...0] counts the number of bits (max.16) which are marked as bad by the demodulator within each RDS block. It could be used as a quality information, indicating the maximum number of bits which are allowed to be corrected.

Table 39. rds_corrp register

rds_corrp	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	0
bit name	cp9	cp8	cp7	cp6	cp5	correct	dat_ok	bovf
access	r	r	r	r	r	r	r	r

Buffer overflow 1: More than 24 blocks have been written into the buffer. 0: No buffer data has been overwritten.
Information if the current RDS data could be used. 1: A correct syndrome was detected and no error correction was done on a good quality marked RDS bit and the flywheel counter is greater than 2 (RDS data is OK). 0: The syndrome was wrong, or an error correction was done on a good quality marked RDS bit, or the flywheel counter is lower than 3 (RDS data is not OK).
It is an information about error correction. 1: An error correction was done. 0: The actual RDS block is detected as error free.
bit 5 of the syndrome register(4).
bit 6 of the syndrome register(4).
bit 7 of the syndrome register(4).
bit 8 of the syndrome register(4).
bit 9 of the syndrome register(4).

(4) (Refer to CENELEC Radio Data System speciÞcation EN50067, ANNEX B). When bits 0...4 of the syndrome register are zero, a possible error burst is detected. With help of the correction pattern (bits 5...9 of the syndrome register), the type of error can be measured, in order to classify the reliability of the correction.

Table 40. rds_bd_h register

rds_bd_h	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	0
bit name	m15	m14	m13	m12	m11	m10	m9	m8
access	r	r	r	r	r	r	r	r

bit 15 of the actual RDS 16 bits information.
bit 14 of the actual RDS 16 bits information.
bit 13 of the actual RDS 16 bits information.
bit 12 of the actual RDS 16 bits information.
bit 11 of the actual RDS 16 bits information.
bit 10 of the actual RDS 16 bits information.
bit 9 of the actual RDS 16 bits information.
bit 8 of the actual RDS 16 bits information.

Table 41. rds_bd_l register

rds_bd_l	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	0
bit name	m7	m6	m5	m4	m3	m2	m1	m0
access	r	r	r	r	r	r	r	r

bit 7 of the actual RDS 16 bits information.
bit 6 of the actual RDS 16 bits information.
bit 5 of the actual RDS 16 bits information.
bit 4 of the actual RDS 16 bits information.
bit 3 of the actual RDS 16 bits information.
bit 2 of the actual RDS 16 bits information.
bit 1 of the actual RDS 16 bits information.
bit 0 of the actual RDS 16 bits information.

Table 42. rds_bd_ctrl register

rds_bd_ctrl	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	1
bit name	freq	qsens1	qsens0	pllb1	pllb0	pllf	shw	syncw
access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Write into buffer if synchronized (refer to page 10-12) (8) 1: Write into buffer only if synchronized (reset value). 0: Write into buffer any incoming RDS block.
Select PLL time constants by software or hardware (8) 1: Software. Time constants are selected by pllb[1:0] respectively pllf. 0: Hardware (reset value). Time constants automatically increase after reset or resynchronization.
Set the 57 kHz pll time constant (5) (8).
Bit 0 of 1187.5 Hz pll time constant (6) (8).
Bit 1 of 1187.5 Hz pll time constant (6) (8).
Bit 0 of quality sensitivity (7) (8).
Bit 1 of quality sensitivity (7) (8).
Select internal master clock frequency (fsys): 1: 8.664 MHz. 0: 8.55 MHz (reset value).

(5)

pllf	lock time needed for 90 deg deviation
0	2 ms
1	10 ms

(6)

pllb1	pllb0	lock time needed for 90 deg deviation
0	0	5 ms (reset status)
0	1	15 ms
1	0	35 ms
1	1	76 ms

(7) Select sensitivity of quality bit.
00: minimum (reset value)
11: maximum

(8) Bit 5 "ar_res" of rds_int register will clear the bits 0-6 of the rds_bd_ctrl register.

Table 43. sinc4reg register

sinc4reg	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	0
bit name	-	-	-	-	-	-	-	-
access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

sinc4reg register is for internal use only. For application this register must be always Þlled with æros.

Table 44. testreg register

testreg	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	0	0	0
bit name	-	-	-	-	-	-	-	-
access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

testreg register is for internal use only. For application this register must be always Þlled with æros.

Table 45. pllreg4 register

pllreg4	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	1	1	0	0
bit name	LOCK	LLOCK	PLLEN	PWDN	DITEN	FRAEN	TEST1	TEST0
access	r	r	r/w	r/w	r/w	r/w	r/w	r/w

This bit is for internal test only.
This bit is for internal test only.
PLL factional mode enable (10). 1: Fractional mode enabled. 0: Fractional mode disabled.
PLL fractional dither enable (10). 1: Fractional dither enabled. 0: Fractional dither disabled.
Power down mode. 0: Normal mode 1: Power down mode. All clocks are stopped. This mode can only be exit by hardware reset.
PLL enable. If this bit is set the PLL will be initialized with the values of the pllreg4-0 registers. After PLL locking, the system clock (fsys) is switched to the PLL output clock which must be 8.55 or 8.664 MHz. Clearing this bit will switch fsys back to the XTI clock.
PLL lost lock. This bit is set if the PLL is used and loses lock. It will be cleared if the PLL is disabled and enabled again.
PLL lock. 1: PLL is currently locked. 0: PLL is currently out of lock.

Table 46. pllreg3 register

pllreg3	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	0	0	0	0	0	1	1	0
bit name	-	IDF4	IDF3	IDF2	IDF1	IDF0	ODF4	ODF3
access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

bit 3 of PLL output divide factor (9) (10) (12).
bit 4 of PLL output divide factor (9) (10) (12).
bit 0 of PLL input divide factor (10) (12).
bit 1 of PLL input divide factor (10) (12).
bit 2 of PLL input divide factor (10) (12).
bit 3 of PLL input divide factor (10) (12).
bit 4 of PLL input divide factor (10) (12).
Not used.

Table 47. pllreg2 register

pllreg2	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	1	1	1	0	1	0	0	1
bit name	ODF3	ODF1	ODF0	MF6	MF5	MF4	MF3	MF2
access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

(9) ODF value equal to zero is ignored, one is then used.

bit 2 of PLL multiplication factor (10) (11) (12).
bit 3 of PLL multiplication factor (10) (11) (12).
bit 4 of PLL multiplication factor (10) (11) (12).
bit 5 of PLL multiplication factor (10) (11) (12).
bit 6 of PLL multiplication factor (10) (11) (12).
bit 0 of PLL output divide factor (9) (10) (12).
bit 1 of PLL output divide factor (9) (10) (12).
bit 2 of PLL output divide factor (9) (10) (12).

Table 48. pllreg1 register

pllreg1	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	1	1	0	0	0	0	1	0
bit name	MF1	MF0	FRA13	FRA12	FRA11	FRA10	FRA9	FRA8
access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

bit 8 of fractional factor (10) (12).
bit 9 of fractional factor (10) (12).
bit 10 of fractional factor (10) (12).
bit 11 of fractional factor (10) (12).
bit 12 of fractional factor (10) (12).
bit 13 of fractional factor (10) (12).
bit 0 of PLL multiplication factor (10) (11) (12).
bit 1 of PLL multiplication factor (10) (11) (12).

(10) Reset values are designed for 10.25 MHz XTI input frequency.

(11) MF values smaller than 9 are ignored, 9 is then used internally.

Table 49. pllreg0 register

pllreg0	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
reset value	1	0	0	0	0	0	0	0
bit name	FRA7	FRA6	FRA5	FRA4	FRA3	FRA2	FRA1	FRA0
access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

bit 0 of fractional factor (10).
bit 1 of fractional factor (10).
bit 2 of fractional factor (10)
bit 3 of fractional factor (10).
bit 4 of fractional factor (10).
bit 5 of fractional factor (10).
bit 6 of fractional factor (10).
bit 7 of fractional factor (10).

(12) The registers pllreg3, pllreg2 and pllreg1 must be written at once to be updated, i.e. if the I2C/SPI stops after pllreg2, then these registers are not updated.

Note: sinc4reg and testreg registers are dedicated for testing and are not described in this specification.

Reset values of rds_qu, rds_corrp, rds_bd_h and rds_bd_l registers are not visible for the programmer, because he can see only the copy of this registers in the RAM buffer after a new RDS block was received.

The pllreg4-0 registers must be initialized first, before the RDS functionality can be used. If the “PLLEN” bit of pllreg4 is set from zero to one, then the PLL will be initialized after I^2C/SPI transfer with the actual values of pllreg4-0. After the lock time the PLL switches automatically over to the PLL output clock. The next I^2C/SPI transfer is only allowed after the lock time (500µs) and additional 25 XTI input clock cycles. If the “PLLEN” bit is set from one to zero, the PLL will be stopped and the system clock is switched back to the XTI input clock (after the I^2C/SPI transfer). The next I^2C/SPI transfer is then only allowed after 25 XTI input clock cycles. This is to avoid any I^2C/SPI communication during clock switching.

The registers pllreg3-1 can be only changed at once. If there are less then all three pllreg3-1 registers written during a I^2C/SPI transfer, then they will be not updated.

If the XTI input frequency is 10.25MHz, then only register pllreg4 must be programmed, because the pllreg3-0 register reset values can be used without any modification.

6.3.2 I²C transfer mode

This interface consists of three lines: a serial data line (SDA), a bit clock (SCL), and a slave address select (SA).

The interface is capable of operating up to 400kbits/s. If during the setup the system clock fsys is smaller then 8.55MHz, then the max. I²C speed decreases linear (e.i. if fsys = 4.275MHz then the maximum I²C speed is 200 kbits/s for setup).

Data transfers follow the format shown in After the START condition (S), a slave address is sent. The address is 7 bits long followed by an eighth bit which is a data direction bit (R/_W).

A zero indicates a transmission (WRITE), a one indicates a request for data (READ).

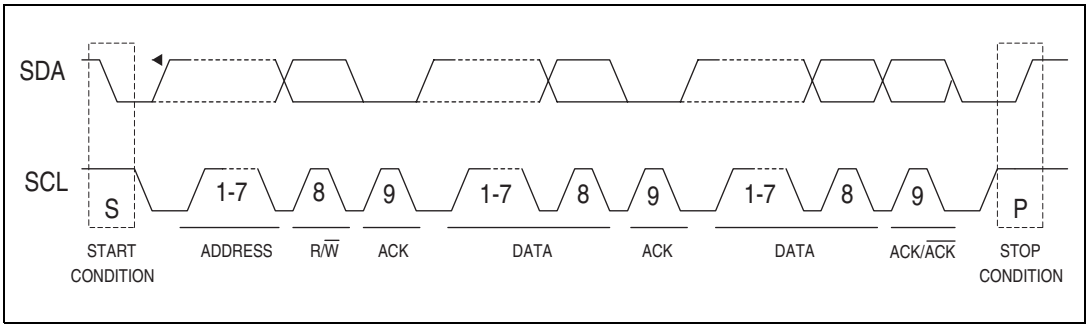
The slave address of the chip is set to 001000S, where S is the least significant bit of the slave address set externally via the pin SA_DATAOUT. This allows to choose between two addresses in case of conflict with another device of the radio set.

Each byte has to be followed by an acknowledge bit (SDA low).

Data is transferred with the most significant (MSB) bit first.

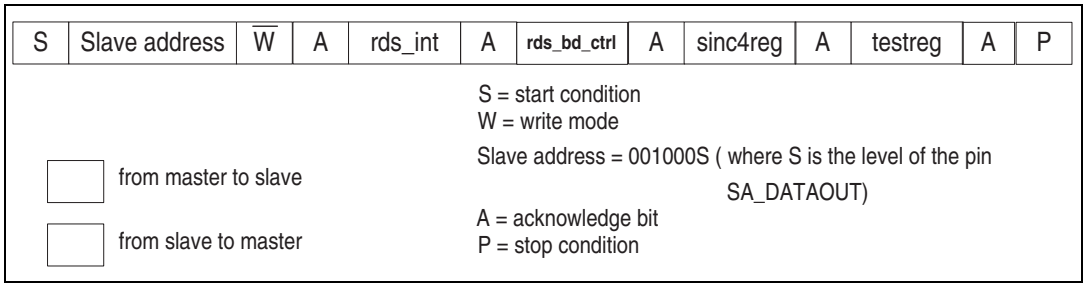
A data transfer is always terminated by a stop condition (P) generated by the master.

Figure 12. I²C data transfer



Write transfer

Figure 13. I²C write transfer



9 registers are available with write access (please refer to the relevant sections for the meaning of each bit).

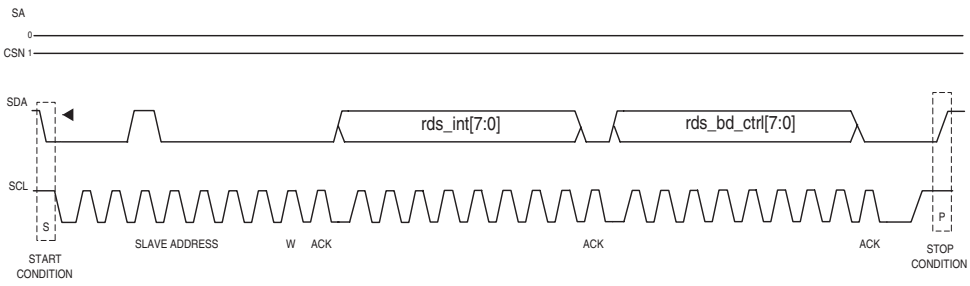
To write registers, the external master must initiate the write transfer as described above, then send the data to be written, and terminate the transfer by generating a stop condition. The transfer can be terminated after having written one, two, three, four (*Figure 13*), or five bytes.

The registers are written in the following order:

rds_int[7:0], rds_bd_ctrl[7:0], sinc4reg[7:0], testreg[7:0], pllreg4[7:0], pllreg3[7:0], pllreg2[7:0], pllreg1[7:0], pllreg0[7:0].

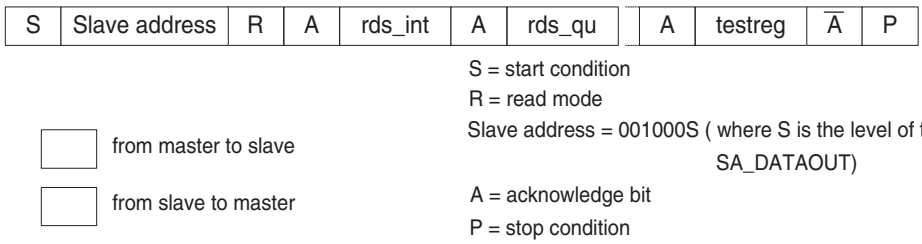
sinc4reg[7:0] and testreg[7:0] are dedicated for test and have to keep zero filled for application.

Figure 14. I²C write operation example: write of rds_int and rds_bd_ctrl registers



Read transfer

Figure 15. I²C read transfer



13 bytes can be read at a time (please refer to the to the relevant sectionsfor the meaning of each bit).

The master has the possibility to read less than 13 registers by not sending the acknowledge bit and then generating a stop condition after having read the needed amount of registers.

There are two typical read access:

- read only the first register rds_int to check the interrupt bit.
- read the first five registers rds_int, rds_qu, rds_corrp, rds_bd_h and rds_bd_l to get the RDS data.

The registers are read in the following order:

rds_int[7:0], rds_qu[7:0], rds_corrp[7:0], rds_bd_h[7:0], rds_bd_l[7:0], rds_bd_ctrl[7:0], sinc4reg[7:0], testreg[7:0], pllreg4[7:0], pllreg3[7:0], pllreg2[7:0], pllreg1[7:0], pllreg0[7:0].

Only the “bne” flag can be used for polling mode. There are two different ways to use this mode, while the first one causes less bus traffic than the second:

1. Read only the first register rds_int to check the “bne” bit.
   If “bne” bit is not set, the stop condition can be set, as shown in (*Figure 17*).

If “bne” bit is set, the transfer must be continued by the I²C master, until at least the four register rds_qu, rds_corrp, rds_bd_h and rds_bd_l are read out, then the I²C master is allowed to set the stop condition (*Figure 16*). Then the whole Buffer must be read out, by reading each time at least the five registers rds_int, rds_qu, rds_corrp, rds_bd_h and rds_bd_l without interruption. This must be done until the “bne” bit is set to zero (last RDS block).

2. If the I²C master is not able to handle the above protocol, it must read always at least the first five registers rds_int, rds_qu, rds_corrp, rds_bd_h, rds_bd_l out independent if “bne” is set or not (*Figure 16*). If the “bne” flag is set the whole RAM buffer must be read out, by reading each time at least the five registers rds_int, rds_qu, rds_corrp, rds_bd_h and rds_bd_l without interruption. This must be done until the “bne” bit is set to zero (last RDS block).

Note: In polling mode the interrupt flag “int” is just a indication that the wanted information is stored within the RAM Buffer.

Note: In polling mode it is possible that the last RDS data (rds_qu, rds_corrp, rds_bd_h and rds_bd_l), which was read out as the “bne” flag was set to zero, is identical to the RDS data before. This must be checked by the external micro controller by comparing the last received 2 RDS blocks. If they are identical, one of them can be skipped. (This is the case if just one RDS block is stored in the RAM buffer).

Figure 16. I²C read access example 1: read of 5 bytes

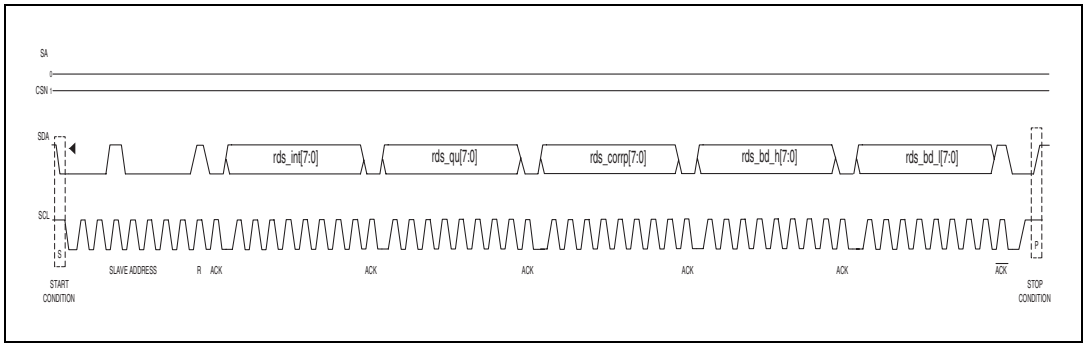
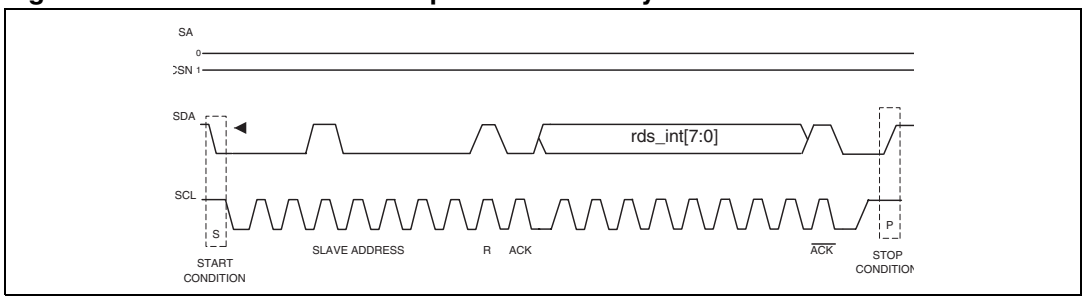
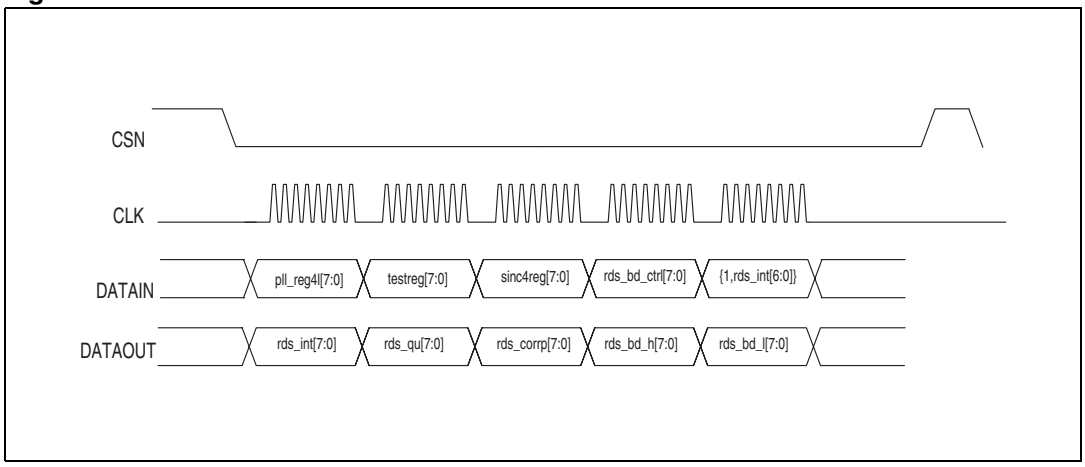


Figure 17. I²C read access example 2: read of 1 byte



6.3.3 SPI mode

Figure 18. SPI data transfer



This interface consists of four lines (*Figure 18*). A serial data input (DATAIN), a serial data output (DATAOUT), a chip select input (CSN) and a bit clock input (CLK).

The interface is capable of operating up to 1 MHz. If during the setup the system clock fsys is smaller then 8.55 MHz, then the max. SPI speed decreases linear (e.i. if fsys = 4.275 MHz then the maximum SPI speed is 500KHz for setup).

CSN starts and stops the data transfer. After starting data transfer, one bit is shifted out (DATAOUT) with the active bit clock edge (CLK) and at the same time one bit in (DATAIN). When CSN stops the data transfer, the pllreg0[7:0], pllreg1[7:0] pllreg2[7:0], pllreg3[7:0], pllreg4[7:0], rdstest[7:0], sinc4reg[7:0], rds_bd_ctrl[7:0], rds_int[7:0] registers can be updated with the last bytes which have been shifted in.

The last byte shifted in on DATAIN must be always rds_int[7:0] and the last but one is rds_bd_ctrl[7:0], and so on, as listed above. In other words, the master has take into account the number of bytes to transfer before starting, to be sure that the last byte shifted in at DATAIN is rds_int[7:0].

If the pllreg0[7:0], pllreg1[7:0] pllreg2[7:0], pllreg3[7:0], pllreg4[7:0], rdstest[7:0], sinc4reg[7:0], rds_bd_ctrl[7:0], rds_int[7:0] registers will be updated depends on the MSB of rds_int. If rds_int[7] = 1 all registers listed above are updated (refer to page 48). The registers pllreg3-1 are only updated if they are shifted completely into the SPI.

sinc4reg[7:0] and testreg[7:0] are dedicated for test **and have to be kept zero filled** in the application, independent if rds_int[7] bit is set or not.

Only the “bne” flag can be used for polling mode. There are two different ways to use **polling mode**, while the first one causes less bus traffic than the second:

1. Read only the first register rds_int to check the “bne” bit.
   If “bne” bit is not set, the CSN can be set, as shown in (*Figure 21*).
   If “bne” bit is set, the transfer must be continued by the SPI master, until at least the four register rds_qu, rds_corrp, rds_bd_h and rds_bd_l are read out, then the SPI master is allowed to stop the transfer by pulling CSN up. Then the whole Buffer must be read out, by reading each time at least the five registers rds_int, rds_qu, rds_corrp,

rds_bd_h and rds_bd_l without interruption. This must be done until the “bne” bit is set to zero (last RDS block).

2. If the SPI master is not able to handle the above protocol, it must read always at least the first five registers rds_int, rds_qu, rds_corrp, rds_bd_h, rds_bd_l out independent if “bne” is set or not. If the “bne” flag is set the whole RAM Buffer must be read out, by reading each time at least the five registers rds_int, rds_qu, rds_corrp, rds_bd_h and rds_bd_l without interruption. This must be done until the “bne” bit is set to zero (last RDS block).

Note: In polling mode the interrupt flag “int” is just a indication that the wanted information is stored within the RAM buffer.

Note: In polling mode it is possible that the last RDS data (rds_qu, rds_corrp, rds_bd_h and rds_bd_l), which was read out as the “bne” flag was set to zero, is identical to the RDS data before. This must be checked by the external micro controller by comparing the last received 2 RDS blocks. If they are identical, one of them can be skipped (This is the case if just one RDS block is stored within the RAM buffer).

Hereafter you can find typical read/write access in SPI mode:

Figure 19. Write rds_int, rds_bd_ctrl and pll_reg4 registers in SPI mode, reading RDS data and related flags

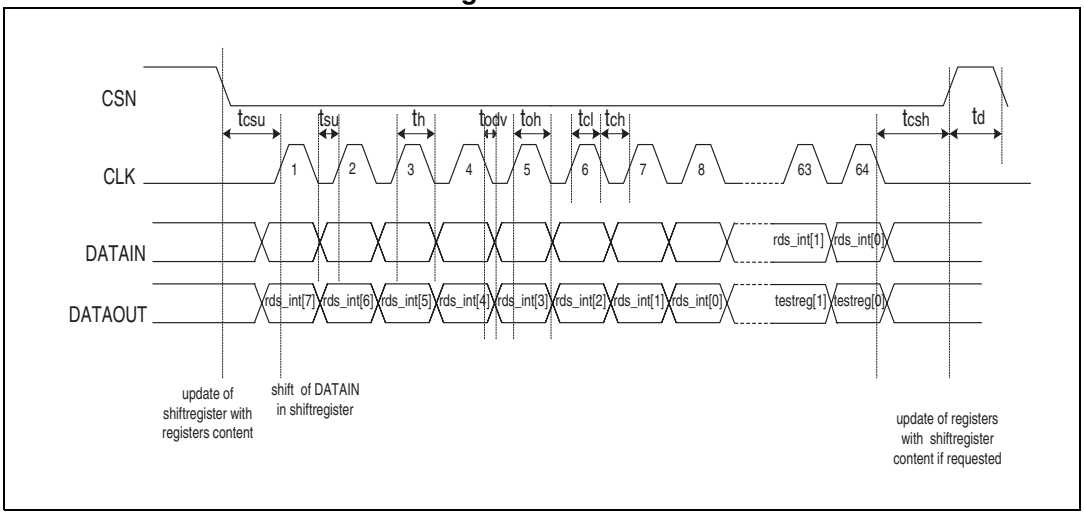
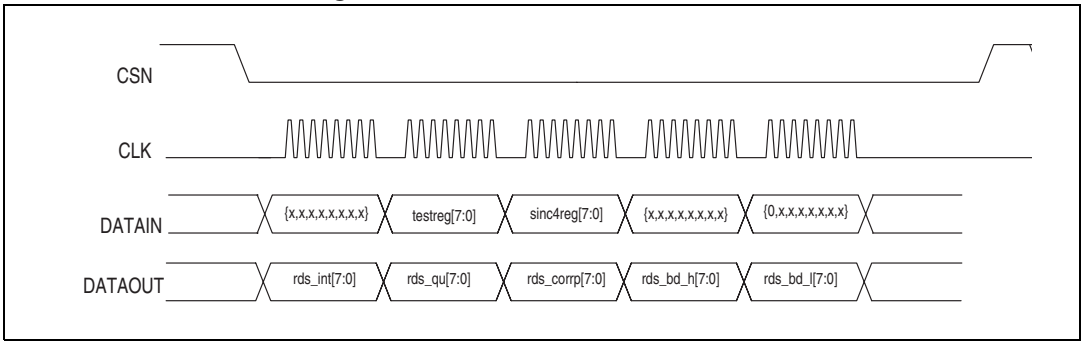
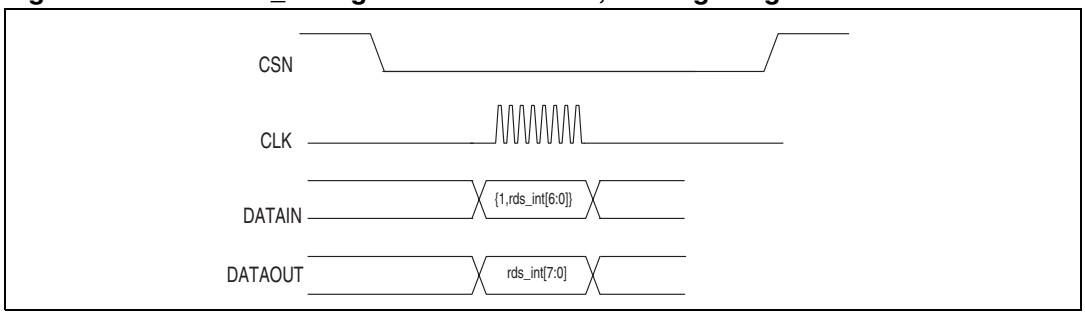


Figure 20. Read out RDS data and related flags, no update of rds_int and rds_bd_ctrl registers



Note: sinc4reg and testreg must be zero filled for application.

Figure 21. Write rds_int registers in SPI mode, reading 1 register



The content of the RDS registers is clocked out on DATAOUT pin in the following order:

rds_int[7:0], rds_qu[7:0], rds_corrp[7:0], rds_bd_l[7:0], rds_bd_h[7:0], rds_ctrl[7:0], sinc4reg[7:0], testreg[7:0], pllreg4[7:0], pllreg3[7:0], pllreg2[7:0], pllreg1[7:0], pllreg0[7:0].

For the meaning of each bit please refer to the relevant sections.

Note: After 40 bit clocks the whole RDS data and flags are clocked out.

7 Other functions detailed block diagrams

Figure 22. Block diagram I/Q mixer

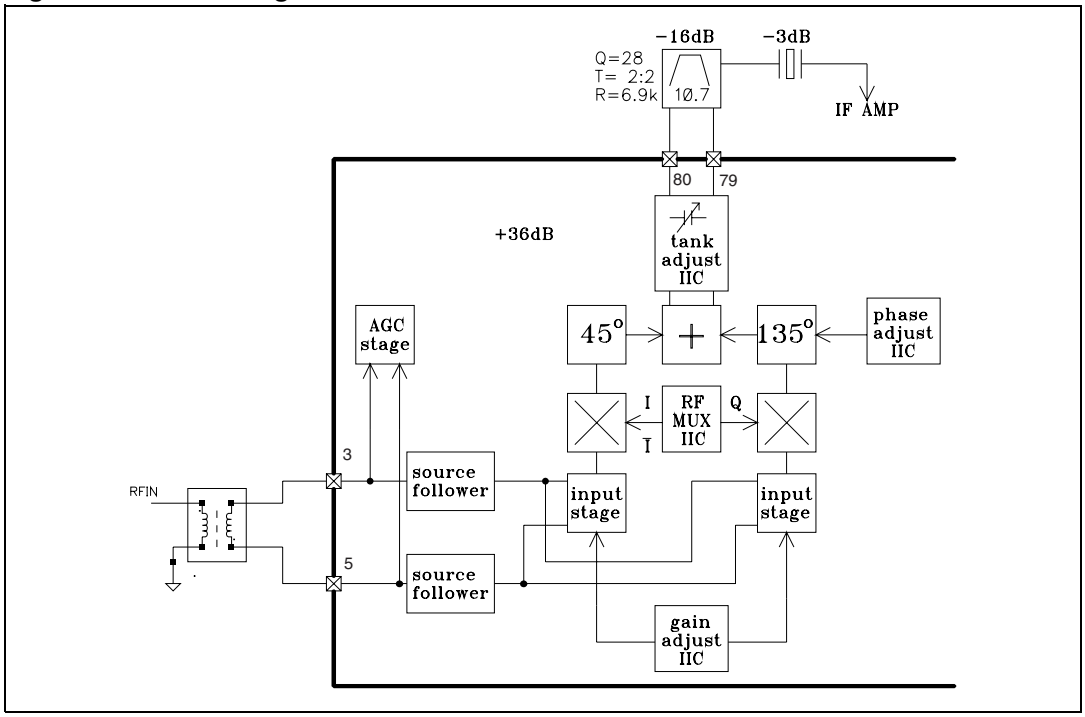


Figure 23. Block diagram VCO

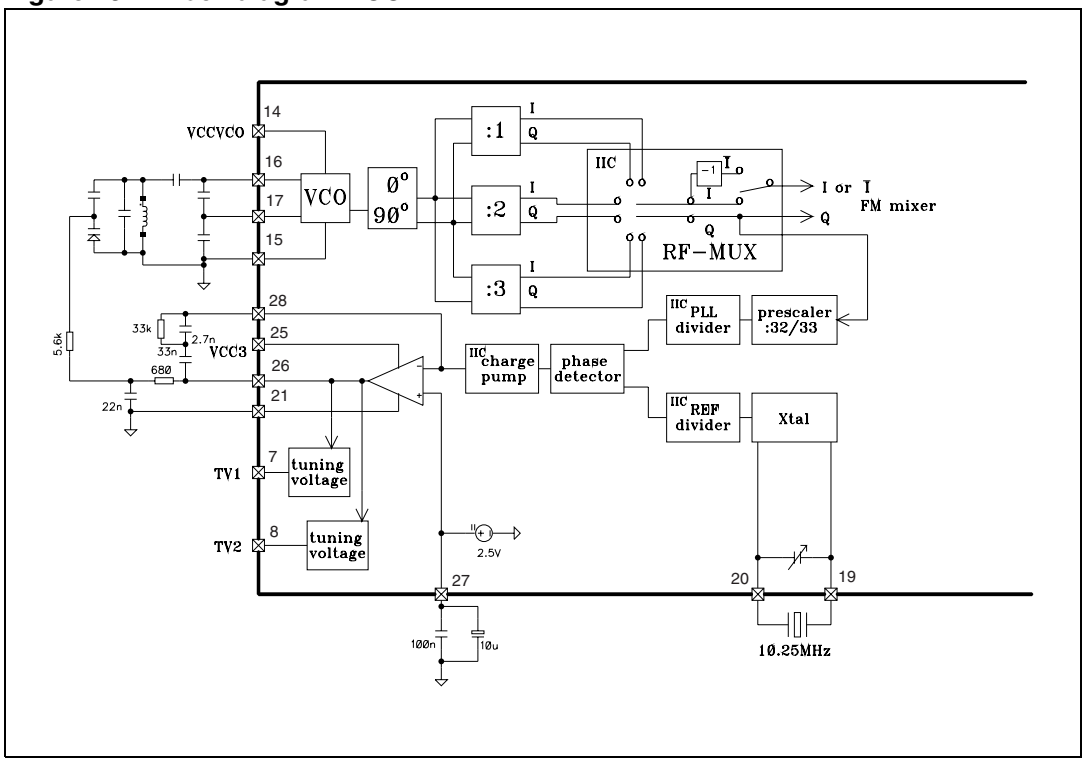


Figure 24. Block diagram keying AGC

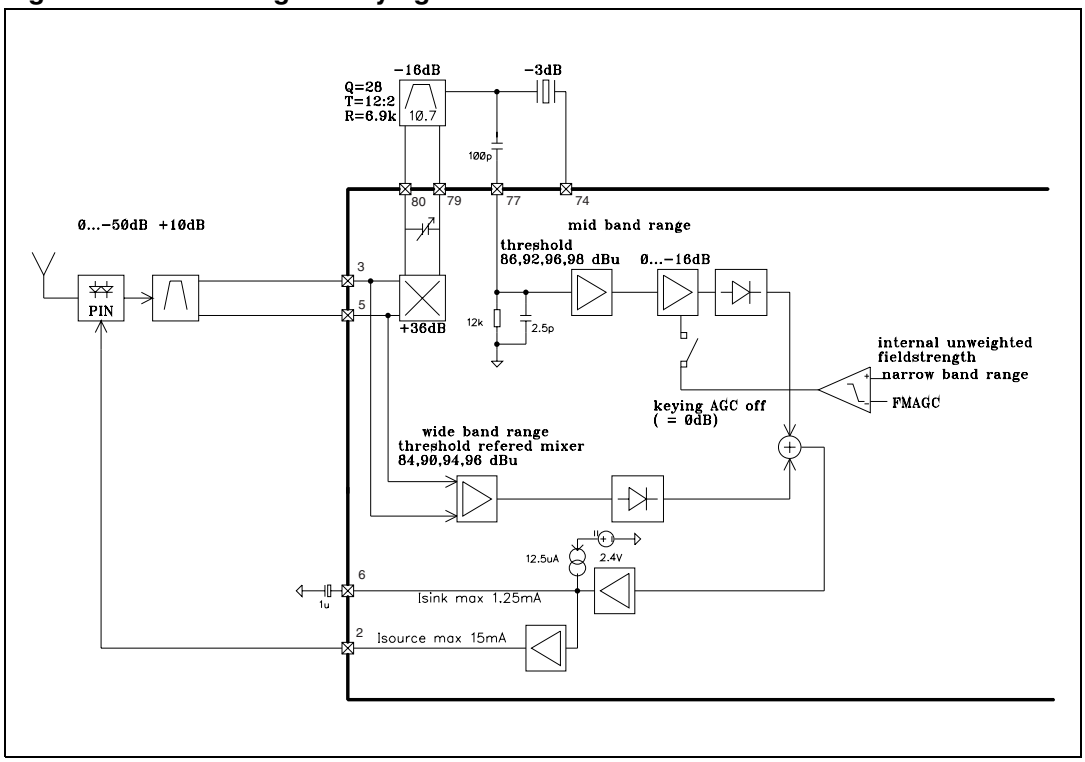


Figure 25. Block diagram ISS function

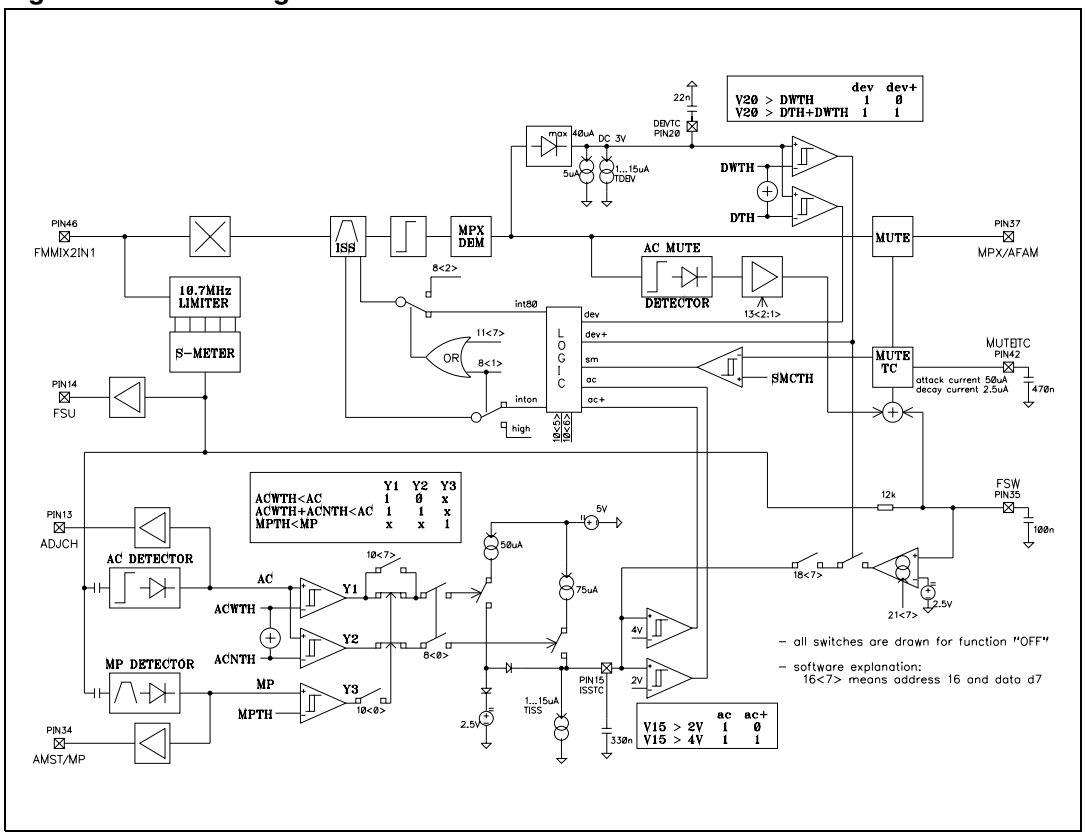


Table 50. Block diagram quality detection principle (without overdeviation correction)

Signal	LOW	HIGH
ac	No adjacent channel	Adjacent channel present
ac+	No strong adjacent channel	Adjacent channel higher as ac
sm	Fieldstrength higher as softmute threshold	Fieldstrength lower as softmute threshold
dev	Deviation lower as threshold DWTH	Deviation higher as threshold DWTH
dev+	Deviation lower as threshold DTH*DWTH	Deviation higher as threshold DTH*DWTH
inton	ISS filter off by logic (wide)	ISS filter on by logic
int80	ISS filter 120KHz (mid)	ISS filter 80KHz (narrow)

Input Signals					Mode1			Mode2		
ac	ac+	sm	dev	dev+	inton	int80	Function	inton	int80	Function
0	0	0	0	0	0	0	wide	0	0	wide
0	0	0	1	0	0	0	wide	0	0	wide
0	0	0	1	1	0	0	wide	0	0	wide
0	0	1	0	0	1	1	narrow	1	1	narrow
0	0	1	1	0	0	0	wide	1	0	mid
0	0	1	1	1	0	0	wide	0	0	wide
1	0	0	0	0	1	1	narrow	1	0	mid
1	1	0	0	0	1	1	narrow	1	1	narrow
1	0	0	1	0	1	0	mid	1	0	mid
1	1	0	1	1	1	0	mid	1	1	narrow
1	0	1	0	0	1	1	narrow	1	1	narrow
1	1	1	0	0	1	1	narrow	1	1	narrow
1	0	1	1	0	1	0	mid	1	0	mid
1	1	1	1	0	1	0	mid	1	1	narrow
1	0	1	1	1	1	0	mid	1	0	mid
1	1	1	1	1	1	0	mid	1	1	narrow

8 Application notes

8.1 Typical RDS data transfer:

1. After power up the device, the PLL must be initialized and enabled to generate the 8.55 MHz or 8.664 MHz system clock (fsys). If the XTI frequency is already 8.55 MHz or 8.664 MHz, this point can be skipped. If not, the pllreg4-0 register must be programmed via I^2C/SPI. If the XTI frequency is smaller then 8.55 MHz, the reduced maximum I^2C/SPI speed must be considered. After the pllreg4-0 register has been programmed, 500 us and additional 25 XTI input clock cycles must be waited until the PLL is locked and the system clock fsys is switched over to the PLL output clock. Then the next I^2C/SPI transfer is allowed with its maximum speed specified for the 8.55/8.664 MHz system clock (fsys).
2. In the next I^2C/SPI transfer the interrupt source will be set to “buffer not empty” (itsrc[2:0] = 001) and a resynchronization should be forced (rds_int[5] = 1), to be sure that the buffer is empty and not filled with spurious RDS data. To do this only an write access to the first register rds_int is needed.
3. Now the pin INTN must be continuously checked for an interrupt (active low). If there is an interrupt the five registers rds_int, rds_qu, rds_corrp, rds_bd_h and rds_bd_l must be read out to get the RDS data. The next interrupt can not be expected before 22 ms.
4. If it is not possible to service the interrupt in time, then the RDS buffer can store up to 24 RDS bocks. If the buffer is full and the data could not be read before the next RDS block, the “buffer overflow” flag (rds_corrp[0] = 1) will be set. In this case at least one RDS block is missed. The “buffer overflow” flag is only cleared, if the whole RDS buffer is read out.

If there is no pin available for checking the INTN pin, then it is possible to read out the RDS data by I^2C/SPI polling. Only the “buffer not empty” flag (rds_int[6]) can be used for that. If rds_int[6] bit is set, the I^2C/SPI transfer must be continued, until at least the four register rds_qu, rds_corrp, rds_bd_h and rds_bd_l are read out.

This must be done until rds_int[6] bit is set to zero (last RDS block). It is possible that the last RDS block is the same as the last but one RDS block. This is the case if just one RDS block was stored in the RAM buffer. If they are identical, one of them can be skipped.

If another interrupt source is used instead of “buffer not empty” for the INTN pin, also the polling mode must be used for reading out the whole RDS buffer, as described above.

9 Package information

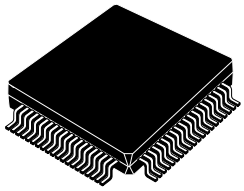
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

ECOPACK specifications are available at: www.st.com.

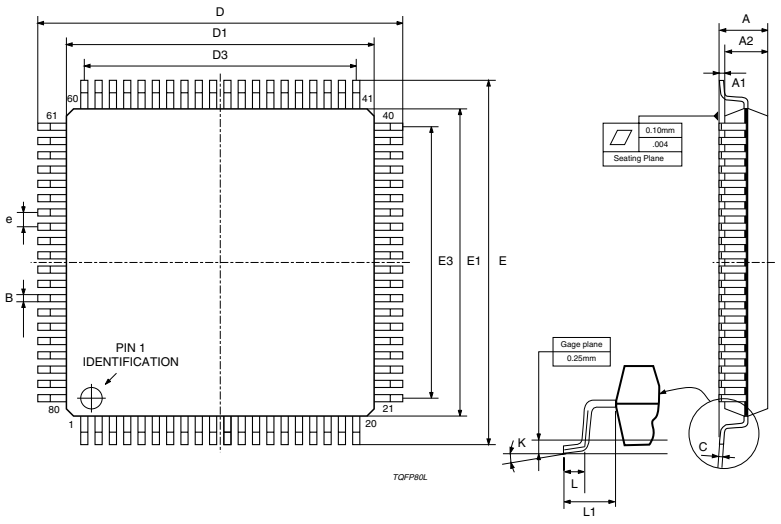
Figure 26. TQFP80LS mechanical data & package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.22	0.32	0.38	0.009	0.013	0.015
C	0.09		0.20	0.003		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.35			0.295	
e		0.65			0.0256	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.35			0.486	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.0393	
K	3.5°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



LQFP80 (14x14x1.40mm)



10 Revision history

Table 51. Document revision history

Date	Revision	Changes
02-Nov-2005	1	Initial release.
14-Nov-2005	1.1	Minor corrections.
05-Dec-2005	1.2	Updated datas in the Electrical specification chapter.
22-Dec-2005	1.3	Minimum tuner supply voltage changed to 7.7V.
13-Jan-2006	1.4	Updated datas in the Electrical specification chapter.
02-Feb-2006	1.5	Corrected *Figure 11*, *Table 48* & *49*.
08-Mar-2006	1.6	Changed Vco impedance value.
04-May-2006	2	First issue in st.com web site.
30-May-2006	3	Corrected type error in Order Codes table.
30-Oct-2006	4	Changed *Table 40*.

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