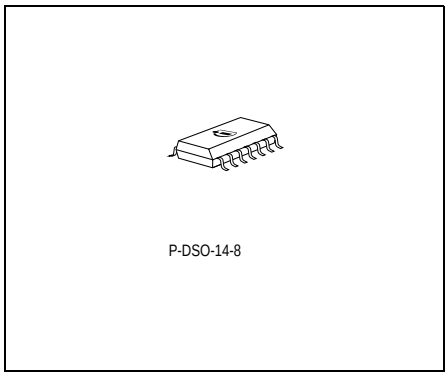
5-V Low-Drop Voltage Regulator TLE 4263

Features



- Output voltage tolerance $\leq \pm$ 2 %
- 200 mA output current capability
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Adjustable reset threshold
- Watchdog
- Wide temperature range
- Suitable for use in automotive electronics

Type	Ordering Code	Package
TLE 4263 GM	Q67006-A9357-A201K5	P-DSO-14-8

SMD type

Functional Description

TLE 4263 is a 5-V low-drop voltage regulator in a P-DSO-14-8 SMD package. The maximum input voltage is 45 V. The maximum output current is more than 200 mA. The IC is short-circuit proof and incorporates temperature protection which turns off the IC at overtemperature.

The IC regulates an input voltage V_I in the range of 6 V < V_I < 45 V to $V_{Q,nom}$ = 5.0 V. A reset signal is generated for an output voltage of $V_{Q,rt}$ < 4.5 V. This voltage threshold can be decreased to 3.5 V by external connection of a voltage divider. The reset delay can be set externally by a capacitor. The integrated watchdog logic supervises the connected microcontroller. The IC can be switched off via the inhibit input, which causes the current consumption to drop from 900 µA to typical 0 µA.

Choosing External Components

The input capacitor C_I is necessary for compensation of line influences. Using a resistor of approx. 1 Ω in series with C_I, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed at values ≥ 22 µF and an ESR of ≤ 3 Ω within the operating temperature range. For small tolerances of the reset delay the spread of the capacitance of the delay capacitor and its temperature coefficient should be noted.

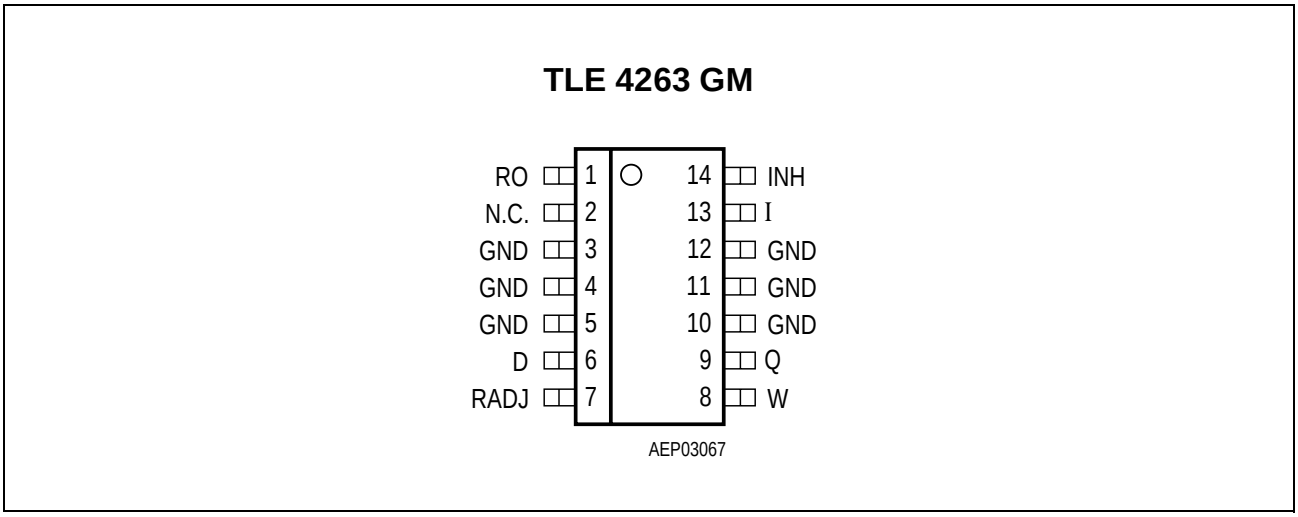


Figure 1 **Pin Configuration** (top view)

Pin Definitions and Functions

Pin (P-DSO-14-4)	Symbol	Function
1	RO	**Reset output;** open-collector output connected to the output via a resistor of 30 kΩ.
2	N.C.	Not connected
3 - 5, 10 - 12	GND	**Ground**
6	D	**Reset delay;** connected to ground with a capacitor.
7	RADJ	**Reset threshold;** to adjust the switching threshold connect a voltage divider (output to GND) to the pin. If this input is connected to GND, reset is triggered at an output voltage of 4.5 V.
8	W	**Watchdog;** rising edge triggered input for monitoring a microcontroller.
9	Q	**5-V output voltage;** block to ground with a capacitor, $C \geq 22\ \mu F$, $ESR \leq 3\ \Omega$ at
13	I	**Input voltage;** block to ground directly at the IC with a ceramic capacitor.
14	INH	**Inhibit;** TTL-compatible, low-active input.

Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35 V, the external reset delay capacitor is discharged by the reset generator. When the voltage of the capacitor reaches the lower threshold V_{DRL}, a reset signal occurs at the reset output and is held until the upper threshold V_{DU} is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of typ. 4.65 V. A connected microcontroller will be monitored through the watchdog logic. In case of missing pulses at pin W, the reset output is set to low. The pulse sequence time can be set in a wide range with the reset delay capacitor. The IC can be switched at the TTL-compatible, low-active inhibit input. The IC also incorporates a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity

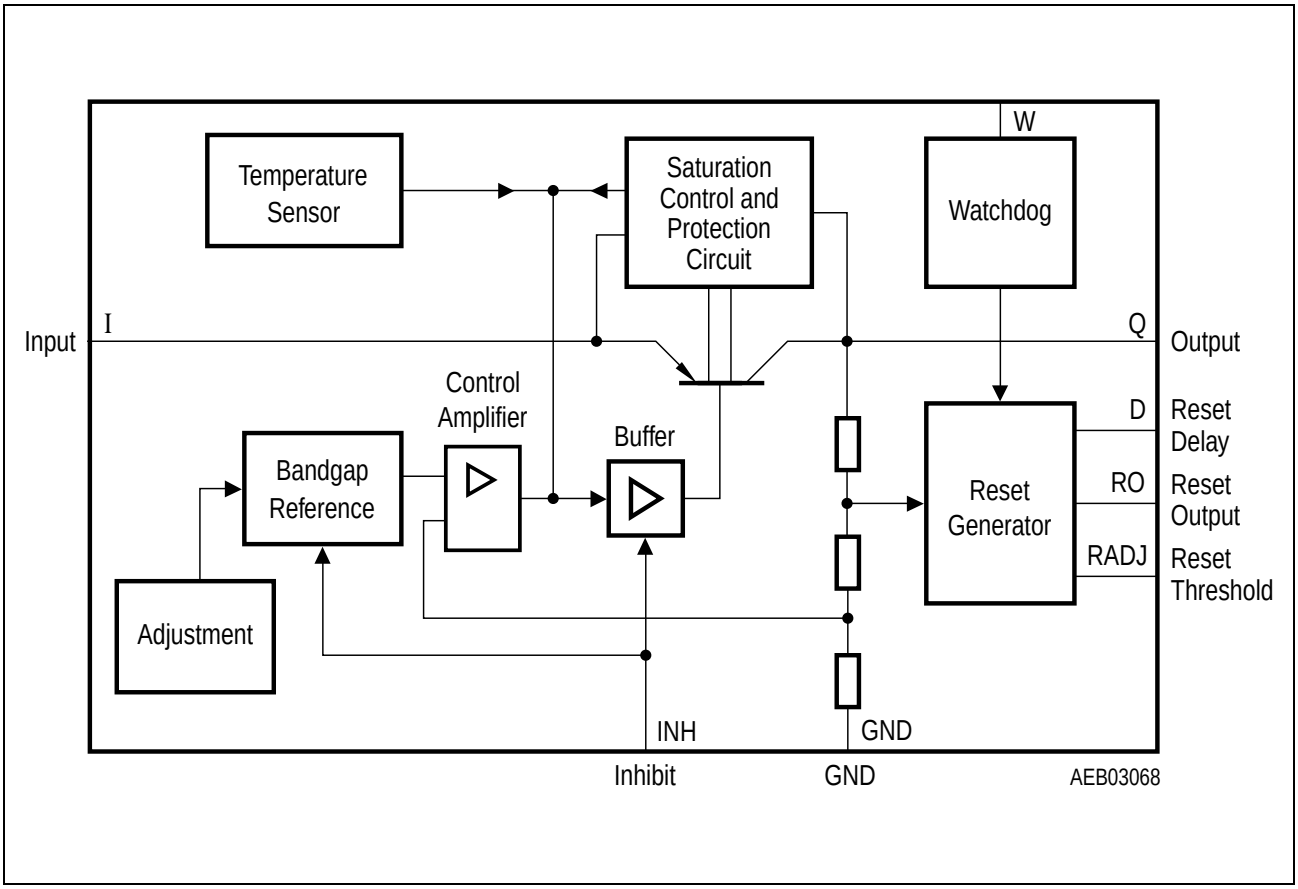


Figure 2 Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input I					
Input voltage Input current	V_I I_I	– 42 –	45 –	V –	– internally limited
Reset Output RO					
Voltage Current	V_R I_R	– 0.3 –	42 –	V –	– internally limited
Reset Threshold RADJ					
Voltage	V_{RADJ}	– 0.3	6	V	–
Reset Delay D					
Voltage Current	V_D I_D	– 0.3 –	42 –	V –	– internally limited
Output Q					
Voltage Current	V_Q I_Q	– 0.3 –	7 –	V –	– internally limited
Inhibit INH					
Voltage	V_{INH}	– 42	45	V	–
Watchdog W					
Voltage	V_W	– 0.3	6	V	–
Ground GND					
Current	I_{GND}	– 0.5	–	A	–

Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Temperature					
Junction temperature	T_j	–	150	°C	–
Storage temperature	T_{stg}	– 50	150	°C	–
Operating Range					
Input voltage	V_I	–	45	V	–
Junction temperature	T_j	– 40	150	°C	–
Thermal resistance					
junction-ambient	$R_{thj\text{-}a}$	–	112	K/W	1)
junction-pin	$R_{thj\text{-}p}$	–	32	K/W	2)

1) Package mounted on PCB 80 × 80 × 1.5mm^3; 35µ Cu; 5µ Sn; Footprint only; zero airflow.
2) Measured to pin 4.

Characteristics

V_I = 13.5 V; – 40 °C < T_j < 125 °C; V_{INH} > 3.5 V; (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Normal Operation						
Output voltage	V_Q	4.90	5.00	5.10	V	5 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_I ≤ 28 V
Output voltage	V_Q	4.90	5.00	5.10	V	6 V ≤ V_I ≤ 32 V; I_Q = 100 mA; T_j = 100 °C
Output current	I_Q	200	250	–	mA	1)
Current consumption; $I_q = I_I - I_Q$	I_q I_q I_q I_q	– – – –	0 900 10 15	50 1300 18 23	µA µA mA mA	V_{INH} = 0 I_Q = 0 mA I_Q = 150 mA I_Q = 150 mA; V_I = 4.5 V
Drop voltage	V_{dr}	–	0.35	0.50	V	I_Q = 150 mA1)
Load regulation	$\Delta V_{Q,lo}$	–	–	25	mV	I_Q = 5 mA to 150 mA
Line regulation	$\Delta V_{Q.li}$	–	3	25	mV	V_I = 6 V to 28 V; I_Q = 150 mA
Power Supply Ripple Rejection	PSRR	–	54	–	dB	f_r = 100 Hz; V_r = 0.5 V_{PP}
Reset Generator						
Switching threshold	$V_{Q,rt}$	4.5	4.65	4.8	V	V_{RADJ} = 0 V
Reset adjust threshold	$V_{RADJ,th}$	1.26	1.35	1.44	V	V_Q > 3.5 V
Reset low voltage	$V_{RO,I}$	–	0.10	0.40	V	I_{RO} = 1 mA

Note: The reset output is low within the range V_Q = 1 V to $V_{Q,rt}$

1) Drop voltage = $V_i - V_Q$ (measured when the output voltage has dropped 100 mV from the nominal value obtained at 6 V input)

Characteristics (cont'd)

V_I = 13.5 V; – 40 °C < T_j < 125 °C; V_{INH} > 3.5 V; (unless specified otherwise)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Saturation voltage	$V_{D,sat}$	–	50	100	mV	$V_Q < V_{R,th}$
Upper timing threshold	V_{DU}	1.45	1.70	2.05	V	–
Lower reset timing threshold	V_{DRL}	0.20	0.35	0.55	V	–
Charge current	$I_{D,ch}$	40	60	85	µA	–
Reset delay time	t_{rd}	1.3	2.8	4.1	ms	C_D = 100 nF
Reset reaction time	t_{rr}	0.5	1.2	4	µs	C_D = 100 nF
Watchdog						
Discharge current	$I_{D,wd}$	4.40	6.25	9.10	µA	V_D = 1.0 V
Upper timing threshold	V_{DU}	1.45	1.70	2.05	V	–
Lower timing threshold	V_{DWL}	0.20	0.35	0.55	V	–
Watchdog trigger time	$T_{WI,tr}$	16	22.5	27	ms	C_D = 100 nF
Inhibit						
Switching voltage	$V_{INH,ON}$	3.6	–	–	V	IC turned on
Turn-OFF voltage	$V_{INH,OFF}$	–	–	0.8	V	IC turned off
Input current	I_{INH}	5	10	25	µA	V_{INH} = 5 V

Note: The reset output is low within the range V_Q = 1 V to $V_{Q,rt}$

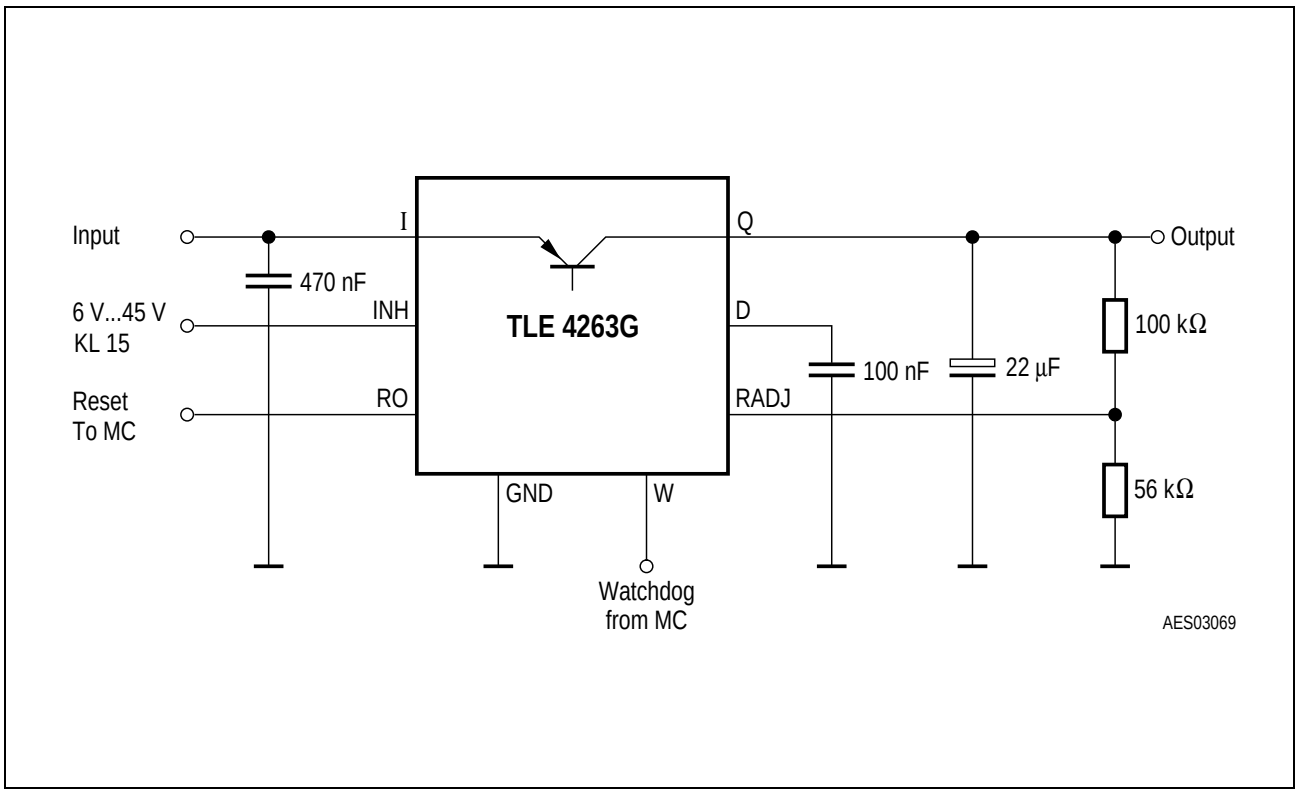


Figure 3 Application Circuit

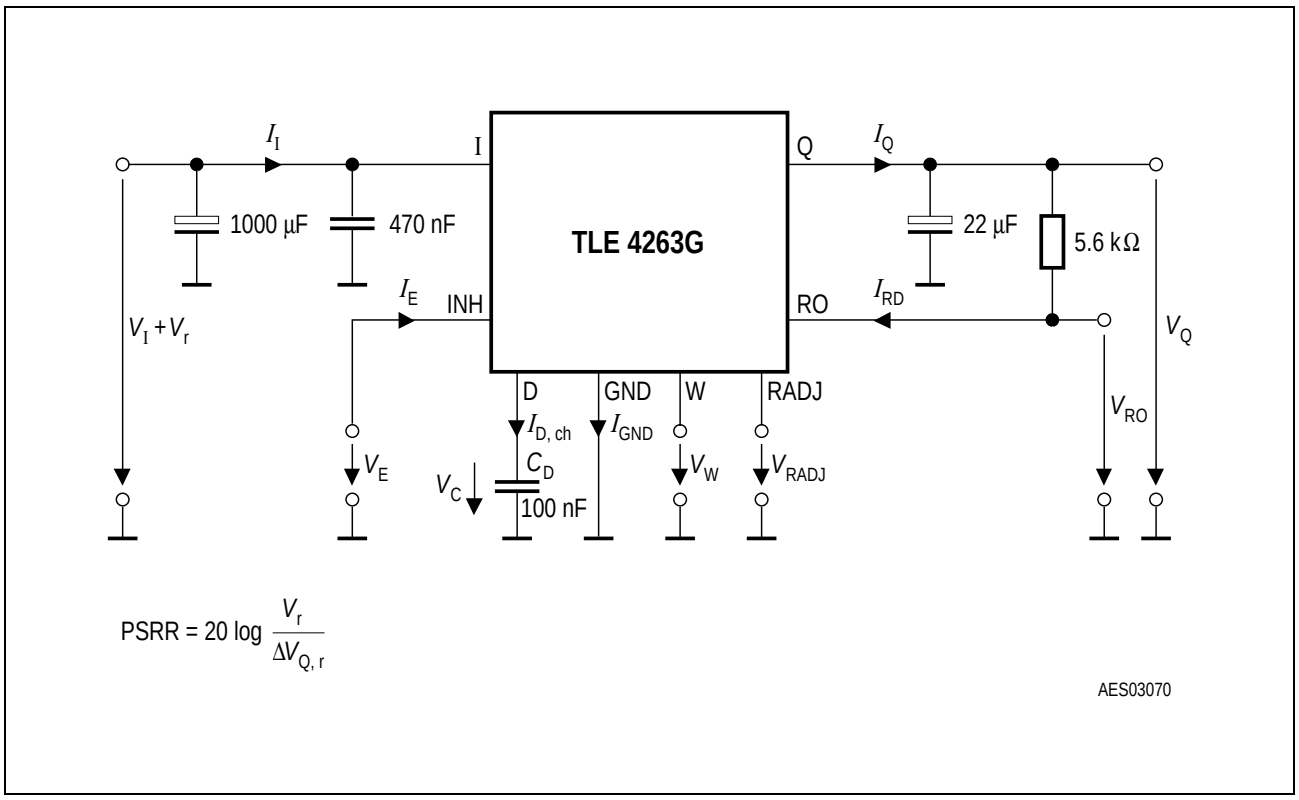


Figure 4 Test Circuit

Reset Timing

The power-on reset delay time is defined by the charging time of an external capacitor C_D which can be calculated as follows:

$$C_D = (t_{rd} \times I_{D,ch})/\Delta V$$

Definitions:

C_D = delay capacitor

t_{rd} = reset delay time

$I_{D,ch}$ = charge current, typical 60 µA

$\Delta V = V_{DU}$, typical 1.70 V

V_{DU} = upper delay switching threshold at C_D for reset delay time

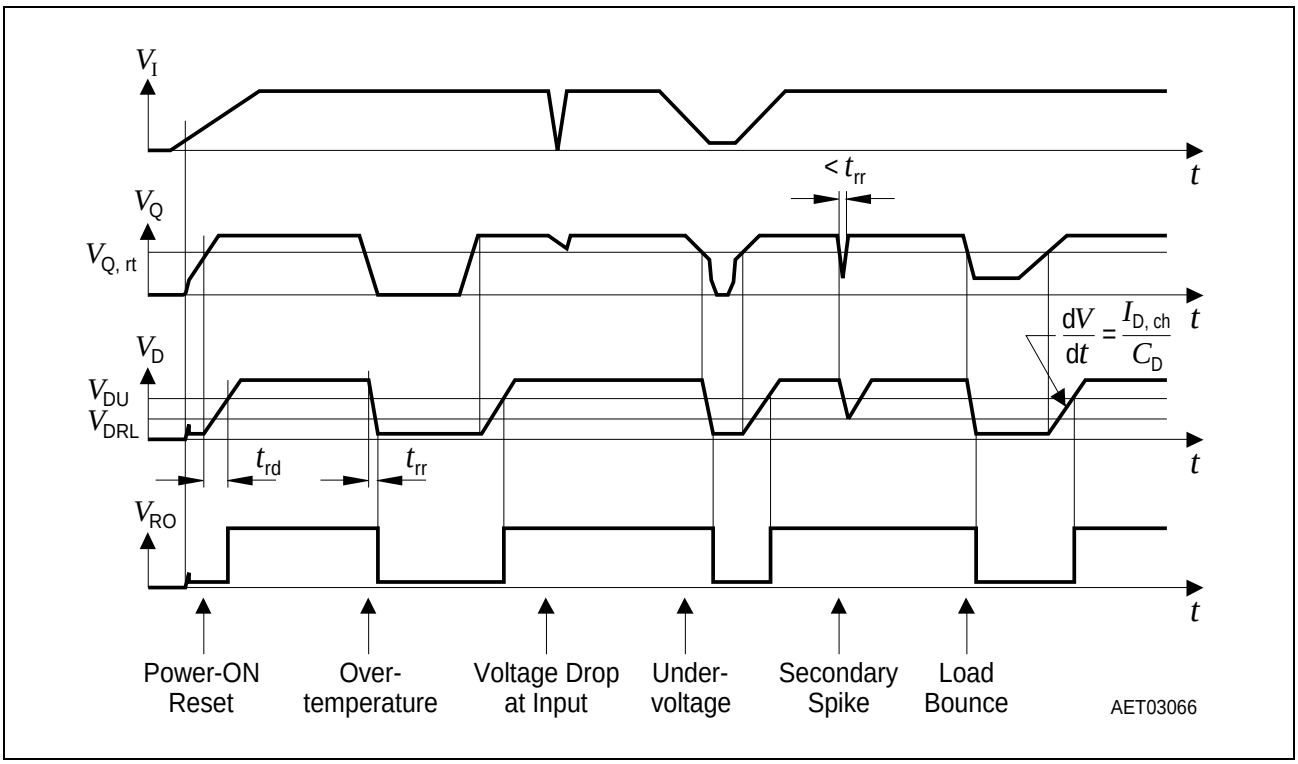


Figure 5 Time Response, Watchdog with High-Frequency Clock

Reset Switching Threshold

The present default value is typ. 4.65 V. When using the TLE 4263 the reset threshold can be set to 3.5 V < $V_{Q,rt}$ < 4.6 V by connecting an external voltage divider to pin RADJ. The calculation can be easily done since the reset adjust input current can be neglected. If this feature is not needed, the pin has to be connected to GND.

$$V_{Q, rt} = (1+R1/R2) \times V_{RADJ,th}$$

Definitions: $V_{Q,rt}$ = reset threshold

$V_{RADJ, th}$ = comparator reference voltage, typical 1.35 V

Watchdog Timing

The frequency of the watchdog pulses has to be higher than the minimum pulse sequence which is set by the external reset delay capacitor C_D. Calculation can be done according to the formulas given in **Figure 6**.

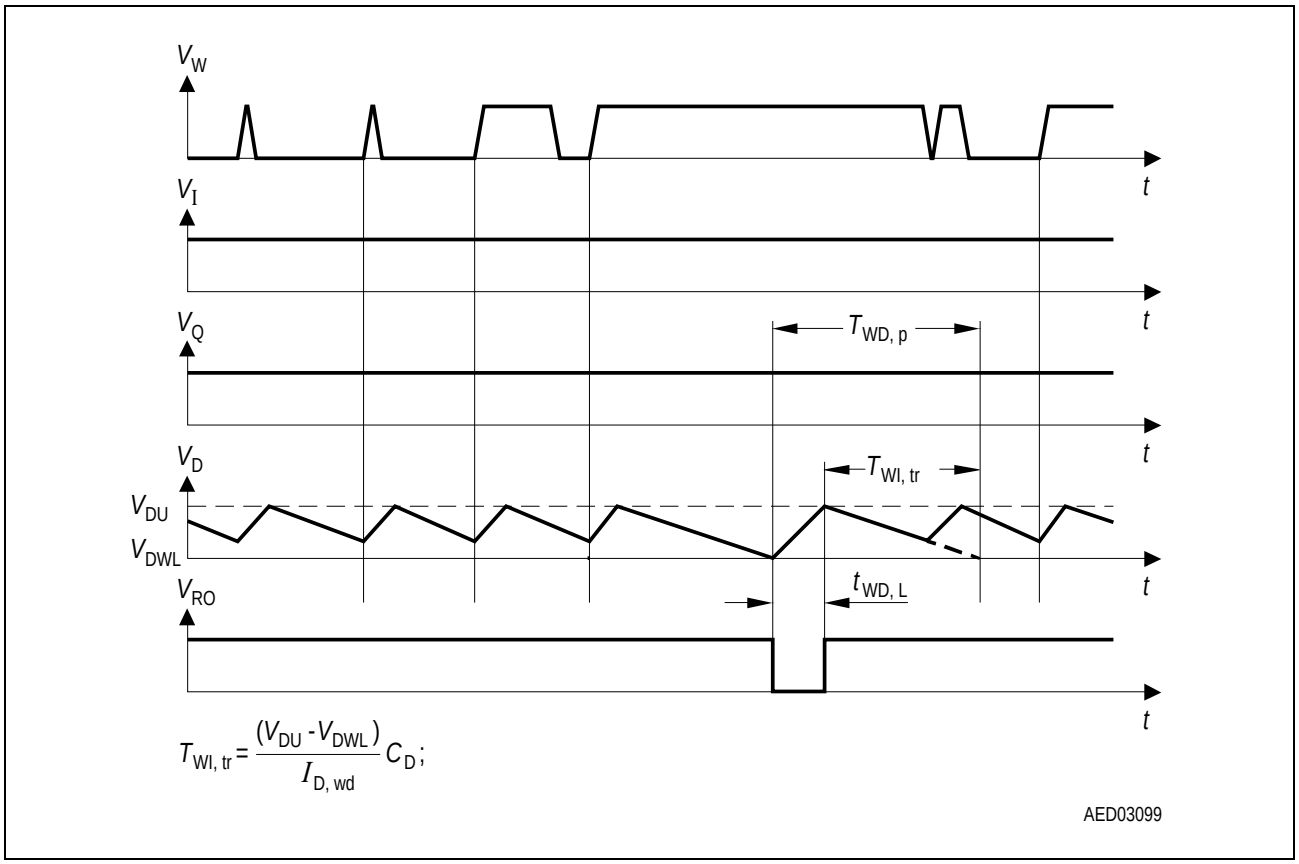
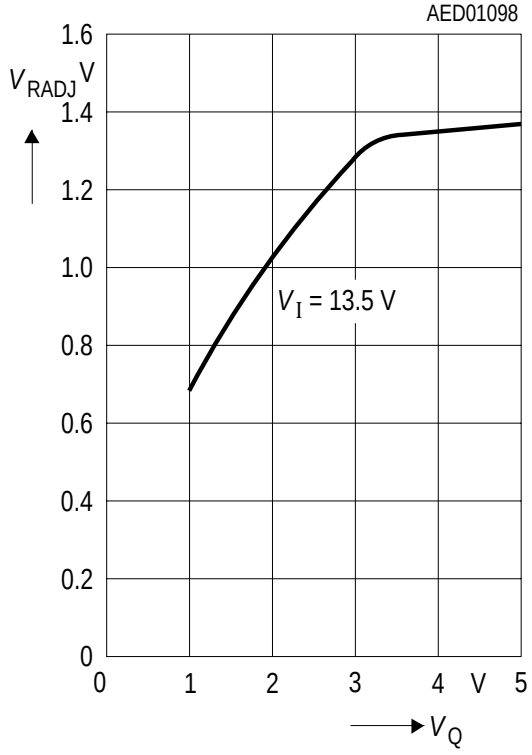
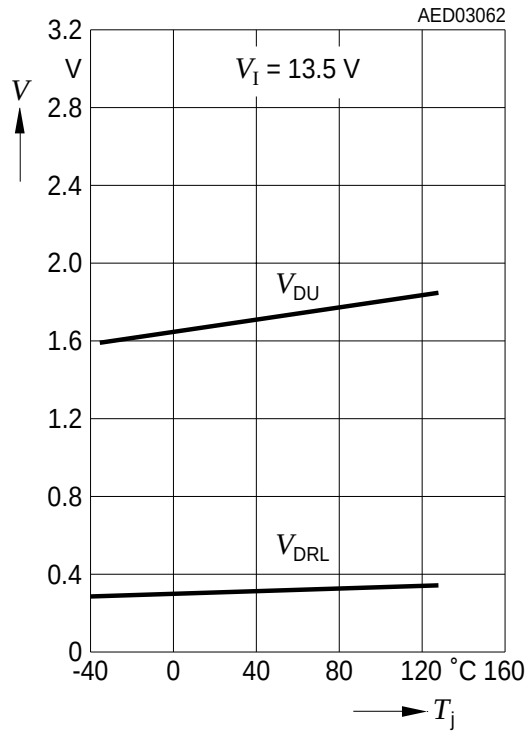


Figure 6 Timing of the Watchdog FunctionReset

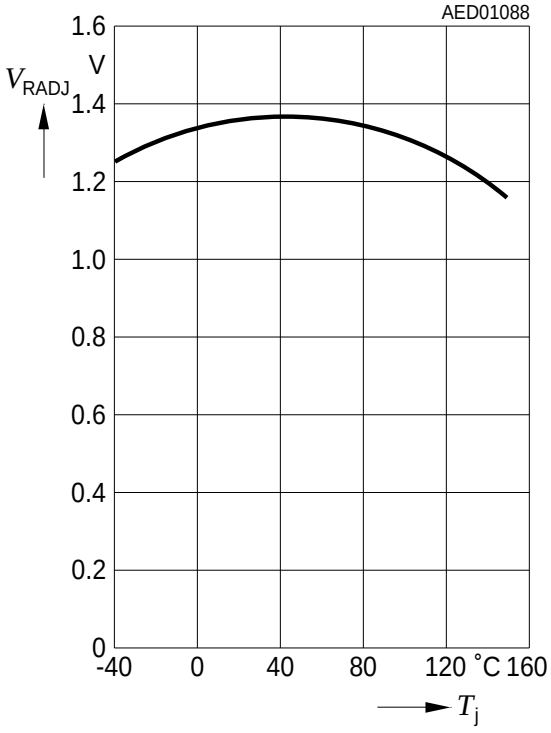
Reset Switching Threshold versus Output Voltage



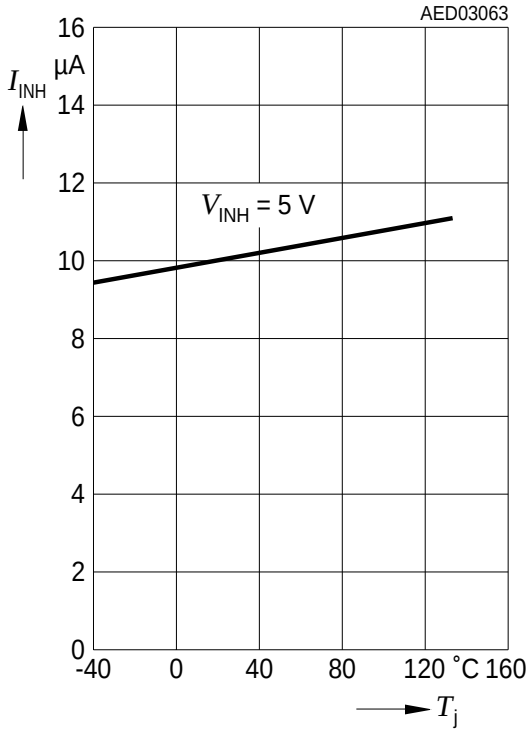
Timing Threshold Voltage V_{DU} and V_{DRL} versus Temperature



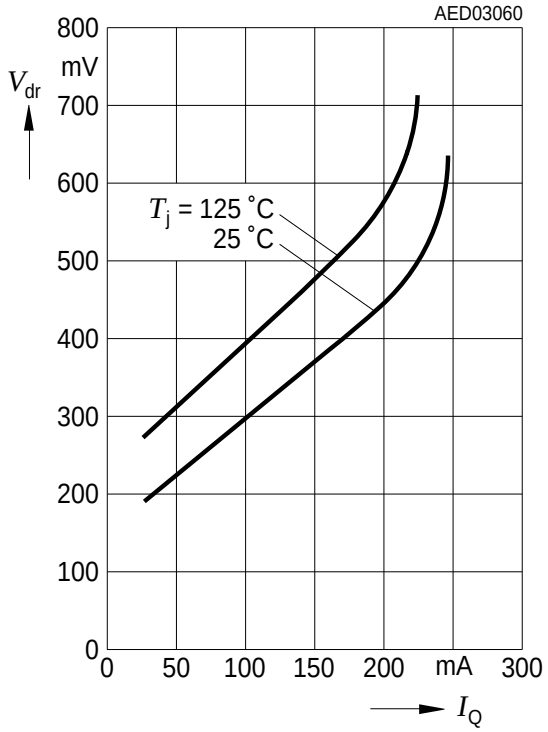
Reset Switching Threshold versus Temperature



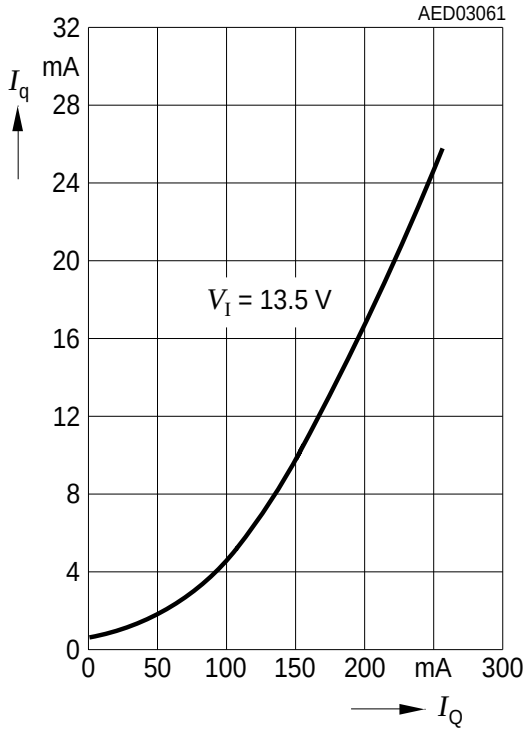
Current Consumption of Inhibit versus Temperature



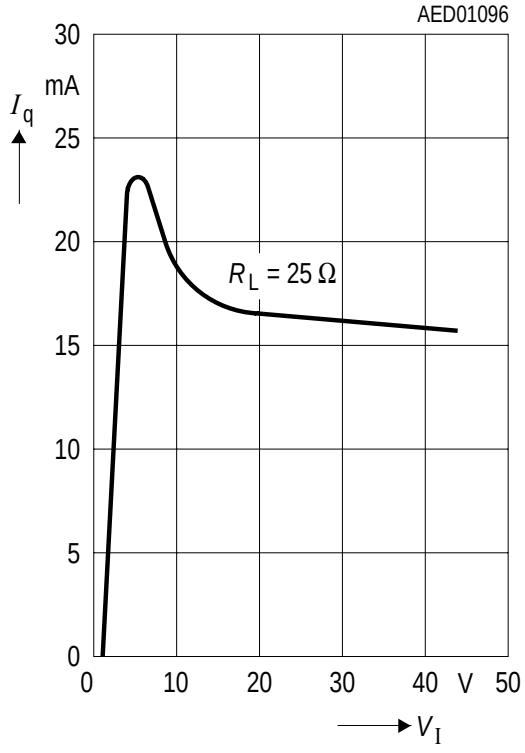
Drop Voltage versus OutputCurrent



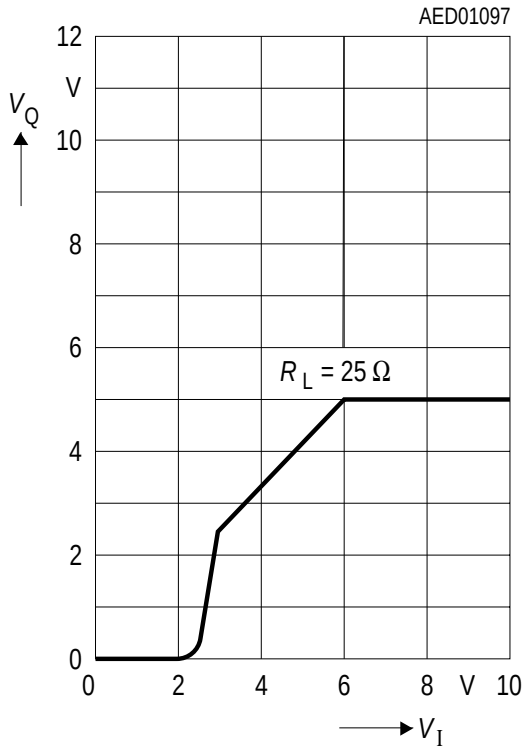
Current Consumption versus Output Current



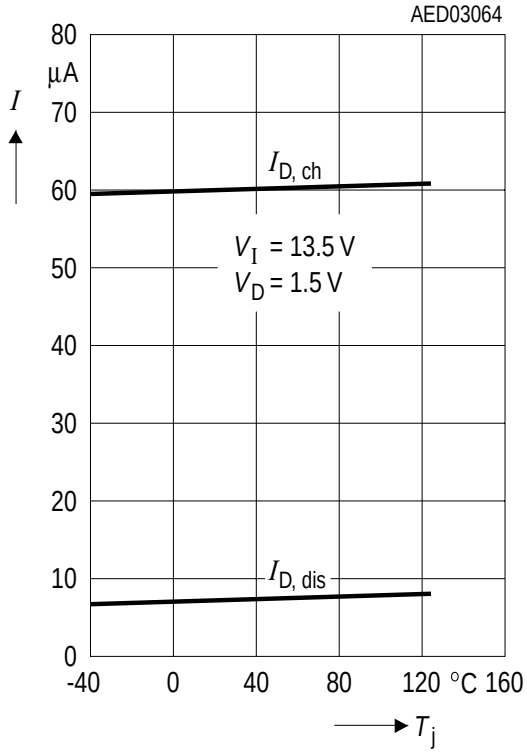
Current Consumption versus Input Voltage



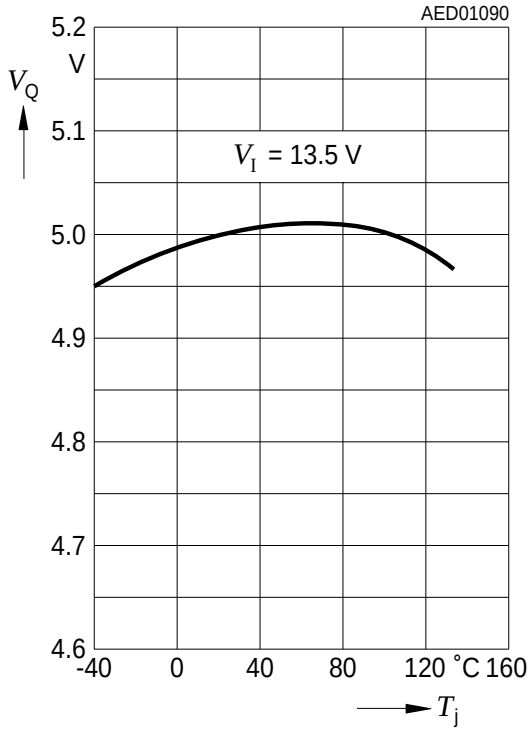
Output Voltage versus Input Voltage



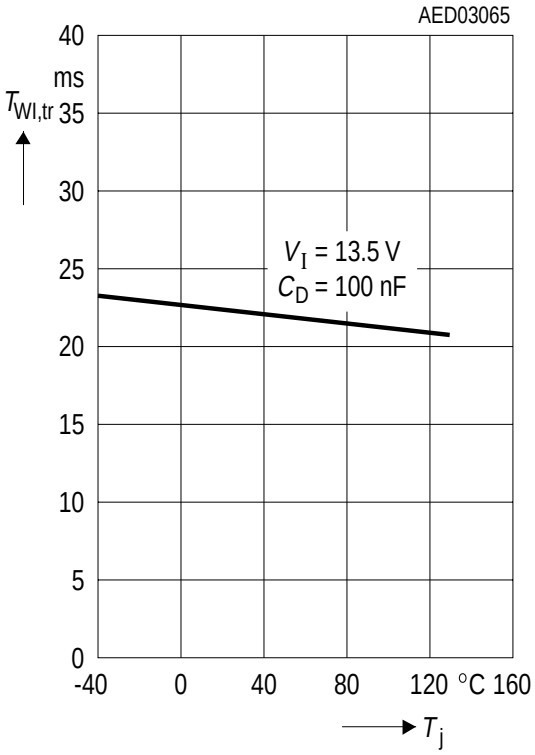
Charge Current and Discharge Current versus Temperature



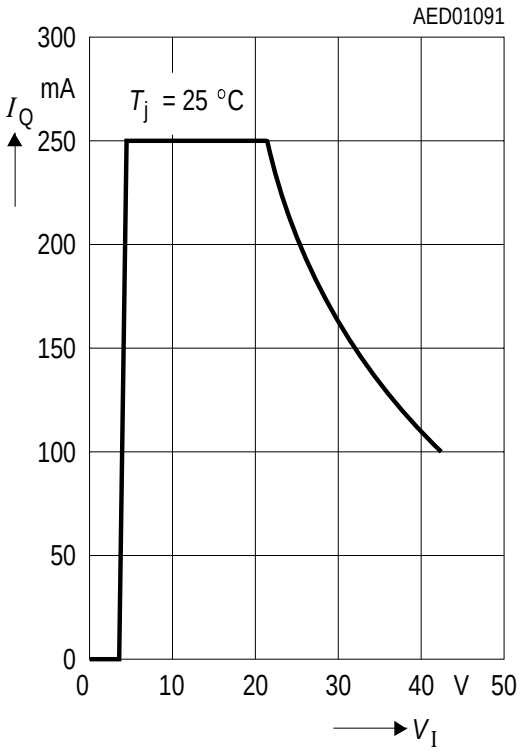
Output Voltage versus Temperature



Pulse Time versus Temperature

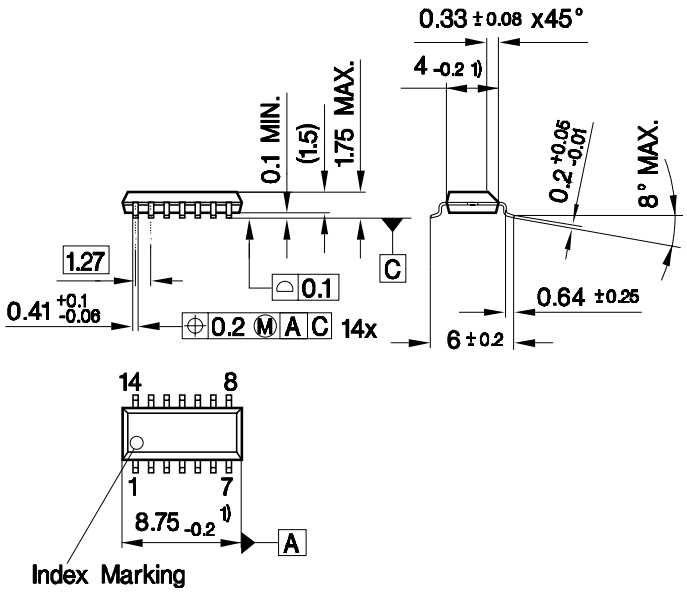


Output Current versus Input Voltage



Package Outlines

P-DSO-14-8
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS09222

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Edition 2001-01-17

**Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
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