

AsahiKASEI

ASAHI KASEI EMD

AK4673**Stereo CODEC with MIC/HP-AMP and Touch Screen Controller****GENERAL DESCRIPTION**

The AK4673 is a stereo CODEC with a built-in Microphone-Amplifier, Headphone-Amplifier and Touch Screen Controller (TSC) which includes the SAR type ADC. The AK4673 features analog mixing circuits, PLL and a 4-wire resistive touch screen I/F that allows easy interfacing in mobile phone and portable A/V player designs. The AK4673 is available in a 57pin BGA package, utilizing less board space than competitive offerings.

FEATURES**1. Recording Function**

- 4 Stereo Input Selectors
- Stereo Mic Input (Full-differential or Single-ended)
- Stereo Line Input
- MIC Amplifier (+32dB/+26dB/+20dB or 0dB)
- Digital ALC (Automatic Level Control)
 - (+36dB ~ -54dB, 0.375dB Step, Mute)
- ADC Performance: S/(N+D): 83dB DR, S/N: 86dB (MIC-Amp=+20dB)
S/(N+D): 88dB DR, S/N: 95dB (MIC-Amp=0dB)
- Wind-noise Reduction Filter
- Stereo Separation Emphasis
- Programmable EQ

2. Playback Function

- Digital De-emphasis Filter (tc=50/15 μ s, fs=32kHz, 44.1kHz, 48kHz)
- Bass Boost
- Soft Mute
- Digital Volume (+12dB ~ -115.0dB, 0.5dB Step, Mute)
- Digital ALC (Automatic Level Control)
 - (+36dB ~ -54dB, 0.375dB Step, Mute)
- Stereo Separation Emphasis
- Programmable EQ
- Stereo Line Output
 - Performance: S/(N+D): 88dB, S/N: 92dB
- Stereo Headphone-Amp
 - S/(N+D): 70dB@7.5mW, S/N: 90dB
 - Output Power: 70mW@16 Ω (HVDD=5V), 62mW@16 Ω (HVDD=3.3V)
 - Pop Noise Free at Power ON/OFF
- Analog Mixing: 4 Stereo Input

3. Power Management**4. Master Clock:****(1) PLL Mode**

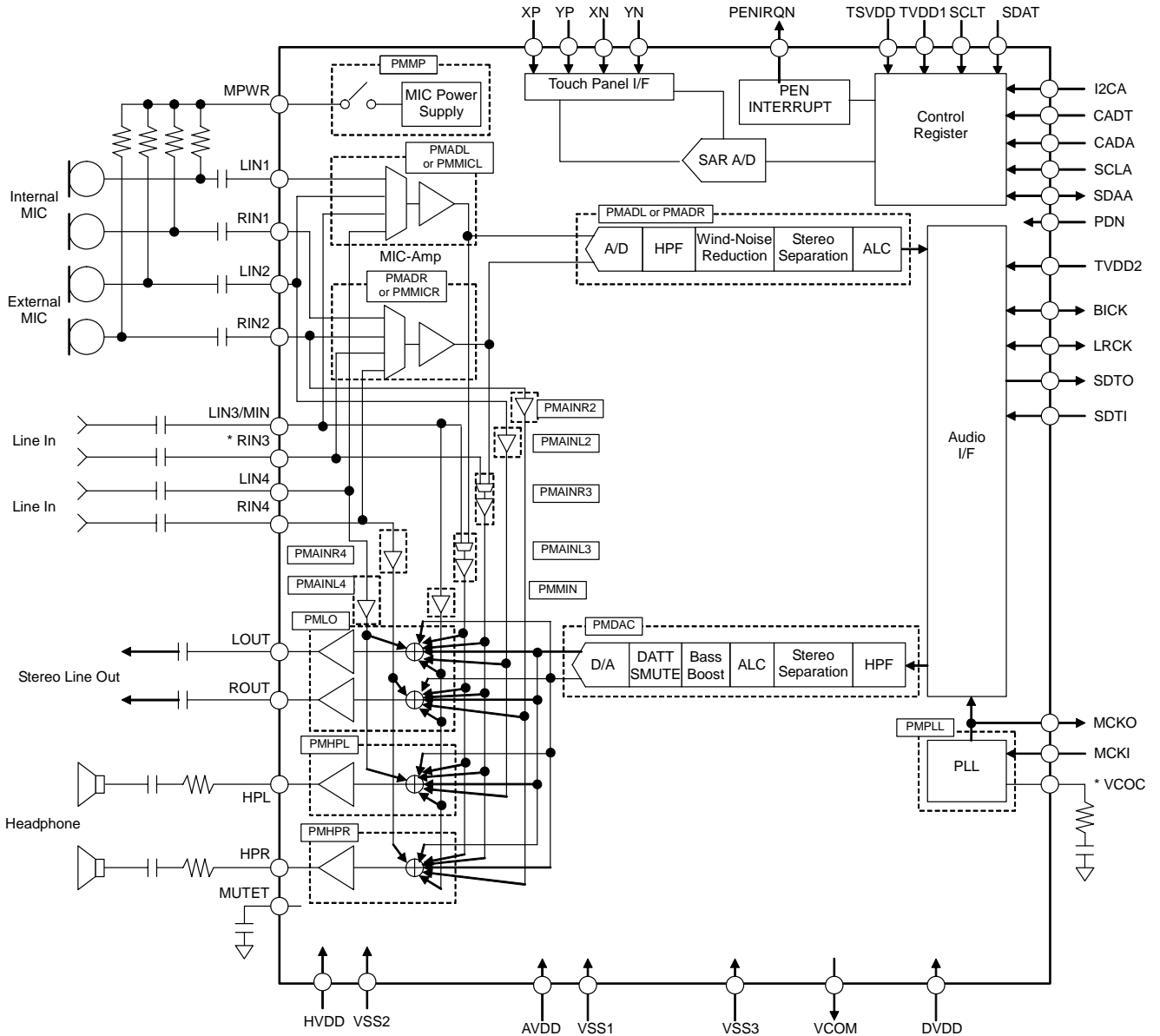
- Frequencies:
 - MCKI pin: 11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz, 27MHz
 - LRCK pin: 1fs
 - BICK pin: 32fs or 64fs

(2) External Clock Mode

- Frequencies: 256fs, 512fs or 1024fs (MCKI pin)

5. Output Master Clock Frequencies: 32fs/64fs/128fs/256fs

6. Sampling Rate:
 - PLL Slave Mode (LRCK pin): 7.35kHz ~ 48kHz
 - PLL Slave Mode (BICK pin): 7.35kHz ~ 48kHz
 - PLL Slave Mode (MCKI pin):
8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
 - PLL Master Mode:
8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
 - EXT Master/Slave Mode:
7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 26kHz (512fs), 7.35kHz ~ 13kHz (1024fs)
7. Master/Slave mode
8. Audio Interface Format: MSB First, 2's complement
 - ADC: 16bit MSB justified, I²S, DSP Mode
 - DAC: 16bit MSB justified, 16bit LSB justified, 16-24bit I²S, DSP Mode
9. Touch Screen Control Function
 - 12-bit SAR type A/D Converter with S/H circuit
 - 4-wire Resistive Touch Screen Interface
 - Pen Pressure Measurement
 - Auto Power Down
 - Continuous Read Operation
10. μ P I/F: I²C Bus (Ver 1.0, 400kHz Fast-Mode)
11. Ta = -30 ~ 85°C
12. Power Supply:
 - AVDD (Analog): 2.6 ~ 3.6V
 - DVDD (Digital): 2.6 ~ 3.6V
 - HVDD (Headphone): 2.6 ~ 5.25V
 - TVDD1 (Digital I/O): 2.5 ~ 3.6V
 - TVDD2 (Digital I/O): 1.6 ~ 3.6V
 - TSVDD (Touch Screen Controller): 2.5 ~ 3.6V
13. Package: 57pin BGA (5mm x 5mm, 0.5mm pitch)

■ Block Diagram


(VCOC and RIN3 pins are shared by the same pin.)

Figure 1. Block Diagram

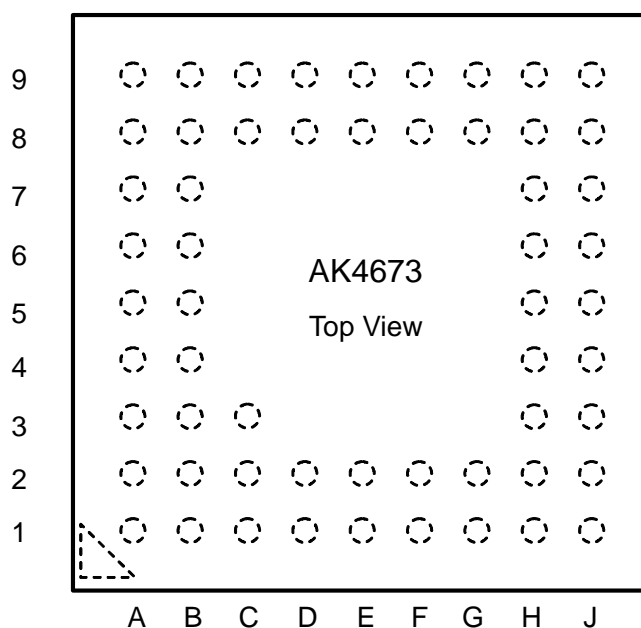
■ Ordering Guide

 AK4673EG
 AKD4673

 -30 ~ +85°C
 Evaluation board for AK4673

57pin BGA (0.5mm pitch)

■ Pin Layout



| | | | | | | | | | |
|---|-----------|-----------|----------|------|---------------|---------|-----|-------|-------|
| 9 | NC | MUTET | HPL | HVDD | SCLT | CADT | NC | MCKI | NC |
| 8 | RIN4/IN4- | NC | HPR | VSS2 | SDAT | PENIRQN | NC | MCKO | NC |
| 7 | ROUT/LON | LIN4/IN4+ | Top View | | | | | NC | TVDD1 |
| 6 | LOUT/LOP | MIN/LIN3 | | | | | | TVDD2 | DVDD |
| 5 | NC | RIN2/IN2- | | | | | | NC | VSS3 |
| 4 | TSVDD | LIN2/IN2+ | | | | | | LRCK | BICK |
| 3 | LIN1/IN1- | NC | NC | | | | | SDTI | SDTO |
| 2 | VCOM | RIN1/IN1+ | MPWR | I2CA | VCOC/ RIN3 | NC | PDN | SCLA | SDAA |
| 1 | NC | VSS1 | AVDD | XP | YP | XN | YN | CADA | NC |
| | A | B | C | D | E | F | G | H | J |

| PIN/FUNCTION | | | |
|--------------|----------|-----|---|
| No. | Pin Name | I/O | Function |
| A1 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |
| C2 | MPWR | O | MIC Power Supply Pin |
| A2 | VCOM | O | Common Voltage Output Pin, 0.45 x AVDD Bias voltage of ADC inputs and DAC outputs. |
| B1 | VSS1 | - | Ground 1 Pin |
| C1 | AVDD | - | Analog Power Supply Pin, 2.6 ~ 3.6V |
| E2 | VCOC | O | Output Pin for Loop Filter of PLL Circuit (AIN3 bit = "0": PLL is available.) This pin should be connected to VSS1 with one resistor and capacitor in series. |
| | RIN3 | I | Rch Analog Input 3 Pin (AIN3 bit = "1": PLL is not available.) |
| F2 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |
| D2 | I2CA | I | I ² C Control Mode Pin. This pin should be tied to AVDD. |
| G2 | PDN | I | Power-Down Mode Pin (This pin is valid only for the Audio Block) "H": Power-up, "L": Power-down This pin does not apply to a power down and a reset for the TSC block and TSC related registers. Power-down on the TSC block is determined by the PD0 bit shown in Table 61 . |
| H1 | CADA | I | Audio Block I ² C bus Slave Address (CADA) bit Select Pin |
| H2 | SCLA | I | Audio Block Control Data Clock Pin. |
| J1 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |
| J2 | SDAA | I/O | Audio Block Control Data Input Pin. |
| H3 | SDTI | I | Audio Serial Data Input Pin |
| J3 | SDTO | O | Audio Serial Data Output Pin |
| H4 | LRCK | I/O | Input / Output Channel Clock Pin |
| J4 | BICK | I/O | Audio Serial Data Clock Pin |
| H5 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |
| J6 | DVDD | - | Digital Power Supply Pin, 2.6 ~ 3.6V |
| H7 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |
| H6 | TVDD2 | - | Digital I/O Power Supply Pin (Audio Stream), 1.6 ~ 3.6V |
| J7 | TVDD1 | - | Digital I/O Power Supply Pin (uP I/F), 2.5 ~ 3.6V This pin should be connected to TSVDD pin. |
| J8 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |
| H9 | MCKI | I | External Master Clock Input Pin |
| G8 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |
| G9 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |
| H8 | MCKO | O | Master Clock Output Pin |
| J9 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |
| D8 | VSS2 | - | Ground 2 Pin |
| D9 | HVDD | - | Headphone Amp Power Supply Pin, 2.6 ~ 5.25V |
| C8 | HPR | O | Rch Headphone-Amp Output Pin |
| C9 | HPL | O | Lch Headphone-Amp Output Pin |
| B8 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |
| B9 | MUTET | O | Mute Time Constant Control Pin Connected to VSS2 pin with a capacitor for mute time constant. |

| | | | |
|----|---------|-----|---|
| A9 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |
| A8 | RIN4 | I | Rch Analog Input 4 Pin (L4DIF bit = "0": Single-ended Input) |
| | IN4- | I | Negative Line Input 4 Pin (L4DIF bit = "1": Full-differential Input) |
| B7 | LIN4 | I | Lch Analog Input 4 Pin (L4DIF bit = "0": Single-ended Input) |
| | IN4+ | I | Positive Line Input 4 Pin (L4DIF bit = "1": Full-differential Input) |
| A7 | ROUT | O | Rch Stereo Line Output Pin (LODIF bit = "0": Single-ended Stereo Output) |
| | LON | O | Negative Line Output Pin (LODIF bit = "1": Full-differential Mono Output) |
| A6 | LOUT | O | Lch Stereo Line Output Pin (LODIF bit = "0": Single-ended Stereo Output) |
| | LOP | O | Positive Line Output Pin (LODIF bit = "1": Full-differential Mono Output) |
| B6 | MIN | I | Mono Signal Input Pin (AIN3 bit = "0": PLL is available.) |
| | LIN3 | I | Lch Analog Input 3 Pin (AIN3 bit = "1": PLL is not available.) |
| A5 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |
| B5 | RIN2 | I | Rch Analog Input 2 Pin (MDIF2 bit = "0": Single-ended Input) |
| | IN2- | I | Microphone Negative Input 2 Pin (MDIF2 bit = "1": Full-differential Input) |
| B4 | LIN2 | I | Lch Analog Input 2 Pin (MDIF2 bit = "0": Single-ended Input) |
| | IN2+ | I | Microphone Positive Input 2 Pin (MDIF2 bit = "1": Full-differential Input) |
| A3 | LIN1 | I | Lch Analog Input 1 Pin (MDIF1 bit = "0": Single-ended Input) |
| | IN1- | I | Microphone Negative Input 1 Pin (MDIF1 bit = "1": Full-differential Input) |
| B2 | RIN1 | I | Rch Analog Input 1 Pin (MDIF1 bit = "0": Single-ended Input) |
| | IN1+ | I | Microphone Positive Input 1 Pin (MDIF1 bit = "1": Full-differential Input) |
| A4 | TSVDD | - | TSC Power Supply Pin, 2.5 ~ 3.6V. This pin should be connected to TVDD1 pin. |
| B3 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |
| D1 | XP | I/O | Touch Screen X+ plate Voltage supply <ul style="list-style-type: none"> ■ X axis Measurement: Supplies the voltage to X+ position input of the touch panel. ■ Y axis Measurement: This pin is used as the input for the A/D converter ■ Pen Pressure Measurement: This pin is the input for the A/D converter at Z1 measurement. ■ Pen Waiting State: Pulled up by an internal resistor (typ.10K ohm). |
| E1 | YP | I/O | Touch Screen Y+ plate Voltage supply <ul style="list-style-type: none"> ■ X axis Measurement: This pin is used as the input for the A/D converter ■ Y axis Measurement: Supplies the voltage to Y+ position input of the touch panel ■ Pen Pressure Measurement: Supplies the voltage to Y+ position input of the touch panel. ■ Pen Waiting State: OPEN state |
| F1 | XN | I/O | Touch Screen X- plate Voltage supply <ul style="list-style-type: none"> ■ X axis Measurement: Supplies the voltage to X- position input of the touch panel ■ Y axis Measurement: OPEN state ■ Pen Pressure Measurement: Supplies the voltage to X- position input of the touch panel ■ Pen Waiting State: OPEN state |
| G1 | YN | I/O | Touch Screen Y- plate Voltage supply <ul style="list-style-type: none"> ■ X axis Measurement: OPEN state ■ Y axis Measurement: Supplies the voltage to Y- position input of the touch panel ■ Pen Pressure Measurement: This pin is the input for the A/D converter at Z2 measurement. ■ Pen Waiting State: connected to VSS3. |
| J5 | VSS3 | - | Ground 3 Pin |
| F8 | PENIRQN | O | Pen Interrupt Output This pin is "L" during the pen down on pen interrupt enabled state otherwise this pin is "H". This pin is "L" during the pen interrupt disabled regardless pen touch. |
| F9 | CADT | I | TSC block I ² C bus Slave Address(CADT) bit Select Pin |
| E8 | SDAT | I/O | TSC block I ² C serial data. |
| E9 | SCLT | I | TSC block I ² C serial clock. |
| C3 | NC | - | No Connection pin No internal bonding. This pin should be connected to ground (VSS1, VSS2 or VSS3 pin). |

Note 1. All input pins except analog input pins (MIN/LIN3, LIN1, RIN1, LIN2, RIN2, RIN3, RIN4, LIN4, XP, YP, XN and YN) should not be left floating.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

| Classification | Pin Name | Setting |
|----------------|---|---------------------------------------|
| Analog | MPWR, VCOC/RIN3, HPR, HPL, MUTET, RIN4/IN4-, LIN4/IN4+, ROUT/LOP, LOUT/LON, MIN/LIN3, RIN2/IN2-, LIN2/IN2+, LIN1/IN1-, RIN1/IN1+, XP, YP, XN, YN, PENIRQN | These pins should be open. |
| Digital | MCKO | This pin should be open. |
| | MCKI | This pin should be connected to VSS2. |

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=VSS3=0V; [Note 2](#))

| Parameter | Symbol | min | max | Units | |
|--|---------------|-------|-----------|-------|---|
| Power Supplies: | Analog | AVDD | -0.3 | 6.0 | V |
| | Digital | DVDD | -0.3 | 6.0 | V |
| | Digital I/O1 | TVDD1 | -0.3 | 6.0 | V |
| | Digital I/O2 | TVDD2 | -0.3 | 6.0 | V |
| | Headphone-Amp | HVDD | -0.3 | 6.0 | V |
| | TSC | TSVDD | -0.3 | 6.0 | V |
| Input Current, Any Pin Except Supplies | IIN | - | ±10 | mA | |
| Analog Input Voltage (Note 3) | VINA | -0.3 | AVDD+0.3 | V | |
| Digital Input Voltage (Note 4) | VIND1 | -0.3 | TVDD1+0.3 | V | |
| Digital Input Voltage (Note 5) | VIND2 | -0.3 | TVDD2+0.3 | V | |
| TSC Input Voltage (Note 6) | VIND3 | -0.3 | TSVDD+0.3 | V | |
| Touch panel Drive Current | IOUTDRV | | 50 | mA | |
| Ambient Temperature (powered applied) | Ta | -30 | 85 | °C | |
| Storage Temperature | Tstg | -65 | 150 | °C | |

Note 2. All voltages with respect to ground.

Note 3. I2CA, RIN4/IN4-, LIN4/IN4+, MIN/LIN3, RIN3, RIN2/IN2-, LIN2/IN2+, LIN1/IN1-, RIN1/IN1+ pins

Note 4 PDN, CADA, SCLA, SDAA pins

Pull-up resistors at SDAA and SCLA pins should be connected to (TVDD1+0.3) V or less voltage.

Note 5. SDTI, LRCK, BICK, MCKI pins

Note 6 XP, XN, YP, YN, CADT, SCLT, SDAT pins

Pull-up resistors at SDAT and SCLT pins should be connected to (TSVDD+0.3) V or less voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=0V; [Note 2](#))

| Parameter | Symbol | min | typ | max | Units | |
|--|--------------|-------|-----|-----------|-------|---|
| Power Supplies (Note 7) | Analog | AVDD | 2.6 | 3.3 | 3.6 | V |
| | Digital | DVDD | 2.6 | 3.3 | 3.6 | V |
| | Digital I/O1 | TVDD1 | 2.5 | 3.3 | DVDD | V |
| | Digital I/O2 | TVDD2 | 1.6 | 3.3 | DVDD | V |
| | HP-Amp | HVDD | 2.6 | 3.3 / 5.0 | 5.25 | V |
| | TSC | TSVDD | 2.5 | 3.3 | 3.6 | V |

Note 2. All voltages with respect to ground.

Note 7. The power-up sequence among AVDD, DVDD, TVDD1, TVDD2, HVDD and TSVDD is not critical. The PDN pin should be held to “L” when power-up. The PDN pin should be set to “H” after all power supplies are powered-up. The AK4673 should be operated by the recommended power-up/down sequence shown in “System Design (Grounding and Power Supply Decoupling)” to avoid pop noise at line output and headphone output. When one of power supplies is partially powered OFF, the power supply current at power-down mode may be increased. All the power supplies should be powered OFF when the power supply is powered OFF.

* AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

*** SDAA and SDAT are written as SDA, and also SCLA and SCLT are written as SCL unless otherwise specified in this datasheet.**

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=TVDD1=TVDD2=HVDD=TSVDD=3.3V; VSS1=VSS2=VSS3=0V; fs=44.1kHz, BICK=64fs; Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

| Parameter | | min | typ | max | Units |
|--|------------------------------------|-------|-------|-------|-------|
| MIC Amplifier: LIN1/RIN1/LIN2/RIN2/LIN4/RIN4 pins & LIN3/RIN3 pins (AIN3 bit = "1"); MDIF1=MDIF2 bits = "0" (Single-ended inputs) | | | | | |
| Input Resistance | MGAIN1-0 bits = "00" | 40 | 60 | 80 | kΩ |
| | MGAIN1-0 bits = "01", "10" or "11" | 20 | 30 | 40 | kΩ |
| Gain | MGAIN1-0 bits = "00" | - | 0 | - | dB |
| | MGAIN1-0 bits = "01" | - | +20 | - | dB |
| | MGAIN1-0 bits = "10" | - | +26 | - | dB |
| | MGAIN1-0 bits = "11" | - | +32 | - | dB |
| MIC Amplifier: IN1+/IN1-/IN2+/IN2- pins; MDIF1 = MDIF2 bits = "1" (Full-differential input) | | | | | |
| Input Voltage (Note 8) | | | | | |
| | MGAIN1-0 bits = "01" | - | - | 0.228 | Vpp |
| | MGAIN1-0 bits = "10" | - | - | 0.114 | Vpp |
| | MGAIN1-0 bits = "11" | - | - | 0.057 | Vpp |
| MIC Power Supply: MPWR pin | | | | | |
| Output Voltage (Note 9) | | 2.22 | 2.47 | 2.72 | V |
| Load Resistance | | 0.5 | - | - | kΩ |
| Load Capacitance | | - | - | 30 | pF |
| ADC Analog Input Characteristics: LIN1/RIN1/LIN2/RIN2/LIN4/RIN4 pins & LIN3/RIN3 pins (AIN3 bit = "1") → ADC → IVOL, IVOL=0dB, ALC=OFF | | | | | |
| Resolution | | - | - | 16 | Bits |
| Input Voltage (Note 10) | (Note 11) | 0.168 | 0.198 | 0.228 | Vpp |
| | (Note 12) | 1.68 | 1.98 | 2.28 | Vpp |
| S/(N+D) (-1dBFS) | (Note 11, LIN1/RIN1/LIN2/RIN2) | 71 | 83 | - | dBFS |
| | (Note 11, LIN3/RIN3/LIN4/RIN4) | - | 83 | - | dBFS |
| | (Note 12, except for LIN3/RIN3) | - | 88 | - | dBFS |
| | (Note 12, LIN3/RIN3) | - | 72 | - | dBFS |
| D-Range (-60dBFS, A-weighted) | (Note 11) | 76 | 86 | - | dB |
| | (Note 12) | - | 95 | - | dB |
| S/N (A-weighted) | (Note 11) | 76 | 86 | - | dB |
| | (Note 12) | - | 95 | - | dB |
| Interchannel Isolation | (Note 11) | 75 | 90 | - | dB |
| | (Note 12) | - | 100 | - | dB |
| Interchannel Gain Mismatch | (Note 11) | - | 0.1 | 0.8 | dB |
| | (Note 12) | - | 0.1 | 0.8 | dB |

Note 8. The voltage difference between IN1/2+ and IN1/2- pins. AC coupling capacitor should be inserted in series at each input pin. Full-differential mic input is not available at MGAIN1-0 bits = "00". Maximum input voltage of IN1+, IN1-, IN2+ and IN2- pins is proportional to AVDD voltage, respectively.

$V_{in} = 0.069 \times AVDD$ (max)@MGAIN1-0 bits = "01", $0.035 \times AVDD$ (max)@MGAIN1-0 bits = "10", $0.017 \times AVDD$ (max)@MGAIN1-0 bits = "11".

When the signal larger than above value is input to IN1+, IN1-, IN2+ or IN2- pin, ADC does not operate normally.

Note 9. Output voltage is proportional to AVDD voltage. $V_{out} = 0.75 \times AVDD$ (typ)

Note 10. Input voltage is proportional to AVDD voltage. $V_{in} = 0.06 \times AVDD$ (typ)@MGAIN1-0 bits = "01" (+20dB), $V_{in} = 0.6 \times AVDD$ (typ)@MGAIN1-0 bits = "00" (0dB)

Note 11. MGAIN1-0 bits = "01" (+20dB)

Note 12. MGAIN1-0 bits = "00" (0dB)

| Parameter | | min | typ | max | Units |
|---|----------------|------|------|------|-----------|
| DAC Characteristics: | | | | | |
| Resolution | | - | - | 16 | Bits |
| Stereo Line Output Characteristics: DAC → LOUT/ROUT pins, ALC=OFF, IVOL=0dB, DVOL=0dB, LOVL bit = "0", LODIF bit = "0", $R_L=10k\Omega$ (Single-ended) | | | | | |
| Output Voltage (Note 13) | LOVL bit = "0" | 1.78 | 1.98 | 2.18 | V_{pp} |
| | LOVL bit = "1" | 2.25 | 2.50 | 2.75 | V_{pp} |
| S/(N+D) (-3dBFS) | | 78 | 88 | - | dBFS |
| S/N (A-weighted) | | 82 | 92 | - | dB |
| Interchannel Isolation | | 80 | 100 | - | dB |
| Interchannel Gain Mismatch | | - | 0.1 | 0.5 | dB |
| Load Resistance | | 10 | - | - | $k\Omega$ |
| Load Capacitance | | - | - | 30 | pF |
| Mono Line Output Characteristics: DAC → LOP/LON pins, ALC=OFF, IVOL=0dB, DVOL=0dB, LOVL bit = "0", LODIF bit = "1", $R_L=10k\Omega$ for each pin (Full-differential) | | | | | |
| Output Voltage (Note 14) | LOVL bit = "0" | 3.52 | 3.96 | 4.36 | V_{pp} |
| | LOVL bit = "1" | - | 5.00 | - | V_{pp} |
| S/(N+D) (-3dBFS) | | 78 | 88 | - | dBFS |
| S/N (A-weighted) | | 85 | 95 | - | dB |
| Load Resistance (LOP/LON pins, respectively) | | 10 | - | - | $k\Omega$ |
| Load Capacitance (LOP/LON pins, respectively) | | - | - | 30 | pF |

Note 13. Output voltage is proportional to AVDD voltage. $V_{out} = 0.6 \times AVDD$ (typ)@LOVL bit = "0".

Note 14. Output voltage is proportional to AVDD voltage. $V_{out} = (LOP) - (LON) = 1.2 \times AVDD$ (typ)@LOVL bit = "0".

| Parameter | | min | typ | max | Units |
|--|----------------|------|------|------|------------------|
| Headphone-Amp Characteristics: DAC → HPL/HPR pins, ALC=OFF, IVOL=0dB, DVOL=0dB, VBAT bit = "0"; unless otherwise specified. | | | | | |
| Output Voltage (Note 15) | | | | | |
| HPG bit = "0", 0dBFS, HVDD=3.3V, $R_L=22.8\Omega$ | | 1.58 | 1.98 | 2.38 | V _{pp} |
| HPG bit = "1", 0dBFS, HVDD=5V, $R_L=100\Omega$ | | 2.40 | 3.00 | 3.60 | V _{pp} |
| HPG bit = "1", 0dBFS, HVDD=3.3V, $R_L=16\Omega$ (Po=62mW) | | - | 1.0 | - | V _{rms} |
| HPG bit = "1", 0dBFS, HVDD=5V, $R_L=16\Omega$ (Po=70mW) | | - | 1.06 | - | V _{rms} |
| S/(N+D) | | | | | |
| HPG bit = "0", -3dBFS, HVDD=3.3V, $R_L=22.8\Omega$ | | 60 | 70 | - | dBFS |
| HPG bit = "1", -3dBFS, HVDD=5V, $R_L=100\Omega$ | | - | 80 | - | dBFS |
| HPG bit = "1", 0dBFS, HVDD=3.3V, $R_L=16\Omega$ (Po=62mW) | | - | 20 | - | dBFS |
| HPG bit = "1", 0dBFS, HVDD=5V, $R_L=16\Omega$ (Po=70mW) | | - | 70 | - | dBFS |
| S/N (A-weighted) | (Note 16) | 80 | 90 | - | dB |
| | (Note 17) | - | 90 | - | dB |
| Interchannel Isolation | (Note 16) | 65 | 75 | - | dB |
| | (Note 17) | - | 80 | - | dB |
| Interchannel Gain Mismatch | (Note 16) | - | 0.1 | 0.8 | dB |
| | (Note 17) | - | 0.1 | 0.8 | dB |
| Load Resistance | | 16 | - | - | Ω |
| Load Capacitance | C1 in Figure 2 | - | - | 30 | pF |
| | C2 in Figure 2 | - | - | 300 | pF |

Note 15. Output voltage is proportional to AVDD voltage.

$$V_{out} = 0.6 \times AVDD(\text{typ}) @ \text{HPG bit} = "0", 0.91 \times AVDD(\text{typ}) @ \text{HPG bit} = "1".$$

Note 16. HPG bit = "0", HVDD=3.3V, $R_L=22.8\Omega$.

Note 17. HPG bit = "1", HVDD=5V, $R_L=100\Omega$.

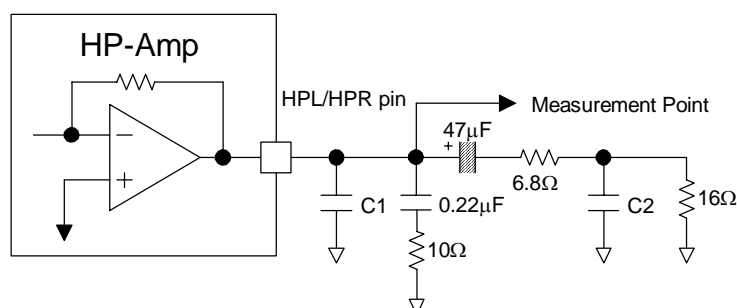


Figure 2. Headphone-Amp output circuit

| Parameter | | min | typ | max | Units |
|--|----------------|-------|-------|-------|-----------------|
| Mono Input: MIN pin (AIN3 bit = "0"; External Input Resistance=20kΩ) | | | | | |
| Maximum Input Voltage (Note 18) | | - | 1.98 | - | V _{pp} |
| Gain (Note 19) | | | | | |
| MIN → LOU/ROUT | LOVL bit = "0" | -4.5 | 0 | +4.5 | dB |
| | LOVL bit = "1" | - | +2 | - | dB |
| MIN → HPL/HPR | HPG bit = "0" | -24.5 | -20 | -15.5 | dB |
| | HPG bit = "1" | - | -16.4 | - | dB |
| Stereo Input: LIN2/RIN2/LIN4/RIN4 pins; LIN3/RIN3 pins (AIN3 bit = "1") | | | | | |
| Maximum Input Voltage (Note 20) | | - | 1.98 | - | V _{pp} |
| Gain | | | | | |
| LIN/RIN → LOU/ROUT | LOVL bit = "0" | -4.5 | 0 | +4.5 | dB |
| | LOVL bit = "1" | - | +2 | - | dB |
| LIN/RIN → HPL/HPR | HPG bit = "0" | -4.5 | 0 | +4.5 | dB |
| | HPG bit = "1" | - | +3.6 | - | dB |
| Full-differential Mono Input: IN4+/- pins (L4DIF bit = "1") | | | | | |
| Maximum Input Voltage (Note 21) | | - | 3.96 | - | V _{pp} |
| Gain | | | | | |
| IN4+/- → LOU/ROUT (LODIF bit = "0") | LOVL bit = "0" | -10.5 | -6 | -1.5 | dB |
| | LOVL bit = "1" | - | -4 | - | dB |
| IN4+/- → LOP/LON (LODIF bit = "1") (Note 22) | LOVL bit = "0" | -4.5 | 0 | +4.5 | dB |
| | LOVL bit = "1" | - | +2 | - | dB |
| IN4+/- → HPL/HPR | HPG bit = "0" | -10.5 | -6 | -1.5 | dB |
| | HPG bit = "1" | - | -2.4 | - | dB |

Note 18. Maximum voltage is in proportion to both AVDD and external input resistance (R_{in}). $V_{in} = 0.6 \times AVDD \times R_{in} / 20k\Omega$ (typ).

Note 19. The gain is in inverse proportion to external input resistance.

Note 20. Maximum Input voltage is proportional to AVDD voltage. $V_{out} = 0.6 \times AVDD$ (typ).

Note 21. Maximum Input voltage is proportional to AVDD voltage. $V_{out} = (IN4+) - (IN4-) = 1.2 \times AVDD$ (typ). The signals with same amplitude and inverted phase should be input to IN4+ and IN4- pins, respectively.

Note 22. $V_{out} = (LOP) - (LON)$ at LODIF bit = "1".

| SAR ADC Analog Input Characteristics: XP, YP, YN input → SAR ADC | | | | | |
|---|------------------------------|-------------|-------------|--------------|----|
| Parameter | min. | typ. | max. | Units | |
| ADC for Touch Screen | | | | | |
| Resolution | | 12 | | Bits | |
| No Missing Codes | 11 | 12 | | Bits | |
| Integral Nonlinearity (INL) Error | | | ±2 | LSB | |
| Differential Nonlinearity (DNL) Error | | ±1 | | LSB | |
| Offset Error | | | ±6 | LSB | |
| Gain Error | | | ±4 | LSB | |
| Throughput Rate | | 8.2 | | ksps | |
| Touch Panel Driver On-Resistance | | | | | |
| XP, YP | | 5 | | Ω | |
| XN, YN | | 5 | | Ω | |
| XP Pull Up Register (when pen interrupt enable) | | 10 | | kΩ | |
| Power Supplies: | | | | | |
| Power-Up (PDN pin = "H", PD0 bit="0") | | | | | |
| All Circuit Power-up: | | | | | |
| Audio Block | | | | | |
| AVDD+DVDD+TVDD1+TVDD2 (Note 23) | - | 16 | 24 | mA | |
| HVDD: HP-Amp Normal Operation No Output (Note 24) | - | 5 | 8 | mA | |
| TSVDD | | | | | |
| Normal Mode Addressed | Fast Mode: SCL=400KHz | | 0.1 | 0.2 | mA |
| | Standard Mode: SCL=100KHz | | 0.077 | 0.15 | mA |
| Power Down Not Addressed | Fast Mode: SCL=400KHz | | 0.023 | | mA |
| | Standard Mode: SCL=100KHz | | 0.006 | | mA |
| Power-Down (PDN pin = "L", PD0 bit = "0") (Note 25) | | | | | |
| AVDD+DVDD+TVDD1+TVDD2+HVDD+ TSVDD | - | 1 | 100 | μA | |

Note 23. PLL Master Mode (MCKI=12.288MHz) and PMADL = PMADR = PMDAC = PMLO = PMHPL = PMHPR = PMVCM = PMPLL = MCKO = PMMIN = PMMP = M/S bits = "1". MPWR pin outputs 0mA.
 AVDD=11mA(typ), DVDD=3mA(typ), TVDD1+TVDD2=2mA(typ).
 EXT Slave Mode (PMPLL = M/S = MCKO bits = "0"): AVDD=10mA(typ), DVDD=3mA(typ),
 TVDD1+TVDD2=0.03mA(typ).

Note 24. PMADL = PMADR = PMDAC = PMLO = PMHPL = PMHPR = PMVCM = PMPLL = PMMIN bits = "1".

Note 25. All digital input pins are fixed to each supply pin (TVDD1, TVDD2 or TSVDD) or (VSS2 or VSS3).

■ Power Consumption for Each Operation Mode

Conditions: Ta=25°C; AVDD=DVDD=TVDD1=TVDD2=HVDD=TSVDD=3.3V; VSS1=VSS2=VSS3=0V;
fs=44.1kHz, External Slave Mode, BICK=64fs; 1kHz, 0dBFS input; Headphone = No output.

| Mode | Power Management Bit | | | | | | | | | | | | | | | AVDD [mA] | DVDD [mA] | TVDD1+TVDD2 [mA] | HVDD [mA] | Total Power [mW] | | | | | | |
|-------------------------------|----------------------|-------|------|-------|-------|-------|-------|-------|--------|--------|---------|---------|---------|---------|---------|--------------|--------------|---------------------|--------------|---------------------|---------|-----|-----|------|-----|------|
| | 00H | | | | | 01H | | 20H | | | | | | | | | | | | | | | | | | |
| | PMVCM | PMMIN | PML0 | PMDAC | PMADL | PMHPL | PMHPR | PMADR | PMMICL | PMMICR | PMAINL2 | PMAINR2 | PMAINL3 | PMAINR3 | PMAINL4 | | | | | | PMAINR4 | | | | | |
| All Power-down | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | |
| DAC → Lineout | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4.4 | 1.8 | 0.03 | 0.2 | 21.2 |
| DAC → HP | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3.8 | 1.8 | 0.03 | 5 | 35.1 |
| LIN2/RIN2 → HP | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1.9 | 0 | 0 | 5 | 22.8 |
| LIN2/RIN2 → ADC | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 5.5 | 1.6 | 0.03 | 0.2 | 24.2 |
| LIN1 (Mono) → ADC | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3.5 | 1.5 | 0.03 | 0.2 | 17.3 |
| LIN2/RIN2 → ADC & DAC → HP | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 8.3 | 2.7 | 0.03 | 5 | 52.9 |

Table 1. Power Consumption for each operation mode (typ)

FILTER CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=2.6 ~ 3.6V, TVDD1=2.5 ~ 3.6V, TVDD2=1.6 ~ 3.6V, HVDD=2.6 ~ 5.25V, TSVDD=3.3V, fs=44.1kHz; DEM=OFF; FIL1=FIL3=EQ=OFF)

| Parameter | | Symbol | min | typ | max | Units | |
|---|---------|--------|------|-------|-------|-------|----|
| ADC Digital Filter (Decimation LPF): | | | | | | | |
| Passband (Note 26) | ±0.16dB | PB | 0 | - | 17.3 | kHz | |
| | -0.66dB | | - | 19.4 | - | kHz | |
| | -1.1dB | | - | 19.9 | - | kHz | |
| | -6.9dB | | - | 22.1 | - | kHz | |
| Stopband | | SB | 26.1 | - | - | kHz | |
| Passband Ripple | | PR | - | - | ±0.1 | dB | |
| Stopband Attenuation | | SA | 73 | - | - | dB | |
| Group Delay (Note 27) | | GD | - | 19 | - | 1/fs | |
| Group Delay Distortion | | ΔGD | - | 0 | - | μs | |
| ADC Digital Filter (HPF): (Note 28) | | | | | | | |
| Frequency Response (Note 26) | -3.0dB | FR | - | 0.9 | - | Hz | |
| | -0.5dB | | - | 2.7 | - | Hz | |
| | -0.1dB | | - | 6.0 | - | Hz | |
| DAC Digital Filter (LPF): | | | | | | | |
| Passband (Note 26) | ±0.1dB | PB | 0 | - | 19.6 | kHz | |
| | -0.7dB | | - | 20.0 | - | kHz | |
| | -6.0dB | | - | 22.05 | - | kHz | |
| Stopband | | SB | 25.2 | - | - | kHz | |
| Passband Ripple | | PR | - | - | ±0.01 | dB | |
| Stopband Attenuation | | SA | 59 | - | - | dB | |
| Group Delay (Note 27) | | GD | - | 25 | - | 1/fs | |
| DAC Digital Filter (LPF) + SCF: | | | | | | | |
| Frequency Response: 0 ~ 20.0kHz | | FR | - | ±1.0 | - | dB | |
| DAC Digital Filter (HPF): (Note 28) | | | | | | | |
| Frequency Response (Note 26) | -3.0dB | FR | - | 0.9 | - | Hz | |
| | -0.5dB | | - | 2.7 | - | Hz | |
| | -0.1dB | | - | 6.0 | - | Hz | |
| BOOST Filter: (Note 29) | | | | | | | |
| Frequency Response | MIN | 20Hz | FR | - | 5.76 | - | dB |
| | | 100Hz | | - | 2.92 | - | dB |
| | | 1kHz | | - | 0.02 | - | dB |
| | MID | 20Hz | FR | - | 10.80 | - | dB |
| | | 100Hz | | - | 6.84 | - | dB |
| | | 1kHz | | - | 0.13 | - | dB |
| | MAX | 20Hz | FR | - | 16.06 | - | dB |
| | | 100Hz | | - | 10.54 | - | dB |
| | | 1kHz | | - | 0.37 | - | dB |

Note 26. The passband and stopband frequencies scale with fs (system sampling rate).

For example, DAC is PB=0.454*fs (@-0.7dB). Each response refers to that of 1kHz.

Note 27. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of both channels from the input register to the output register of the ADC. This time includes the group delay of the HPF. For the DAC, this time is from setting the 16-bit data of both channels from the input register to the output of analog signal. Group delay of DAC part is 25/fs(typ) at PMADL=PMADR bits = "0".

Note 28. When PMADL bit = "1" or PMADR bit = "1", the HPF of ADC is enabled but the HPF of DAC is disabled. When PMADL=PMADR bits = "0", PMDAC bit = "1", the HPF of DAC is enabled but the HPF of ADC is disabled.

Note 29. These frequency responses scale with fs. If a high-level and low frequency signal is input, the analog output clips to the full-scale.

DC CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=2.6 ~ 3.6V, TVDD1=TSVDD=2.5 ~ 3.6V, TVDD2=1.6 ~ 3.6V, HVDD=2.6 ~ 5.25V)

| Parameter | | Symbol | min | Typ | max | Units |
|--|-----------------|--------|-----------|-----|----------|-------|
| High-Level Input Voltage | 2.5V≤TVDD1≤3.6V | VIH1 | 70%TVDD1 | - | - | V |
| | 2.2V≤TVDD2≤3.6V | VIH2 | 70%TVDD2 | - | - | V |
| | 1.6V≤TVDD2<2.2V | VIH2 | 75%TVDD2 | - | - | V |
| | 2.5V≤TSVDD≤3.6V | VIH3 | 70%TSVDD | - | - | V |
| Low-Level Input Voltage | 2.5V≤TVDD1≤3.6V | VIL1 | - | - | 30%TVDD1 | V |
| | 2.2V≤TVDD2≤3.6V | VIL2 | - | - | 30%TVDD2 | V |
| | 1.6V≤TVDD2<2.2V | VIL2 | - | - | 25%TVDD2 | V |
| | 2.5V≤TSVDD≤3.6V | VIL3 | - | - | 30%TSVDD | V |
| High-Level Output Voltage Except PENIRQN pin (Iout = -200μA) Except PENIRQN pin (Iout = -200μA) PENIRQN pin (Iout = -250μA) | | VOHA | TVDD1-0.2 | - | - | V |
| | | VOHB | TVDD2-0.2 | - | - | V |
| | | VOHT | TSVDD-0.4 | - | - | V |
| Low-Level Output Voltage (Except SDA and PENIRQN pin: Iout = 200μA) (PENIRQN pin: Iout = 250mA) (SDA pin: Iout = 3mA) | | VOL | - | - | 0.2 | V |
| | | VOL | - | - | 0.4 | V |
| | | VOL | - | - | 0.4 | V |
| Input Leakage Current | | Iin | - | - | ±10 | μA |

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=2.6 ~ 3.6V; TVDD1 =TSVDD=2.5 ~ 3.6V; TVDD2=1.6 ~ 3.6V; HVDD=2.6 ~ 5.25V; CL=20pF; unless otherwise specified)

| Parameter | | Symbol | min | typ | max | Units |
|---|-----------------------------------|--------|----------|----------|--------|-------|
| PLL Master Mode (PLL Reference Clock = MCKI pin) | | | | | | |
| MCKI Input Timing | | | | | | |
| Frequency | | fCLK | 11.2896 | - | 27 | MHz |
| Pulse Width Low | | tCLKL | 0.4/fCLK | - | - | ns |
| Pulse Width High | | tCLKH | 0.4/fCLK | - | - | ns |
| MCKO Output Timing | | | | | | |
| Frequency | | fMCK | 0.2352 | - | 12.288 | MHz |
| Duty Cycle | | | | | | |
| | Except 256fs at fs=32kHz, 29.4kHz | dMCK | 40 | 50 | 60 | % |
| | 256fs at fs=32kHz, 29.4kHz | dMCK | - | 33 | - | % |
| LRCK Output Timing | | | | | | |
| Frequency | | fs | 7.35 | - | 48 | kHz |
| DSP Mode: Pulse Width High | | tLRCKH | - | tBCK | - | ns |
| Except DSP Mode: Duty Cycle | | Duty | - | 50 | - | % |
| BICK Output Timing | | | | | | |
| Period | BCKO bit = "0" | tBCK | - | 1/(32fs) | - | ns |
| | BCKO bit = "1" | tBCK | - | 1/(64fs) | - | ns |
| Duty Cycle | | dBCK | - | 50 | - | % |

| Parameter | Symbol | min | typ | max | Units | |
|--|----------------------|------------|--------|-------------|--------|-----|
| PLL Slave Mode (PLL Reference Clock = MCKI pin) | | | | | | |
| MCKI Input Timing | | | | | | |
| Frequency | fCLK | 11.2896 | - | 27 | MHz | |
| Pulse Width Low | tCLKL | 0.4/fCLK | - | - | ns | |
| Pulse Width High | tCLKH | 0.4/fCLK | - | - | ns | |
| MCKO Output Timing | | | | | | |
| Frequency | fMCK | 0.2352 | - | 12.288 | MHz | |
| Duty Cycle | | | | | | |
| Except 256fs at fs=32kHz, 29.4kHz | dMCK | 40 | 50 | 60 | % | |
| 256fs at fs=32kHz, 29.4kHz | dMCK | - | 33 | - | % | |
| LRCK Input Timing | | | | | | |
| Frequency | fs | 7.35 | - | 48 | kHz | |
| DSP Mode: Pulse Width High | tLRCKH | tBCK-60 | - | 1/fs - tBCK | ns | |
| Except DSP Mode: Duty Cycle | Duty | 45 | - | 55 | % | |
| BICK Input Timing | | | | | | |
| Period | tBCK | 1/(64fs) | - | 1/(32fs) | ns | |
| Pulse Width Low | tBCKL | 0.4 x tBCK | - | - | ns | |
| Pulse Width High | tBCKH | 0.4 x tBCK | - | - | ns | |
| PLL Slave Mode (PLL Reference Clock = LRCK pin) | | | | | | |
| LRCK Input Timing | | | | | | |
| Frequency | fs | 7.35 | - | 48 | kHz | |
| DSP Mode: Pulse Width High | tLRCKH | tBCK-60 | - | 1/fs - tBCK | ns | |
| Except DSP Mode: Duty Cycle | Duty | 45 | - | 55 | % | |
| BICK Input Timing | | | | | | |
| Period | tBCK | 1/(64fs) | - | 1/(32fs) | ns | |
| Pulse Width Low | tBCKL | 130 | - | - | ns | |
| Pulse Width High | tBCKH | 130 | - | - | ns | |
| PLL Slave Mode (PLL Reference Clock = BICK pin) | | | | | | |
| LRCK Input Timing | | | | | | |
| Frequency | fs | 7.35 | - | 48 | kHz | |
| DSP Mode: Pulse Width High | tLRCKH | tBCK-60 | - | 1/fs - tBCK | ns | |
| Except DSP Mode: Duty Cycle | Duty | 45 | - | 55 | % | |
| BICK Input Timing | | | | | | |
| Period | PLL3-0 bits = "0010" | tBCK | - | 1/(32fs) | ns | |
| | PLL3-0 bits = "0011" | tBCK | - | 1/(64fs) | ns | |
| Pulse Width Low | tBCKL | 0.4 x tBCK | - | - | ns | |
| Pulse Width High | tBCKH | 0.4 x tBCK | - | - | ns | |
| External Slave Mode | | | | | | |
| MCKI Input Timing | | | | | | |
| Frequency | 256fs | fCLK | 1.8816 | - | 12.288 | MHz |
| | 512fs | fCLK | 3.7632 | - | 13.312 | MHz |
| | 1024fs | fCLK | 7.5264 | - | 13.312 | MHz |
| Pulse Width Low | tCLKL | 0.4/fCLK | - | - | ns | |
| Pulse Width High | tCLKH | 0.4/fCLK | - | - | ns | |
| LRCK Input Timing | | | | | | |
| Frequency | 256fs | fs | 7.35 | - | 48 | kHz |
| | 512fs | fs | 7.35 | - | 26 | kHz |
| | 1024fs | fs | 7.35 | - | 13 | kHz |
| DSP Mode: Pulse Width High | tLRCKH | tBCK-60 | - | 1/fs - tBCK | Ns | |
| Except DSP Mode: Duty Cycle | Duty | 45 | - | 55 | % | |
| BICK Input Timing | | | | | | |
| Period | tBCK | 312.5 | - | - | ns | |
| Pulse Width Low | tBCKL | 130 | - | - | ns | |
| Pulse Width High | tBCKH | 130 | - | - | ns | |

| Parameter | Symbol | Min | typ | max | Units | |
|---|----------------|-----------------|------------|-----------------|--------|-----|
| External Master Mode | | | | | | |
| MCKI Input Timing | | | | | | |
| Frequency | 256fs | fCLK | 1.8816 | - | 12.288 | MHz |
| | 512fs | fCLK | 3.7632 | - | 13.312 | MHz |
| | 1024fs | fCLK | 7.5264 | - | 13.312 | MHz |
| Pulse Width Low | tCLKL | 0.4/fCLK | - | - | Ns | |
| Pulse Width High | tCLKH | 0.4/fCLK | - | - | Ns | |
| LRCK Output Timing | | | | | | |
| Frequency | fs | 7.35 | - | 48 | kHz | |
| DSP Mode: Pulse Width High | tLRCKH | - | tBCK | - | ns | |
| Except DSP Mode: Duty Cycle | Duty | - | 50 | - | % | |
| BICK Output Timing | | | | | | |
| Period | BCKO bit = "0" | tBCK | - | 1/(32fs) | - | ns |
| | BCKO bit = "1" | tBCK | - | 1/(64fs) | - | ns |
| Duty Cycle | dBCK | - | 50 | - | % | |
| Audio Interface Timing (DSP Mode) | | | | | | |
| Master Mode | | | | | | |
| LRCK "↑" to BICK "↑" (Note 30) | tDBF | 0.5 x tBCK - 40 | 0.5 x tBCK | 0.5 x tBCK + 40 | ns | |
| LRCK "↑" to BICK "↓" (Note 31) | tDBF | 0.5 x tBCK - 40 | 0.5 x tBCK | 0.5 x tBCK + 40 | ns | |
| BICK "↑" to SDTO (BCKP bit = "0") | tBSD | -70 | - | 70 | ns | |
| BICK "↓" to SDTO (BCKP bit = "1") | tBSD | -70 | - | 70 | ns | |
| SDTI Hold Time | tSDH | 50 | - | - | ns | |
| SDTI Setup Time | tSDS | 50 | - | - | ns | |
| Slave Mode | | | | | | |
| LRCK "↑" to BICK "↑" (Note 30) | tLRB | 0.4 x tBCK | - | - | ns | |
| LRCK "↑" to BICK "↓" (Note 31) | tLRB | 0.4 x tBCK | - | - | ns | |
| BICK "↑" to LRCK "↑" (Note 30) | tBLR | 0.4 x tBCK | - | - | ns | |
| BICK "↓" to LRCK "↑" (Note 31) | tBLR | 0.4 x tBCK | - | - | ns | |
| BICK "↑" to SDTO (BCKP bit = "0") | tBSD | - | - | 80 | ns | |
| BICK "↓" to SDTO (BCKP bit = "1") | tBSD | - | - | 80 | ns | |
| SDTI Hold Time | tSDH | 50 | - | - | ns | |
| SDTI Setup Time | tSDS | 50 | - | - | ns | |
| Audio Interface Timing (Right/Left justified & I²S) | | | | | | |
| Master Mode | | | | | | |
| BICK "↓" to LRCK Edge (Note 30) | tMBLR | -40 | - | 40 | ns | |
| LRCK Edge to SDTO (MSB) (Except I ² S mode) | tLRD | -70 | - | 70 | ns | |
| BICK "↓" to SDTO | tBSD | -70 | - | 70 | ns | |
| SDTI Hold Time | tSDH | 50 | - | - | ns | |
| SDTI Setup Time | tSDS | 50 | - | - | ns | |
| Slave Mode | | | | | | |
| LRCK Edge to BICK "↑" (Note 31) | tLRB | 50 | - | - | ns | |
| BICK "↑" to LRCK Edge (Note 32) | tBLR | 50 | - | - | ns | |
| LRCK Edge to SDTO (MSB) (Except I ² S mode) | tLRD | - | - | 80 | ns | |
| BICK "↓" to SDTO | tBSD | - | - | 80 | ns | |
| SDTI Hold Time | tSDH | 50 | - | - | ns | |
| SDTI Setup Time | tSDS | 50 | - | - | ns | |

Note 30. MSBS, BCKP bits = "00" or "11".

Note 31. MSBS, BCKP bits = "01" or "10".

Note 32. BICK rising edge must not occur at the same time as LRCK edge.

| Parameter | Symbol | min | typ | max | Units |
|---|---------|-----|------|-----|-------|
| Control Interface Timing (I²C Bus mode) (Note 33) | | | | | |
| SCL Clock Frequency | fSCL | - | - | 400 | KHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | - | - | μs |
| Start Condition Hold Time (prior to first clock pulse) | tHD:STA | 0.6 | - | - | μs |
| Clock Low Time | tLOW | 1.3 | - | - | μs |
| Clock High Time | tHIGH | 0.6 | - | - | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | - | - | μs |
| SDA Hold Time from SCL Falling (Note 34) | tHD:DAT | 0 | - | - | μs |
| SDAA, SDAT Setup Time from SCL Rising | tSU:DAT | 0.1 | - | - | μs |
| Rise Time of Both SDA and SCL Lines | tR | - | - | 0.3 | μs |
| Fall Time of Both SDA and SCL Lines | tF | - | - | 0.3 | μs |
| Setup Time for Stop Condition | tSU:STO | 0.6 | - | - | μs |
| Capacitive Load on Bus | Cb | - | - | 400 | pF |
| Pulse Width of Spike Noise Suppressed by Input Filter | tSP | 0 | - | 50 | ns |
| Power-down & Reset Timing | | | | | |
| PDN Pulse Width (Note 35) | tPD | 150 | - | - | ns |
| PMADL or PMADR “↑” to SDTO valid (Note 36) | tPDV | - | 1059 | - | 1/fs |

Note 33. I²C is a registered trademark of Philips Semiconductors.

Note 34. Data must be held long enough to bridge the 300ns-transition time of SCL.

Note 35. The AK4673 can be reset by the PDN pin = “L”.

Note 36. This is the count of LRCK “↑” from the PMADL or PMADR bit = “1”.

■ Timing Diagram

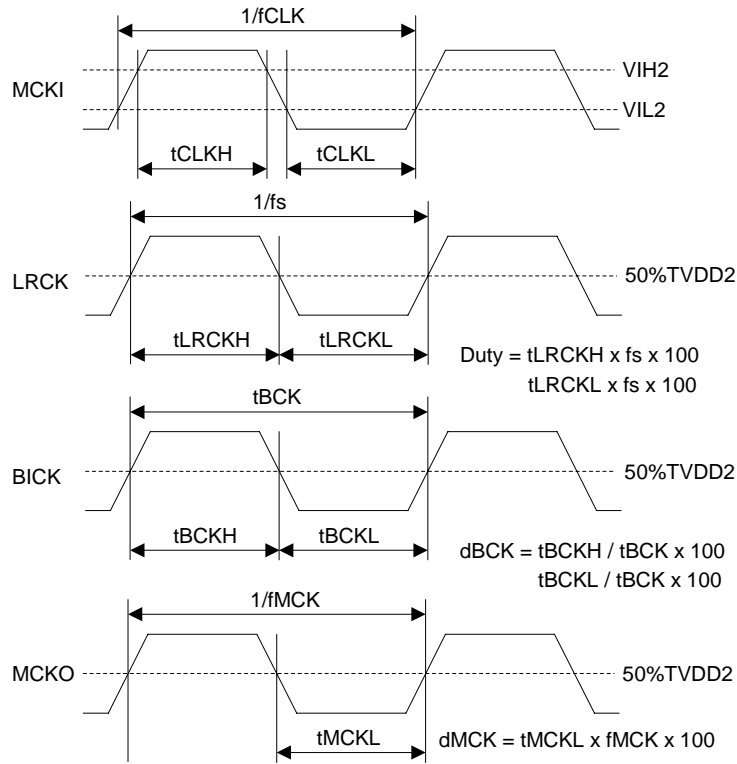


Figure 3. Clock Timing (PLL/EXT Master mode)
 Note 37. MCKO is not available at EXT Master mode.

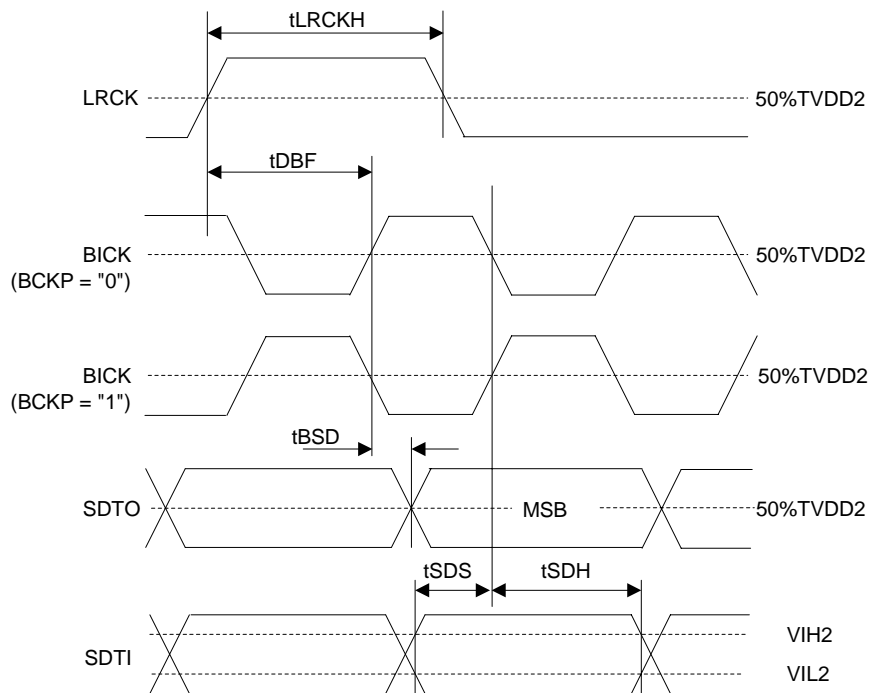


Figure 4. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = "0")

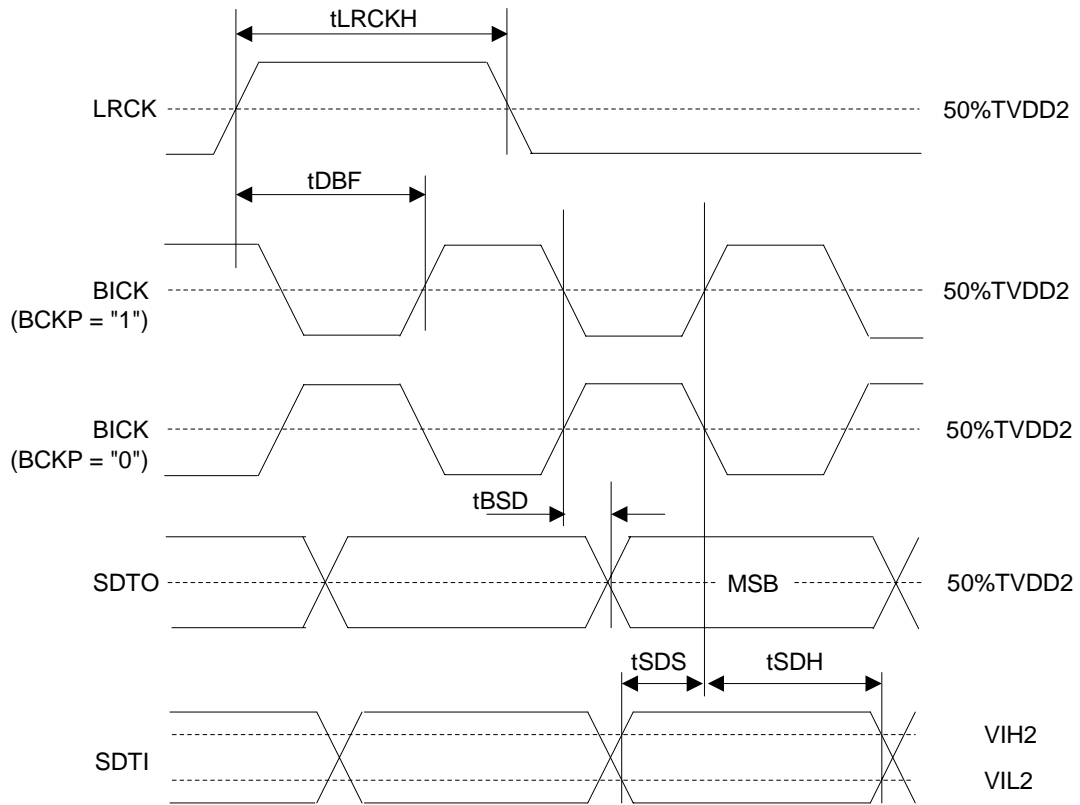


Figure 5. Audio Interface Timing (PLL/EXT Master mode, DSP mode, MSBS = "1")

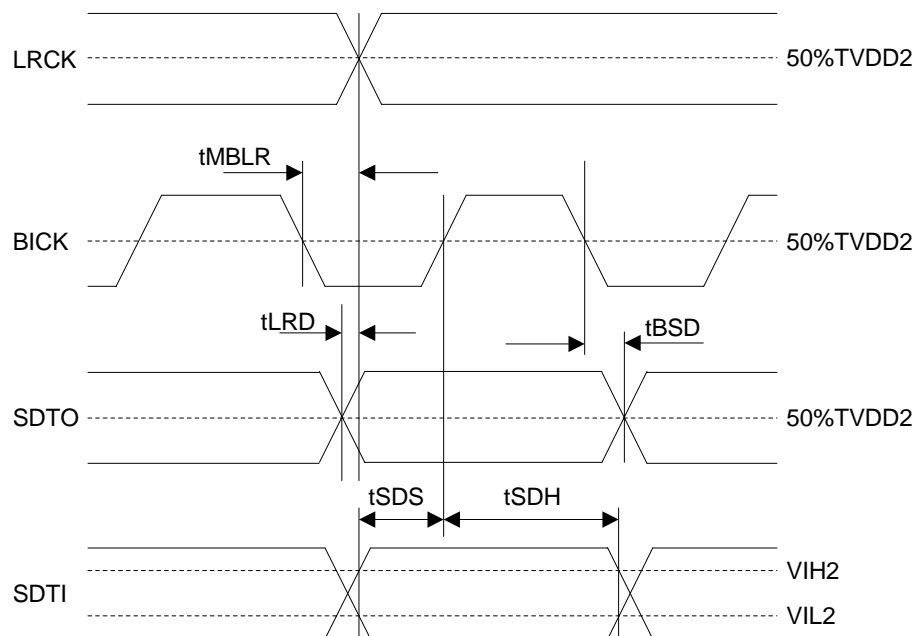


Figure 6. Audio Interface Timing (PLL/EXT Master mode, Except DSP mode)

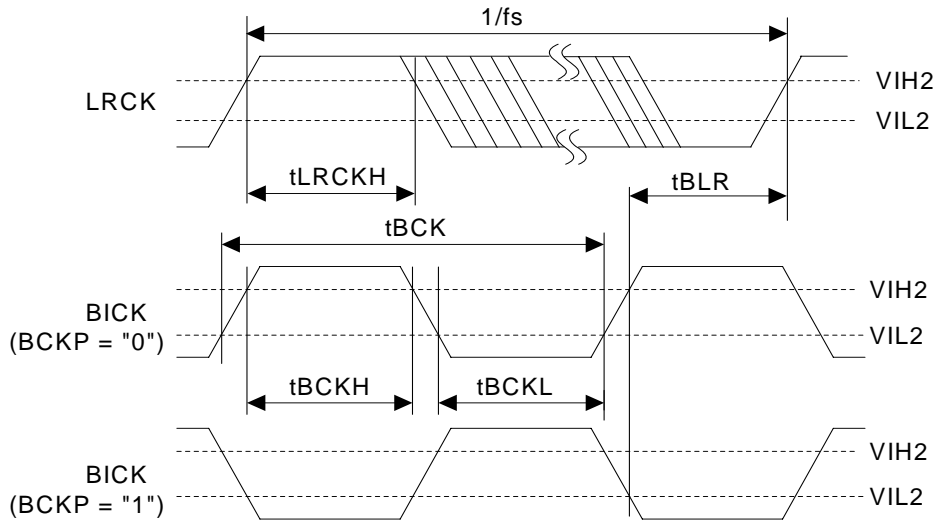


Figure 7. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = "0")

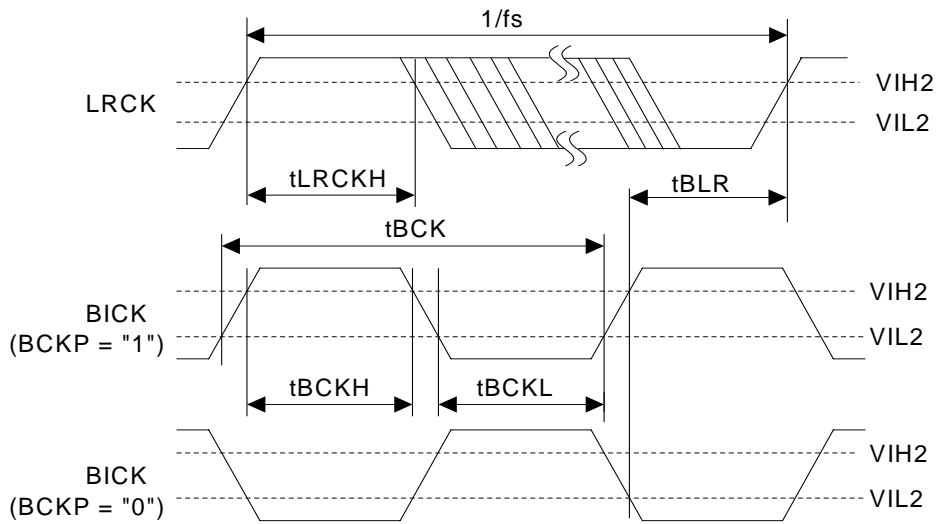


Figure 8. Clock Timing (PLL Slave mode; PLL Reference Clock = LRCK or BICK pin, DSP mode, MSBS = "1")

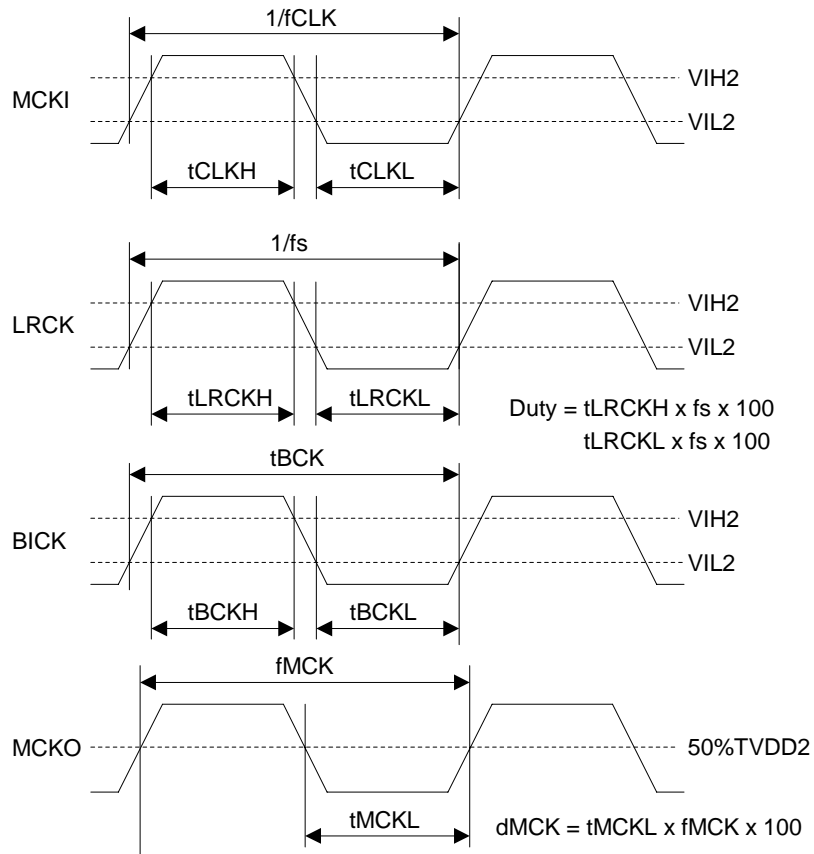


Figure 9. Clock Timing (PLL Slave mode, Except DSP mode)

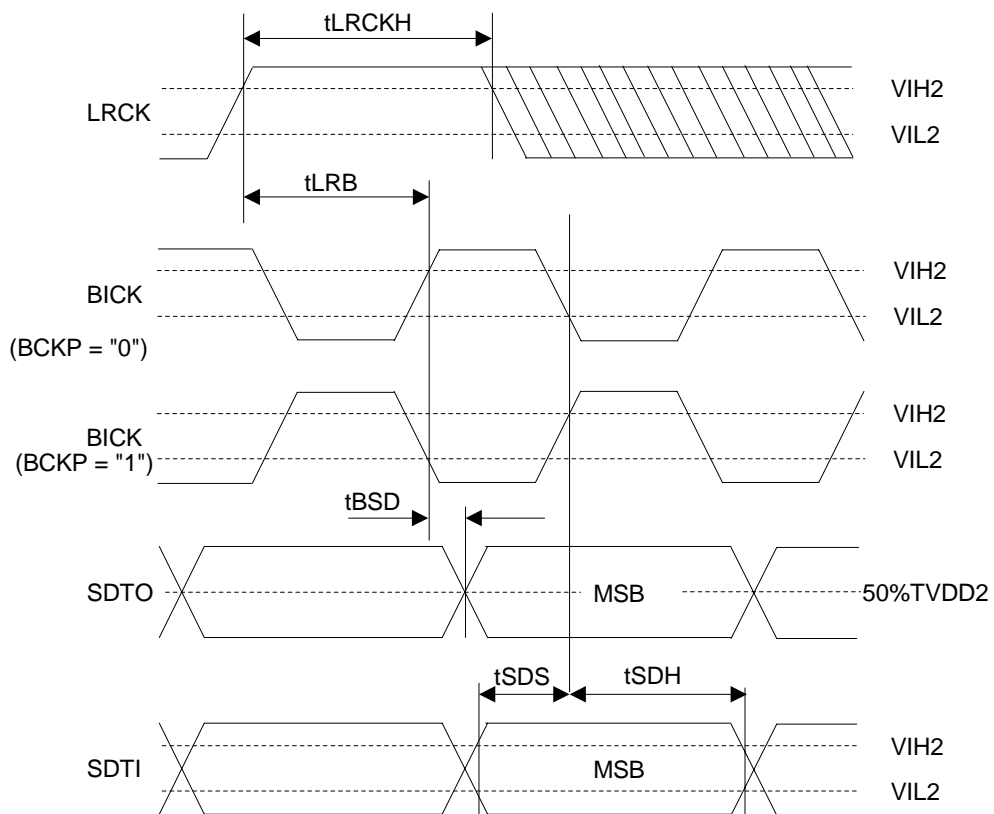


Figure 10. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS = "0")

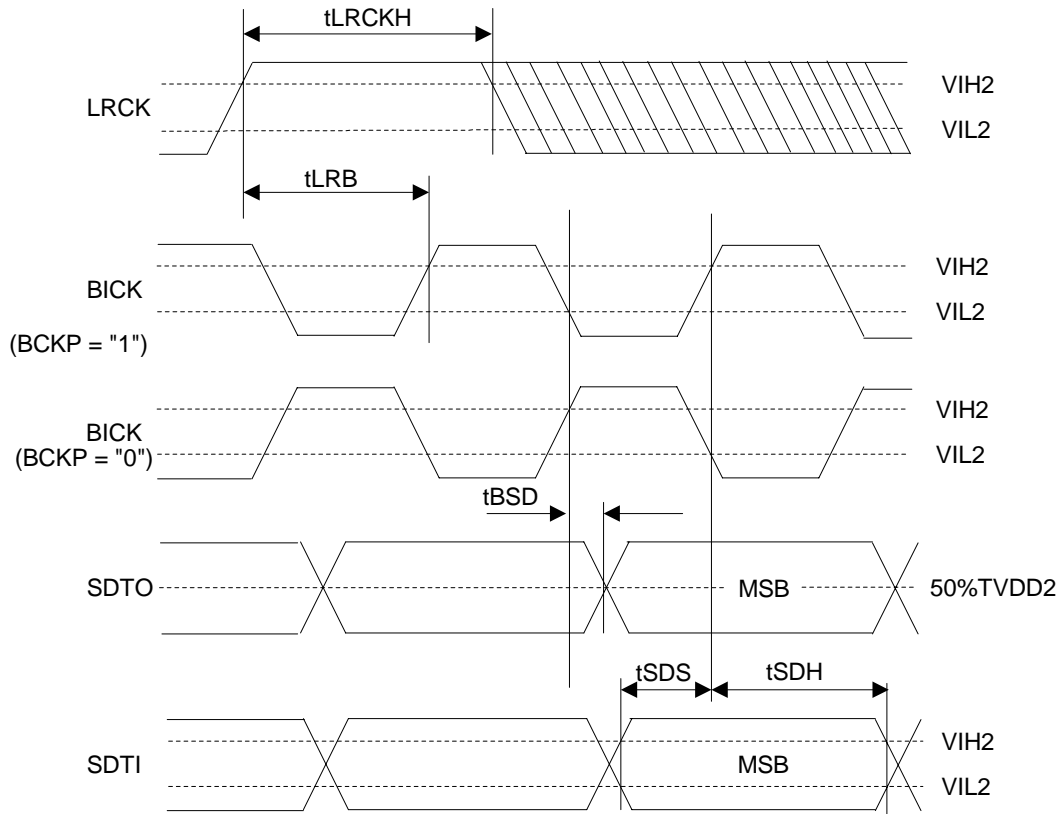


Figure 11. Audio Interface Timing (PLL Slave mode, DSP mode, MSBS = "1")

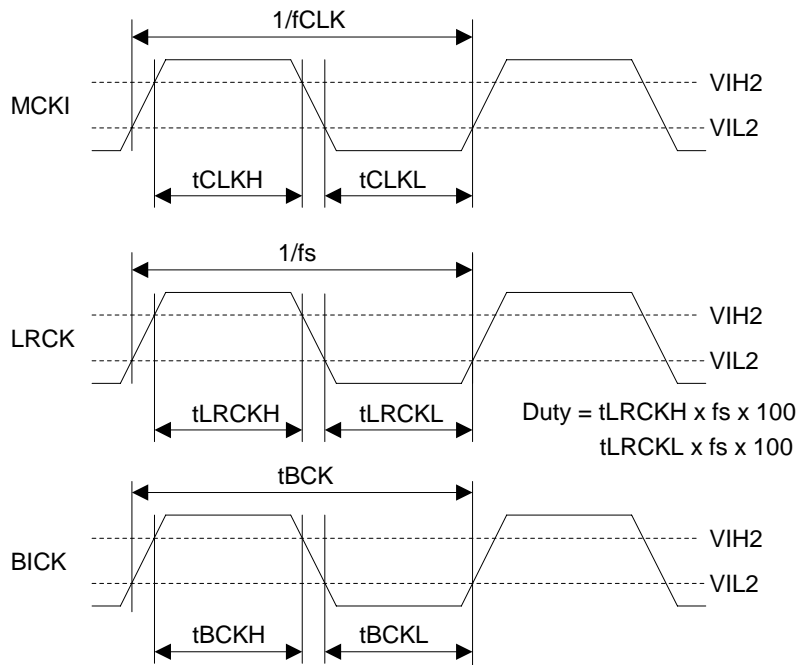


Figure 12. Clock Timing (EXT Slave mode)

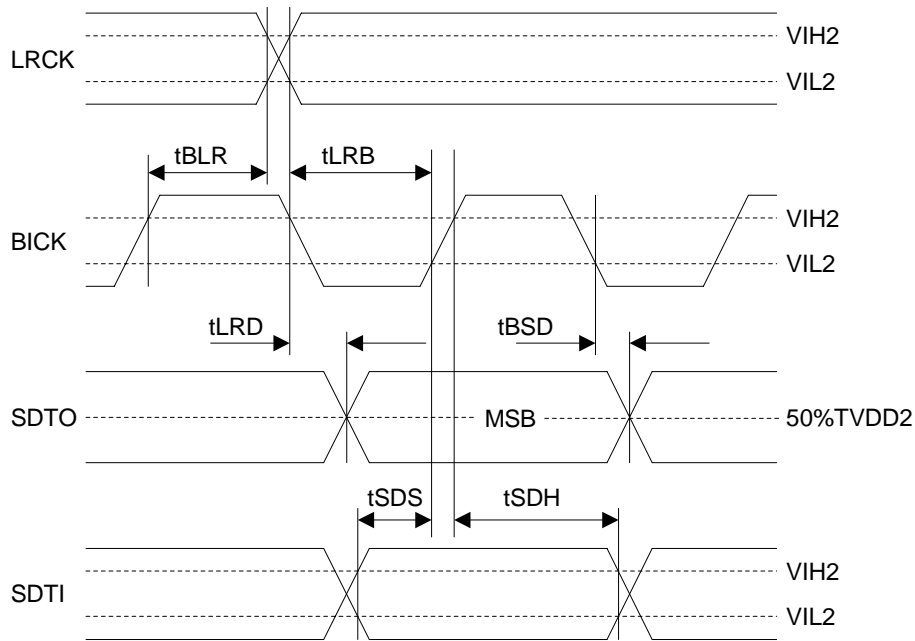
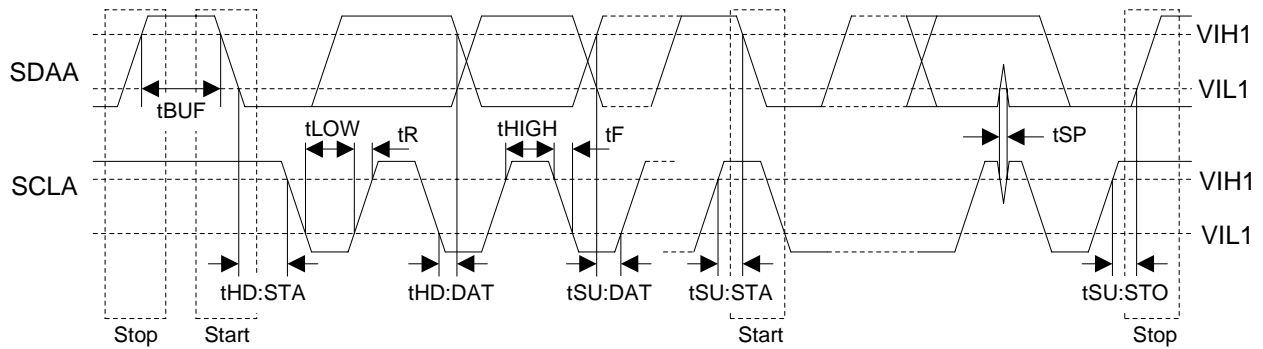
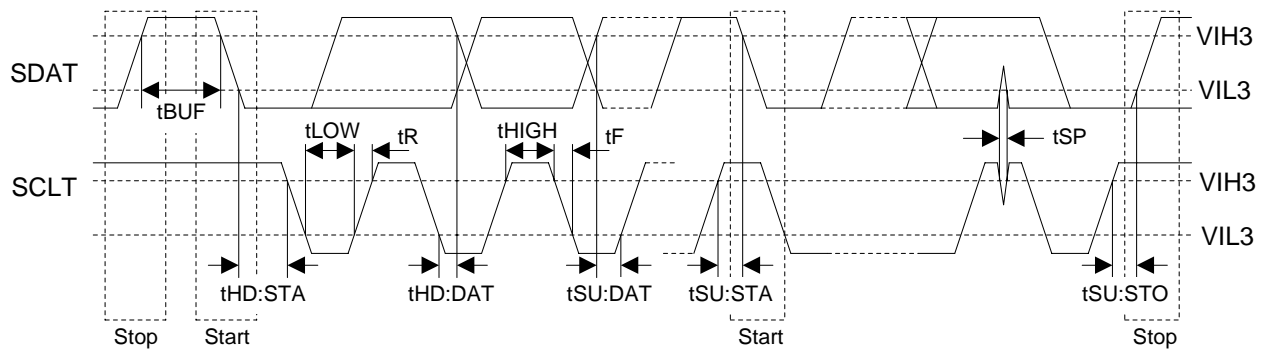


Figure 13. Audio Interface Timing (PLL/EXT Slave mode, Except DSP mode)


 Figure 14. I²C Bus Mode Timing (Audio)

 Figure 15. I²C Bus Mode Timing (TSC)

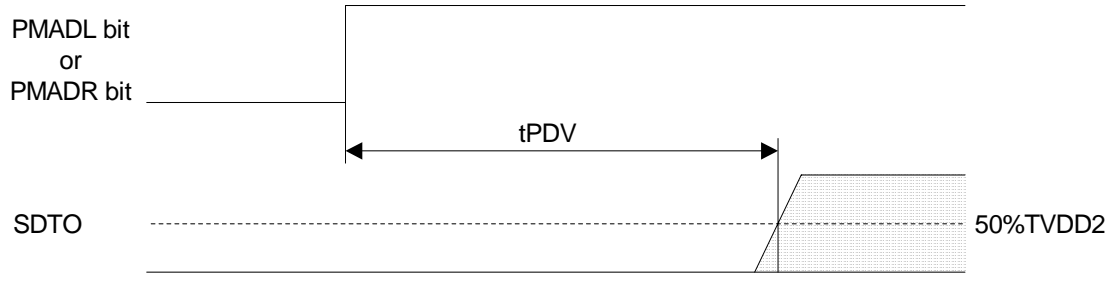


Figure 16. Power Down & Reset Timing 1

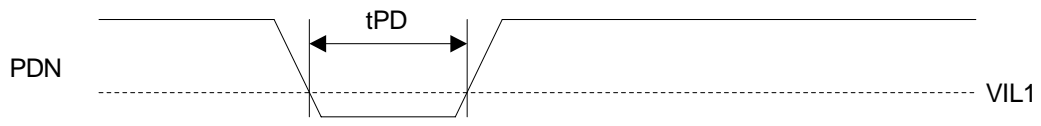


Figure 17. Power Down & Reset Timing 2

AUDIO OPERATION OVERVIEW

■ System Clock

There are the following four clock modes to interface with external devices (Table 2 and Table 3).

| Mode | PMPLL bit | M/S bit | PLL3-0 bits | Figure |
|---|-----------|---------|-------------|------------------------|
| PLL Master Mode (Note 38) | 1 | 1 | See Table 5 | Figure 18 |
| PLL Slave Mode 1 (PLL Reference Clock: MCKI pin) | 1 | 0 | See Table 5 | Figure 19 |
| PLL Slave Mode 2 (PLL Reference Clock: LRCK or BICK pin) | 1 | 0 | See Table 5 | Figure 20 Figure 21 |
| EXT Slave Mode | 0 | 0 | x | Figure 22 |
| EXT Master Mode | 0 | 1 | x | Figure 23 |

Note 38. If M/S bit = “1”, PMPLL bit = “0” and MCKO bit = “1” during the setting of PLL Master Mode, the invalid clocks are output from MCKO pin when MCKO bit is “1”.

Table 2. Clock Mode Setting (x: Don't care)

| Mode | MCKO bit | MCKO pin | MCKI pin | BICK pin | LRCK pin |
|---|----------|---------------------------|----------------------------|---------------------------------------|-----------------|
| PLL Master Mode | 0 | “L” | Selected by PLL3-0 bits | Output (Selected by BCKO bit) | Output (1fs) |
| | 1 | Selected by PS1-0 bits | | | |
| PLL Slave Mode (PLL Reference Clock: MCKI pin) | 0 | “L” | Selected by PLL3-0 bits | Input (≥ 32fs) | Input (1fs) |
| | 1 | Selected by PS1-0 bits | | | |
| PLL Slave Mode (PLL Reference Clock: LRCK or BICK pin) | 0 | “L” | GND | Input (Selected by PLL3-0 bits) | Input (1fs) |
| EXT Slave Mode | 0 | “L” | Selected by FS1-0 bits | Input (≥ 32fs) | Input (1fs) |
| EXT Master Mode | 0 | “L” | Selected by FS1-0 bits | Output (Selected by BCKO bit) | Output (1fs) |

Table 3. Clock pins state in Clock Mode

■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = “1” selects master mode and “0” selects slave mode. When the AK4673 is power-down mode (PDN pin = “L”) and exits reset state, the AK4673 is slave mode. After exiting reset state, the AK4673 goes to master mode by changing M/S bit = “1”.

When the AK4673 is used in master mode, LRCK and BICK pins are a floating state until M/S bit becomes “1”. LRCK and BICK pins of the AK4673 should be pulled-down or pulled-up by the resistor (about 100kΩ) externally to avoid the floating state.

| M/S bit | Mode |
|---------|-------------|
| 0 | Slave Mode |
| 1 | Master Mode |

(default)

Table 4. Select Master/Slave Mode

■ PLL Mode (AIN3 bit = “0”, PMPLL bit = “1”)

When PMPLL bit is “1”, a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time, when the AK4673 is supplied stable clocks after PLL is powered-up (PMPLL bit = “0” → “1”) or sampling frequency changes is shown in [Table 5](#). When AIN3 bit = “1”, the PLL is not available.

1) Setting of PLL Mode

| Mode | PLL3 bit | PLL2 bit | PLL1 bit | PLL0 bit | PLL Reference Clock Input Pin | Input Frequency | R and C of VCOC pin | | PLL Lock Time (max) |
|--------|----------|----------|----------|----------|-------------------------------|-----------------|---------------------|------|---------------------|
| | | | | | | | R[Ω] | C[F] | |
| 0 | 0 | 0 | 0 | 0 | LRCK pin | 1fs | 6.8k | 220n | 160ms |
| 2 | 0 | 0 | 1 | 0 | BICK pin | 32fs | 10k | 4.7n | 2ms |
| | | | | | | | 10k | 10n | 4ms |
| 3 | 0 | 0 | 1 | 1 | BICK pin | 64fs | 10k | 4.7n | 2ms |
| | | | | | | | 10k | 10n | 4ms |
| 4 | 0 | 1 | 0 | 0 | MCKI pin | 11.2896MHz | 10k | 4.7n | 40ms |
| 5 | 0 | 1 | 0 | 1 | MCKI pin | 12.288MHz | 10k | 4.7n | 40ms |
| 6 | 0 | 1 | 1 | 0 | MCKI pin | 12MHz | 10k | 4.7n | 40ms |
| 7 | 0 | 1 | 1 | 1 | MCKI pin | 24MHz | 10k | 4.7n | 40ms |
| 8 | 1 | 0 | 0 | 0 | MCKI pin | 19.2MHz | 10k | 4.7n | 40ms |
| 12 | 1 | 1 | 0 | 0 | MCKI pin | 13.5MHz | 10k | 10n | 40ms |
| 13 | 1 | 1 | 0 | 1 | MCKI pin | 27MHz | 10k | 10n | 40ms |
| 14 | 1 | 1 | 1 | 0 | MCKI pin | 13MHz | 10k | 220n | 60ms |
| 15 | 1 | 1 | 1 | 1 | MCKI pin | 26MHz | 10k | 220n | 60ms |
| Others | Others | | | N/A | | | | | |

Table 5. Setting of PLL Mode (*fs: Sampling Frequency, N/A: Not available)

2) Setting of sampling frequency in PLL Mode

When PLL reference clock input is MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in [Table 6](#).

| Mode | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency |
|--------|---------|---------|---------|---------|--------------------|
| 0 | 0 | 0 | 0 | 0 | 8kHz |
| 1 | 0 | 0 | 0 | 1 | 12kHz |
| 2 | 0 | 0 | 1 | 0 | 16kHz |
| 3 | 0 | 0 | 1 | 1 | 24kHz |
| 4 | 0 | 1 | 0 | 0 | 7.35kHz |
| 5 | 0 | 1 | 0 | 1 | 11.025kHz |
| 6 | 0 | 1 | 1 | 0 | 14.7kHz |
| 7 | 0 | 1 | 1 | 1 | 22.05kHz |
| 10 | 1 | 0 | 1 | 0 | 32kHz |
| 11 | 1 | 0 | 1 | 1 | 48kHz |
| 14 | 1 | 1 | 1 | 0 | 29.4kHz |
| 15 | 1 | 1 | 1 | 1 | 44.1kHz |
| Others | Others | | | | N/A |

Table 6. Setting of Sampling Frequency at PMPLL bit = “1” (Reference Clock = MCKI pin) (N/A: Not available)

When PLL reference clock input is LRCK or BICK pin, the sampling frequency is selected by FS3 and FS1-0 bits. (Table 7). **FS2 bit is “don’t care”.**

| Mode | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency Range |
|--------|---------|---------|---------|---------|--------------------------|
| 0 | 0 | x | 0 | 0 | 7.35kHz ≤ fs ≤ 8kHz |
| 1 | 0 | x | 0 | 1 | 8kHz < fs ≤ 12kHz |
| 2 | 0 | x | 1 | 0 | 12kHz < fs ≤ 16kHz |
| 3 | 0 | x | 1 | 1 | 16kHz < fs ≤ 24kHz |
| 6 | 1 | x | 1 | 0 | 24kHz < fs ≤ 32kHz |
| 7 | 1 | x | 1 | 1 | 32kHz < fs ≤ 48kHz |
| Others | Others | | | | N/A |

(x: Don’t care, N/A: Not available)

Table 7. Setting of Sampling Frequency at PMPLL bit = “1” (Reference Clock = LRCK or BICK pin)

■ PLL Unlock State

1) PLL Master Mode (AIN3 bit = “0”; PMPLL bit = “1”, M/S bit = “1”)

In this mode, LRCK and BICK pins go to “L” and irregular frequency clock is output from the MCKO pins at MCKO bit is “1” before the PLL goes to lock state after PMPLL bit = “0” → “1”. If MCKO bit is “0”, the MCKO pin goes to “L” (Table 8).

After the PLL is locked, a first period of LRCK and BICK may be invalid clock, but these clocks return to normal state after a period of 1/fs.

When sampling frequency is changed, BICK and LRCK pins do not output irregular frequency clocks but go to “L” by setting PMPLL bit to “0”.

| PLL State | MCKO pin | | BICK pin | LRCK pin |
|--------------------------------|----------------|----------------|--------------|------------|
| | MCKO bit = “0” | MCKO bit = “1” | | |
| After that PMPLL bit “0” → “1” | “L” Output | Invalid | “L” Output | “L” Output |
| PLL Unlock (except above case) | “L” Output | Invalid | Invalid | Invalid |
| PLL Lock | “L” Output | See Table 10 | See Table 11 | 1fs Output |

Table 8. Clock Operation at PLL Master Mode (PMPLL bit = “1”, M/S bit = “1”)

2) PLL Slave Mode (AIN3 bit = “0”, PMPLL bit = “1”, M/S bit = “0”)

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = “0” → “1”. Then, the clock selected by Table 10 is output from the MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. For DAC, the output signal should be muted by writing “0” to DACL and DACH bits.

| PLL State | MCKO pin | |
|--------------------------------|----------------|----------------|
| | MCKO bit = “0” | MCKO bit = “1” |
| After that PMPLL bit “0” → “1” | “L” Output | Invalid |
| PLL Unlock | “L” Output | Invalid |
| PLL Lock | “L” Output | Output |

Table 9. Clock Operation at PLL Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

■ **PLL Master Mode (AIN3 bit = “0”, PMPLL bit = “1”, M/S bit = “1”)**

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz or 27MHz) is input to the MCKI pin, MCKO, BICK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (Table 10) and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit (Table 11).

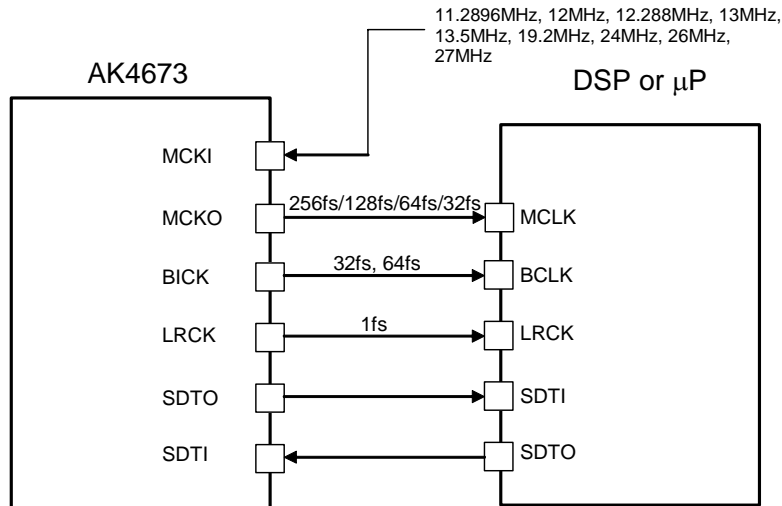


Figure 18. PLL Master Mode

| Mode | PS1 bit | PS0 bit | MCKO pin |
|------|---------|---------|----------|
| 0 | 0 | 0 | 256fs |
| 1 | 0 | 1 | 128fs |
| 2 | 1 | 0 | 64fs |
| 3 | 1 | 1 | 32fs |

(default)

Table 10. MCKO Output Frequency (PLL Mode, MCKO bit = “1”)

| BCKO bit | BICK Output Frequency |
|----------|-----------------------|
| 0 | 32fs |
| 1 | 64fs |

(default)

Table 11. BICK Output Frequency at Master Mode

■ **PLL Slave Mode (AIN3 bit = “0”, PMPLL bit = “1”, M/S bit = “0”)**

A reference clock of PLL is selected among the input clocks to the MCKI, BICK or LRCK pin. The required clock to the AK4673 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 5).

a) PLL reference clock: MCKI pin

BICK and LRCK inputs should be synchronized with MCKO output. The phase between MCKO and LRCK dose not matter. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 10) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 6).

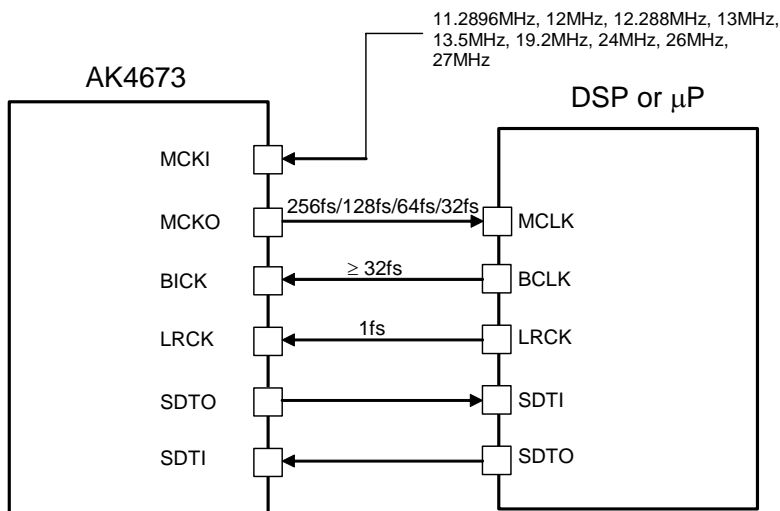


Figure 19. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

b) PLL reference clock: BICK or LRCK pin

Sampling frequency corresponds to 7.35kHz to 48kHz by changing FS3-0 bits (Table 7)

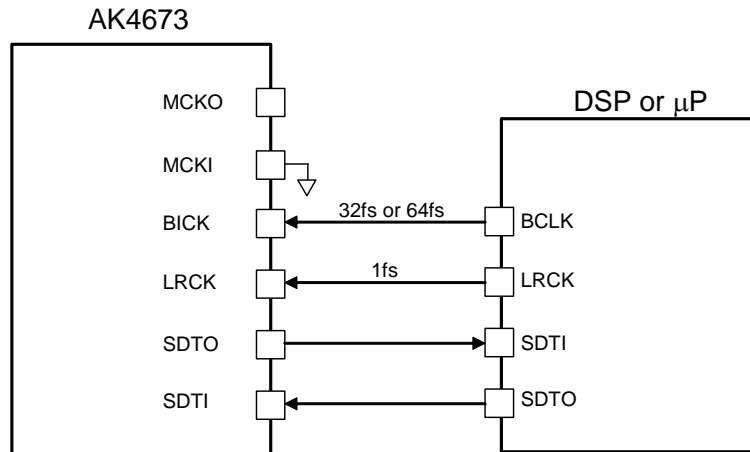


Figure 20. PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

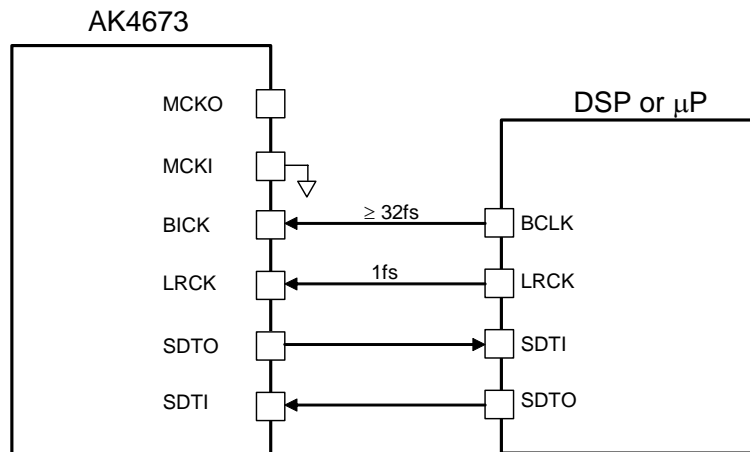


Figure 21. PLL Slave Mode 2 (PLL Reference Clock: LRCK pin)

The external clocks (MCKI, BICK and LRCK) should always be present whenever the ADC or DAC is in operation (PMADL bit = “1”, PMADR bit = “1” or PMDAC bit = “1”). If these clocks are not provided, the AK4673 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAC bits = “0”).

■ EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”)

When PMPLL bit is “0”, the AK4673 becomes EXT mode. The master clock is input from the MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of a normal audio CODEC. The clocks required to operate the AK4673 are MCKI (256fs, 512fs or 1024fs), LRCK (fs) and BICK (≥ 32 fs). The master clock (MCKI) should be synchronized with LRCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by FS1-0 bits (Table 12).

| Mode | FS3-2 bits | FS1 bit | FS0 bit | MCKI Input Frequency | Sampling Frequency Range |
|------|------------|---------|---------|----------------------|--------------------------|
| 0 | x | 0 | 0 | 256fs | 7.35kHz ~ 48kHz |
| 1 | x | 0 | 1 | 1024fs | 7.35kHz ~ 13kHz |
| 2 | x | 1 | 0 | 256fs | 7.35kHz ~ 48kHz |
| 3 | x | 1 | 1 | 512fs | 7.35kHz ~ 26kHz |

Table 12. MCKI Frequency at EXT Slave Mode (PMPLL bit = “0”, M/S bit = “0”) (x: Don’t care)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins at fs=8kHz is shown in Table 13.

| MCKI | S/N (fs=8kHz, 20kHzLPF + A-weighted) |
|--------|---|
| 256fs | 83dB |
| 512fs | 93dB |
| 1024fs | 93dB |

Table 13. Relationship between MCKI and S/N of LOUT/ROUT pins

The external clocks (MCKI, BICK and LRCK) should always be present whenever the ADC or DAC is in operation (PMADL bit = “1”, PMADR bit = “1” or PMDAC bit = “1”). If these clocks are not provided, the AK4673 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAC bits = “0”).

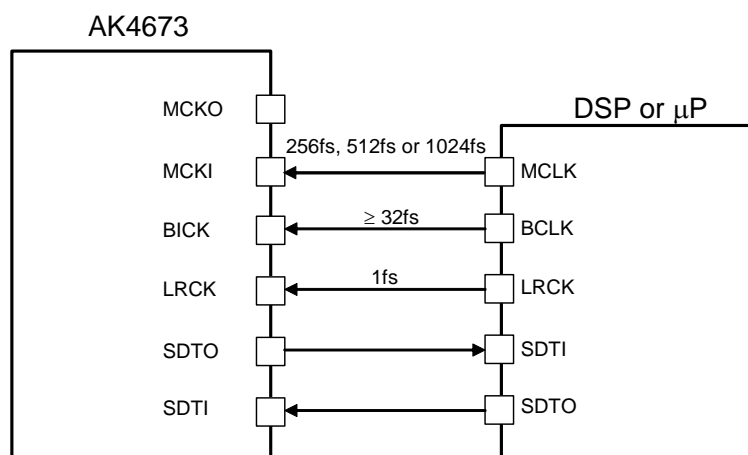


Figure 22. EXT Slave Mode

■ EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”)

The AK4673 becomes EXT master mode by setting PMPLL bit = “0” and M/S bit = “1”. Master clock is input from MCKI pin, the internal PLL circuit is not operated. The clock required to operate is MCKI (256fs, 512fs or 1024fs). The input frequency of MCKI is selected by FS1-0 bits (Table 14).

| Mode | FS3-2 bits | FS1 bit | FS0 bit | MCKI Input Frequency | Sampling Frequency Range | (default) |
|------|------------|---------|---------|----------------------|--------------------------|-----------|
| 0 | x | 0 | 0 | 256fs | 7.35kHz ~ 48kHz | |
| 1 | x | 0 | 1 | 1024fs | 7.35kHz ~ 13kHz | |
| 2 | x | 1 | 0 | 256fs | 7.35kHz ~ 48kHz | |
| 3 | x | 1 | 1 | 512fs | 7.35kHz ~ 26kHz | |

Table 14. MCKI Frequency at EXT Master Mode (PMPLL bit = “0”, M/S bit = “1”) (x: Don’t care)

The S/N of the DAC at low sampling frequencies is worse than at high sampling frequencies due to out-of-band noise. The out-of-band noise can be reduced by using higher frequency of the master clock. The S/N of the DAC output through LOUT/ROUT pins at fs=8kHz is shown in Table 15.

| MCKI | S/N (fs=8kHz, 20kHzLPF + A-weighted) |
|--------|---|
| 256fs | 83dB |
| 512fs | 93dB |
| 1024fs | 93dB |

Table 15. Relationship between MCKI and S/N of LOUT/ROUT pins

MCKI should always be present whenever the ADC or DAC is in operation (PMADL bit = “1”, PMADR bit = “1” or PMDAC bit = “1”). If MCKI is not provided, the AK4673 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC and DAC should be in the power-down mode (PMADL=PMADR=PMDAC bits = “0”).

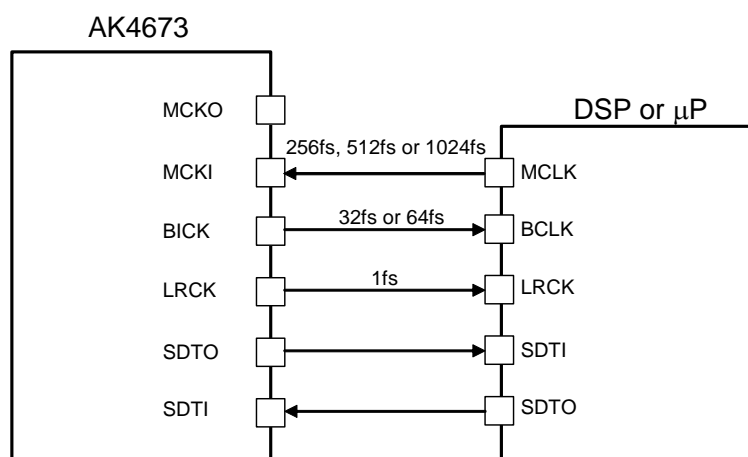


Figure 23. EXT Master Mode

| BCKO bit | BICK Output Frequency | (default) |
|----------|-----------------------|-----------|
| 0 | 32fs | |
| 1 | 64fs | |

Table 16. BICK Output Frequency at Master Mode

■ System Reset

When power-up, the AK4673 should be reset by bringing the PDN pin = “L”. This ensures that all internal registers reset to their initial values.

The ADC enters an initialization cycle when the PMADL or PMADR bit is changed from “0” to “1” at PMDAC bits is “0”. The initialization cycle time is $1059/fs=24ms@fs=44.1kHz$. During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2’s compliment, “0”. The ADC output reflects the analog input signal after the initialization cycle is complete. When PMDAC bit is “1”, the ADC does not require an initialization cycle.

The DAC enters an initialization cycle when the PMDAC bit is changed from “0” to “1” at PMADL and PMADR bits are “0”. The initialization cycle time is $1059/fs=24ms@fs=44.1kHz$. During the initialization cycle, the DAC input digital data of both channels are internally forced to a 2’s compliment, “0”. The DAC output reflects the digital input data after the initialization cycle is complete. When PMADL or PMADR bit is “1”, the DAC does not require an initialization cycle.

■ Audio Interface Format

Four types of data formats are available and are selected by setting the DIF1-0 bits (Table 17). In all modes, the serial data is MSB first, 2’s complement format. Audio interface formats can be used in both master and slave modes. LRCK and BICK are output from the AK4673 in master mode, but must be input to the AK4673 in slave mode.

| Mode | DIF1 bit | DIF0 bit | SDTO (ADC) | SDTI (DAC) | BICK | Figure |
|------|----------|----------|-----------------------------|-----------------------------|-------------|-----------|
| 0 | 0 | 0 | DSP Mode | DSP Mode | $\geq 32fs$ | Table 18 |
| 1 | 0 | 1 | MSB justified | LSB justified | $\geq 32fs$ | Figure 28 |
| 2 | 1 | 0 | MSB justified | MSB justified | $\geq 32fs$ | Figure 29 |
| 3 | 1 | 1 | I ² S compatible | I ² S compatible | $\geq 32fs$ | Figure 30 |

(default)

Table 17. Audio Interface Format

In Modes 1-3, the SDTO is clocked out on the falling edge (“↓”) of BICK and the SDTI is latched on the rising edge (“↑”).

In Mode 0 (DSP mode), the audio I/F timing is changed by BCKP and MSBS bits (Table 18).

| DIF1 | DIF0 | MSB S | BCKP | Audio Interface Format | Figure |
|------|------|-------|------|--|-----------|
| 0 | 0 | 0 | 0 | MSB of SDTO is output by the rising edge (“↑”) of the first BICK after the rising edge (“↑”) of LRCK. MSB of SDTI is latched by the falling edge (“↓”) of the BICK just after the output timing of SDTO’s MSB. | Figure 24 |
| | | 0 | 1 | MSB of SDTO is output by the falling edge (“↓”) of the first BICK after the rising edge (“↑”) of LRCK. MSB of SDTI is latched by the rising edge (“↑”) of the BICK just after the output timing of SDTO’s MSB. | Figure 25 |
| | | 1 | 0 | MSB of SDTO is output by next rising edge (“↑”) of the falling edge (“↓”) of the first BICK after the rising edge (“↑”) of LRCK. MSB of SDTI is latched by the falling edge (“↓”) of the BICK just after the output timing of SDTO’s MSB. | Figure 26 |
| | | 1 | 1 | MSB of SDTO is output by next falling edge (“↓”) of the rising edge (“↑”) of the first BICK after the rising edge (“↑”) of LRCK. MSB of SDTI is latched by the rising edge (“↑”) of the BICK just after the output timing of SDTO’s MSB. | Figure 27 |

(default)

Table 18. Audio Interface Format in Mode 0

If 16-bit data that ADC outputs is converted to 8-bit data by removing LSB 8-bit, “-1” at 16bit data is converted to “-1” at 8-bit data. And when the DAC playbacks this 8-bit data, “-1” at 8-bit data will be converted to “-256” at 16-bit data and this is a large offset. This offset can be removed by adding the offset of “128” to 16-bit data before converting to 8-bit data.

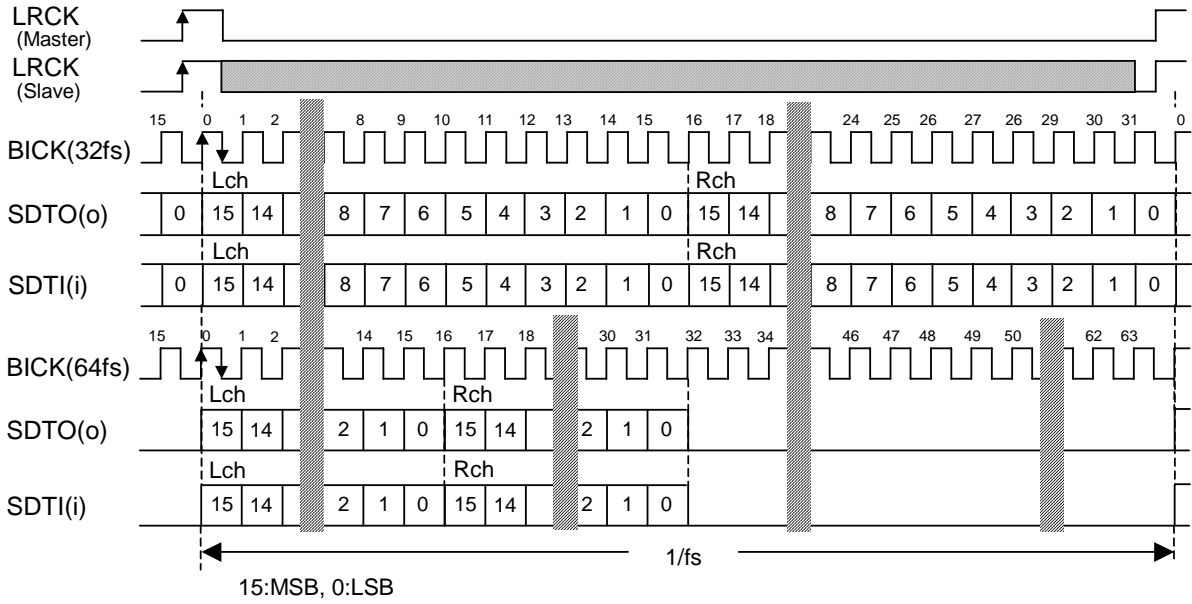


Figure 24. Mode 0 Timing (BCKP = "0", MSBS = "0")

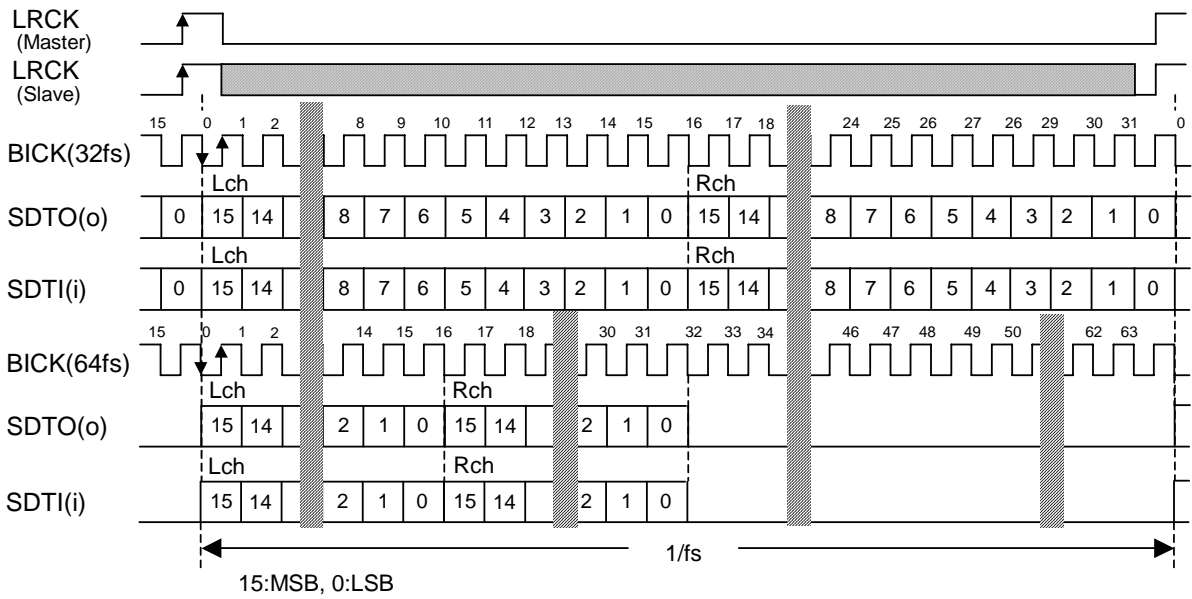


Figure 25. Mode 0 Timing (BCKP = "1", MSBS = "0")

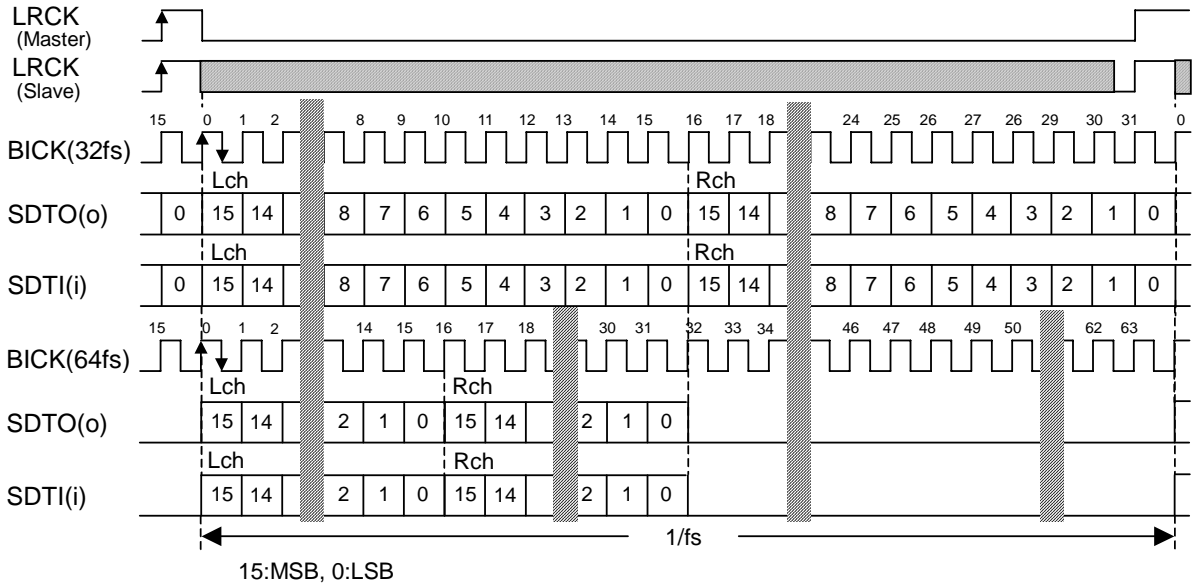


Figure 26. Mode 0 Timing (BCKP = "0", MSBS = "1")

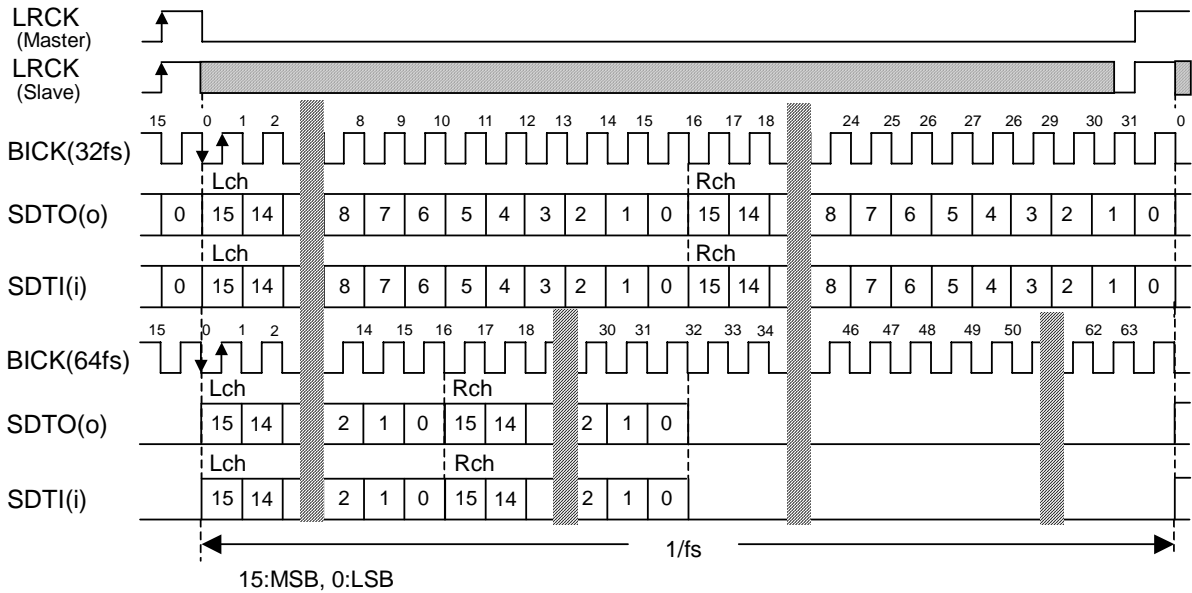


Figure 27. Mode 0 Timing (BCKP = "1", MSBS = "1")

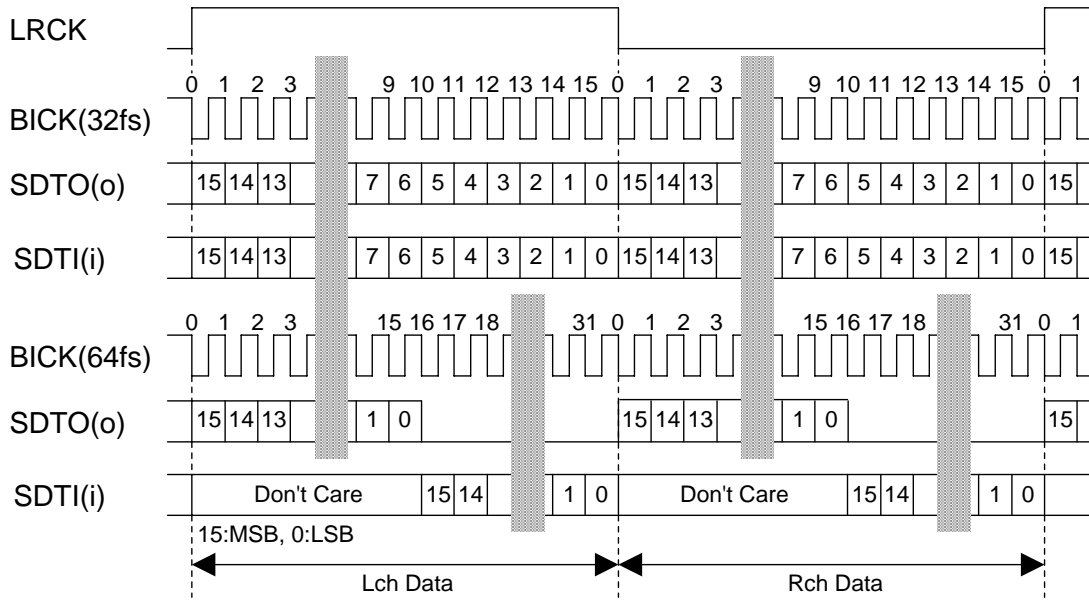


Figure 28. Mode 1 Timing

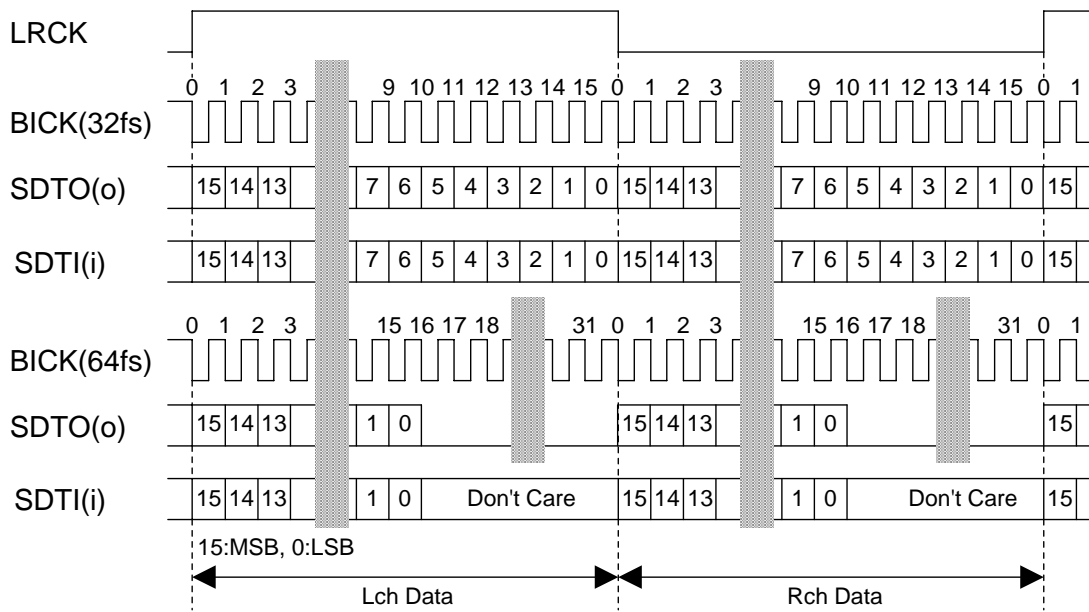


Figure 29. Mode 2 Timing

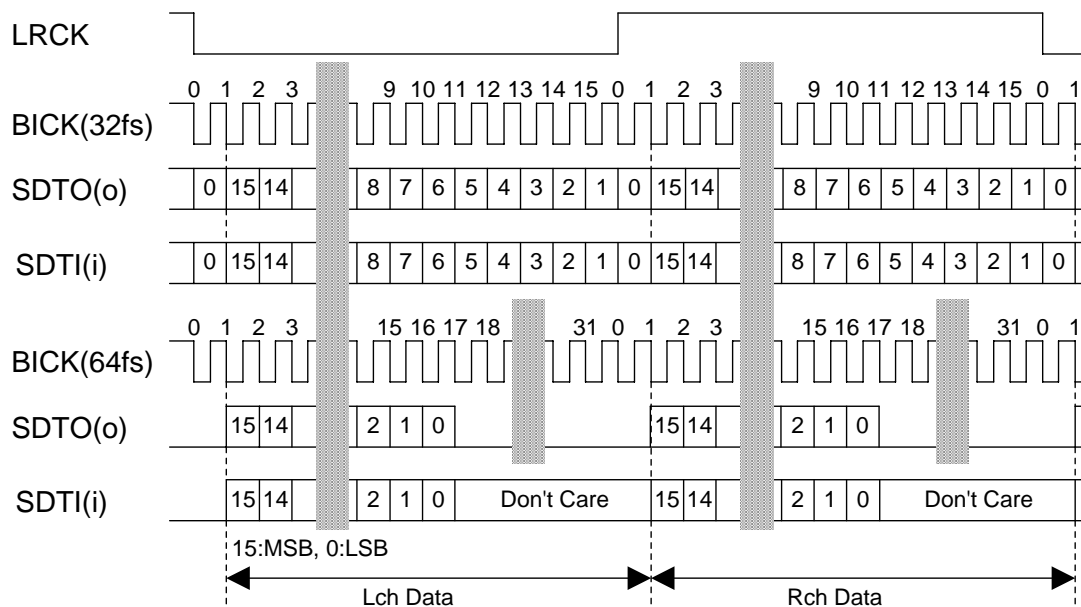


Figure 30. Mode 3 Timing

■ Mono/Stereo Mode

PMADL, PMADR and MIX bits set mono/stereo ADC operation. When MIX bit = "1", EQ and FIL3 bits should be set to "0". ALC operation (ALC bit = "1") or digital volume operation (ALC bit = "0") is applied to the data in [Table 19](#).

| PMADL bit | PMADR bit | MIX bit | ADC Lch data | ADC Rch data | (default) |
|-----------|-----------|---------|------------------|------------------|-----------|
| 0 | 0 | x | All "0" | All "0" | |
| 0 | 1 | x | Rch Input Signal | Rch Input Signal | |
| 1 | 0 | x | Lch Input Signal | Lch Input Signal | |
| 1 | 1 | 0 | Lch Input Signal | Rch Input Signal | |
| | | 1 | (L+R)/2 | (L+R)/2 | |

Table 19. Mono/Stereo ADC operation (x: Don't care)

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 0.9Hz (@fs=44.1kHz) and scales with sampling rate (fs). When PMADL bit = "1" or PMADR bit = "1", the HPF of ADC is enabled but the HPF of DAC is disabled. When PMADL=PMADR bits = "0", PMDAC bit = "1", the HPF of DAC is enabled but the HPF of ADC is disabled.

■ MIC/LINE Input Selector

The AK4673 has input selector for MIC-Amp. When MDIF1 and MDIF2 bits are “0”, INL1-0 and INR1-0 bits select LIN1/LIN2/LIN3/LIN4 and RIN1/RIN2/RIN3/RIN4, respectively. When MDIF1 and MDIF2 bits are “1”, LIN1, RIN1, LIN2 and RIN2 pins become IN1-, IN1+, IN2+ and IN2- pins respectively. In this case, full-differential input is available (Figure 32). When full-differential input is used, the signal should not be input to the pins marked by “X” in Table 21.

| MDIF1 bit | MDIF2 bit | INL1 bit | INL0 bit | INR1 bit | INR0 bit | Lch | Rch | |
|-----------|-----------|----------|----------|----------|----------|--------|--------|-----------|
| 0 | 0 | 0 | 0 | 0 | 0 | LIN1 | RIN1 | (default) |
| 0 | 0 | 0 | 0 | 0 | 1 | LIN1 | RIN2 | |
| 0 | 0 | 0 | 0 | 1 | 0 | LIN1 | RIN3 | |
| 0 | 0 | 0 | 0 | 1 | 1 | LIN1 | RIN4 | |
| 0 | 0 | 0 | 1 | 0 | 0 | LIN2 | RIN1 | |
| 0 | 0 | 0 | 1 | 0 | 1 | LIN2 | RIN2 | |
| 0 | 0 | 0 | 1 | 1 | 0 | LIN2 | RIN3 | |
| 0 | 0 | 0 | 1 | 1 | 1 | LIN2 | RIN4 | |
| 0 | 0 | 1 | 0 | 0 | 0 | LIN3 | RIN1 | |
| 0 | 0 | 1 | 0 | 0 | 1 | LIN3 | RIN2 | |
| 0 | 0 | 1 | 0 | 1 | 0 | LIN3 | RIN3 | |
| 0 | 0 | 1 | 0 | 1 | 1 | LIN3 | RIN4 | |
| 0 | 0 | 1 | 1 | 0 | 0 | LIN4 | RIN1 | |
| 0 | 0 | 1 | 1 | 0 | 1 | LIN4 | RIN2 | |
| 0 | 0 | 1 | 1 | 1 | 0 | LIN4 | RIN3 | |
| 0 | 0 | 1 | 1 | 1 | 1 | LIN4 | RIN4 | |
| 0 | 1 | 0 | 0 | 0 | 0 | LIN1 | IN2+/- | |
| 0 | 1 | 1 | 0 | 0 | 0 | LIN3 | IN2+/- | |
| 0 | 1 | 1 | 1 | 0 | 0 | LIN4 | IN2+/- | |
| 1 | 0 | 0 | 0 | 0 | 1 | IN1+/- | RIN2 | |
| 1 | 0 | 0 | 0 | 1 | 0 | IN1+/- | RIN3 | |
| 1 | 0 | 0 | 0 | 1 | 1 | IN1+/- | RIN4 | |
| 1 | 1 | 0 | 0 | 0 | 0 | IN1+/- | IN2+/- | |
| Others | | | | | | N/A | N/A | |

Table 20. MIC/Line In Path Select (N/A: Not available)

| Register | | | Pin | | | | | | | |
|----------|-----------|-----------|--------------|--------------|--------------|--------------|-------------|--------------|--------------|--------------|
| AIN3 bit | MDIF1 bit | MDIF2 bit | LIN1 IN1- | RIN1 IN1+ | LIN2 IN2+ | RIN2 IN2- | MIN LIN3 | VCOC RIN3 | LIN4 IN4+ | RIN4 IN4- |
| 0 | 0 | 0 | O | O | O | O | O | - | O | O |
| 0 | 0 | 1 | O | X | O | O | O | - | O | X |
| 0 | 1 | 0 | O | O | X | O | O | - | X | O |
| 0 | 1 | 1 | O | O | O | O | O | - | X | X |
| 1 | 0 | 0 | O | O | O | O | O | O | O | O |
| 1 | 0 | 1 | O | X | O | O | O | X | O | X |
| 1 | 1 | 0 | O | O | X | O | X | O | X | O |
| 1 | 1 | 1 | O | O | O | O | X | X | X | X |

Table 21. Handling of MIC/Line Input Pins (“-”: Not available, “X”: Signal should not be input.)

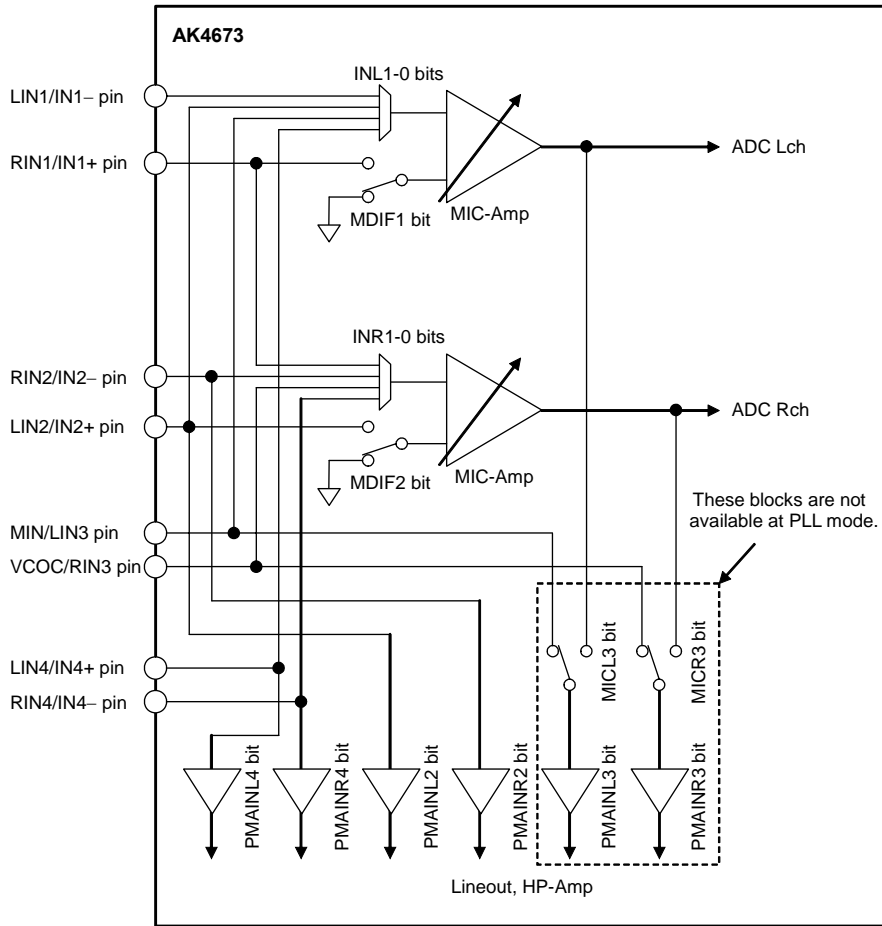


Figure 31. Mic/Line Input Selector

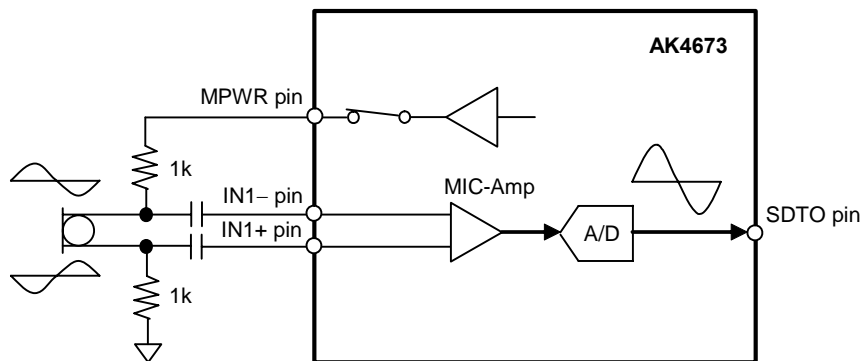


Figure 32. Connection Example for Full-differential Mic Input (MDIF1/2 bits = "1")

<Input Selector Setting Example>

In case that IN1+/- pins are used as full-differential mic input and LIN2/RIN2 pins are used as stereo line input, it is recommended that the following two modes are set by register setting according to each case.

| MDIF1 bit | MDIF2 bit | INL1 bit | INL0 bit | INR1 bit | INR0 bit | Lch | Rch |
|-----------|-----------|----------|----------|----------|----------|--------|------|
| 1 | 0 | 0 | 0 | 0 | 1 | IN1+/- | RIN2 |
| 0 | 0 | 0 | 1 | 0 | 1 | LIN2 | RIN2 |

Table 22. MIC/Line In Path Select Example

■ MIC Gain Amplifier

The AK4673 has a gain amplifier for microphone input. The gain of MIC-Amp is selected by the MGAIN1-0 bits (Table 23). The typical input impedance is 60kΩ(typ)@MGAIN1-0 bits = “00” or 30kΩ(typ)@MGAIN1-0 bits = “01”, “10” or “11”.

| MGAIN1 bit | MGAIN0 bit | Input Gain |
|------------|------------|------------|
| 0 | 0 | 0dB |
| 0 | 1 | +20dB |
| 1 | 0 | +26dB |
| 1 | 1 | +32dB |

(default)

Table 23. Mic Input Gain

■ MIC Power

When PMMP bit = “1”, the MPWR pin supplies power for the microphone. This output voltage is typically 0.75 x AVDD and the load resistance is minimum 0.5kΩ. In case of using two sets of stereo mic, the load resistance is minimum 2kΩ for each channel. Any capacitor must not be connected directly to the MPWR pin (Figure 33).

| PMMP bit | MPWR pin |
|----------|----------|
| 0 | Hi-Z |
| 1 | Output |

(default)

Table 24. MIC Power

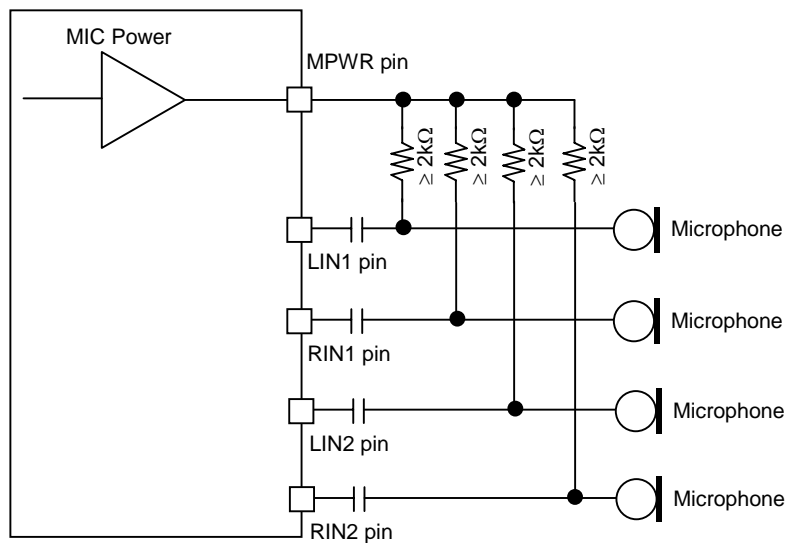


Figure 33. MIC Block Circuit

[Filter Coefficient Setting]

1) When FIL1 and FIL3 are set to “HPF”

fs: Sampling frequency
 fc: Cut-off frequency
 f: Input signal frequency
 K: Filter gain [dB] (Filter gain of should be set to 0dB.)

Register setting

FIL1: F1AS bit = “0”, F1A[13:0] bits =A, F1B[13:0] bits =B
 FIL3: F3AS bit = “0”, F3A[13:0] bits =A, F3B[13:0] bits =B
 (MSB=F1A13, F1B13, F3A13, F3B13; LSB=F1A0, F1B0, F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1 / \tan (\pi f c / f s)}{1 + 1 / \tan (\pi f c / f s)}, \quad B = \frac{1 - 1 / \tan (\pi f c / f s)}{1 + 1 / \tan (\pi f c / f s)}$$

| Transfer function | Amplitude | Phase |
|---|--|---|
| $H(z) = A \frac{1 - z^{-1}}{1 + Bz^{-1}}$ | $M(f) = A \sqrt{\frac{2 - 2\cos (2\pi f / f s)}{1 + B^2 + 2B\cos (2\pi f / f s)}}$ | $\theta(f) = \tan^{-1} \frac{(B+1)\sin (2\pi f / f s)}{1 - B + (B-1)\cos (2\pi f / f s)}$ |

2) When FIL1 and FIL3 are set to “LPF”

fs: Sampling frequency
 fc: Cut-off frequency
 f: Input signal frequency
 K: Filter gain [dB] (Filter gain of FIL1 should be set to 0dB.)

Register setting

FIL1: F1AS bit = “1”, F1A[13:0] bits =A, F1B[13:0] bits =B
 FIL3: F3AS bit = “1”, F3A[13:0] bits =A, F3B[13:0] bits =B
 (MSB=F1A13, F1B13, F3A13, F3B13; LSB=F1A0, F1B0, F3A0, F3B0)

$$A = 10^{K/20} \times \frac{1}{1 + 1 / \tan (\pi f c / f s)}, \quad B = \frac{1 - 1 / \tan (\pi f c / f s)}{1 + 1 / \tan (\pi f c / f s)}$$

| Transfer function | Amplitude | Phase |
|---|--|---|
| $H(z) = A \frac{1 + z^{-1}}{1 + Bz^{-1}}$ | $M(f) = A \sqrt{\frac{2 + 2\cos (2\pi f / f s)}{1 + B^2 + 2B\cos (2\pi f / f s)}}$ | $\theta(f) = \tan^{-1} \frac{(B-1)\sin (2\pi f / f s)}{1 + B + (B+1)\cos (2\pi f / f s)}$ |

3) EQ

fs: Sampling frequency
 fc₁: Pole frequency
 fc₂: Zero-point frequency
 f: Input signal frequency
 K: Filter gain [dB] (Maximum +12dB)

Register setting

EQA[15:0] bits =A, EQB[13:0] bits =B, EQC[15:0] bits =C
 (MSB=EQA15, EQB13, EQC15; LSB=EQA0, EQB0, EQC0)

$$A = 10^{K/20} \times \frac{1 + 1 / \tan(\pi f c_2 / f_s)}{1 + 1 / \tan(\pi f c_1 / f_s)}, \quad B = \frac{1 - 1 / \tan(\pi f c_1 / f_s)}{1 + 1 / \tan(\pi f c_1 / f_s)}, \quad C = 10^{K/20} \times \frac{1 - 1 / \tan(\pi f c_2 / f_s)}{1 + 1 / \tan(\pi f c_1 / f_s)}$$

| Transfer function | Amplitude | Phase |
|--|--|--|
| $H(z) = \frac{A + Cz^{-1}}{1 + Bz^{-1}}$ | $M(f) = \sqrt{\frac{A^2 + C^2 + 2AC \cos(2\pi f / f_s)}{1 + B^2 + 2B \cos(2\pi f / f_s)}}$ | $\theta(f) = \tan^{-1} \frac{(AB - C) \sin(2\pi f / f_s)}{A + BC + (AB + C) \cos(2\pi f / f_s)}$ |

[Translation the filter coefficient calculated by the equations above from real number to binary code (2's complement)]

$$X = (\text{Real number of filter coefficient calculated by the equations above}) \times 2^{13}$$

X should be rounded to integer, and then should be translated to binary code (2's complement).

MSB of each filter coefficient setting register is sine bit.

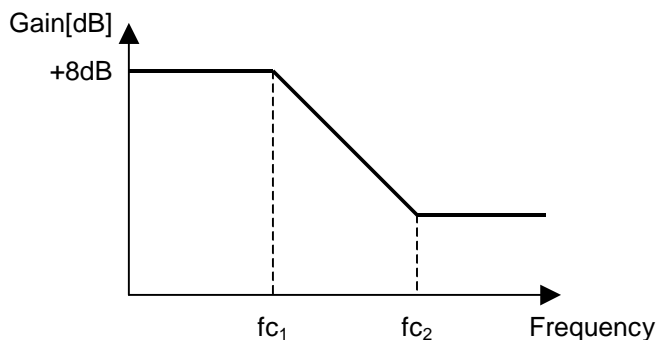
[Filter Coefficient Setting Example]

1) FIL1 block

Example: HPF, fs=44.1kHz, fc=100Hz
 F1AS bit = "0"
 F1A[13:0] bits = 01 1111 1100 0110
 F1B[13:0] bits = 10 0000 0111 0100

2) EQ block

Example: fs=44.1kHz, fc₁=300Hz, fc₂=3000Hz, Gain=+8dB



EQA[15:0] bits = 0000 1001 0110 1110
 EQB[13:0] bits = 10 0001 0101 1001
 EQC[15:0] bits = 1111 1001 1110 1111

■ ALC Operation

The ALC (Automatic Level Control) is executed by ALC block when ALC bit is “1”. When only DAC is powered-up, ALC circuit operates at playback path. When only ADC is powered-up or both ADC and DAC are powered-up, ALC circuit operates at recording path.

| PMADL bit, PMADR bit | PMDAC bit | LOOP bit | Status | ALC |
|----------------------|-----------|----------|----------------------------|----------------|
| “00” | 0 | x | Power-down | Power-down |
| | 1 | x | Playback | Playback path |
| “01”, “10” or “11” | 0 | x | Recording | Recording path |
| | | 0 | Recording & Playback | Recording path |
| | 1 | 1 | Recording Monitor Playback | Recording path |

Table 27. ALC Setting (x: Don't care)

1. ALC Limiter Operation

During the ALC limiter operation, if either Lch or Rch exceeds the ALC limiter detection level (Table 28), the IVL and IVR values (same value) are attenuated automatically to the amount defined by the ALC limiter ATT step (Table 29). The IVL and IVR are then set to the same value for both channels.

When ZELMN bit = “0” (zero cross detection is enabled), the IVL and IVR values are changed by ALC limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 30).

When ZELMN bit = “1” (zero cross detection is disabled), IVL and IVR values are immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless of the setting of LMAT1-0 bits.

The attenuate operation is executed continuously until the input signal level becomes ALC limiter detection level (Table 28) or less. After completing the attenuation operation, unless ALC bit is changed to “0”, the operation repeats when the input signal level exceeds LMTH1-0 bits.

| LMTH1 | LMTH0 | ALC Limier Detection Level | ALC Recovery Waiting Counter Reset Level |
|-------|-------|----------------------------|--|
| 0 | 0 | ALC Output \geq -2.5dBFS | -2.5dBFS > ALC Output \geq -4.1dBFS |
| 0 | 1 | ALC Output \geq -4.1dBFS | -4.1dBFS > ALC Output \geq -6.0dBFS |
| 1 | 0 | ALC Output \geq -6.0dBFS | -6.0dBFS > ALC Output \geq -8.5dBFS |
| 1 | 1 | ALC Output \geq -8.5dBFS | -8.5dBFS > ALC Output \geq -12dBFS |

Table 28. ALC Limiter Detection Level / Recovery Counter Reset Level

| ZELMN | LMAT1 | LMAT0 | ALC Limiter ATT Step | |
|-------|-------|-------|----------------------|---------|
| 0 | 0 | 0 | 1 step | 0.375dB |
| | 0 | 1 | 2 step | 0.750dB |
| | 1 | 0 | 4 step | 1.500dB |
| | 1 | 1 | 8 step | 3.000dB |
| 1 | x | x | 1step | 0.375dB |

Table 29. ALC Limiter ATT Step (x: Don't care)

| ZTM1 | ZTM0 | Zero Crossing Timeout Period | | | |
|------|------|------------------------------|-------|-------|---------|
| | | | 8kHz | 16kHz | 44.1kHz |
| 0 | 0 | 128/fs | 16ms | 8ms | 2.9ms |
| 0 | 1 | 256/fs | 32ms | 16ms | 5.8ms |
| 1 | 0 | 512/fs | 64ms | 32ms | 11.6ms |
| 1 | 1 | 1024/fs | 128ms | 64ms | 23.2ms |

Table 30. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

The ALC recovery operation waits for the WTM2-0 bits (Table 31) to be set after completing the ALC limiter operation. If the input signal does not exceed “ALC recovery waiting counter reset level” (Table 28) during the wait time, the ALC recovery operation is executed. The IVL and IVR values are automatically incremented by RGAIN1-0 bits (Table 32) up to the set reference level (Table 33) with zero crossing detection which timeout period is set by ZTM1-0 bits (Table 30). Then the IVL and IVR are set to the same value for both channels. The ALC recovery operation is executed at a period set by WTM2-0 bits. When zero cross is detected at both channels during the wait period set by WTM2-0 bits, the ALC recovery operation waits until WTM2-0 period and the next recovery operation is executed. If ZTM1-0 is longer than WTM2-0 and no zero crossing occurs, the ALC recovery operation is executed at a period set by ZTM1-0 bits.

For example, when the current IVOL value is 30H and RGAIN1-0 bits are set to “01”, IVOL is changed to 32H by the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the IVOL value exceeds the reference level (REF7-0), the IVOL values are not increased.

When

“ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)” during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When

“ALC recovery waiting counter reset level (LMTH1-0) > Output Signal”, the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation (Fast Recovery Operation). When large noise is input to microphone instantaneously, the quality of small signal level in the large noise can be improved by this fast recovery operation. The speed of fast recovery operation is set by RFST1-0 bits (Table 34).

| WTM2 | WTM1 | WTM0 | ALC Recovery Operation Waiting Period | | | (default) |
|------|------|------|---------------------------------------|--------|--------|-----------|
| | | | | 8kHz | 16kHz | |
| 0 | 0 | 0 | 128/fs | 16ms | 8ms | 2.9ms |
| 0 | 0 | 1 | 256/fs | 32ms | 16ms | 5.8ms |
| 0 | 1 | 0 | 512/fs | 64ms | 32ms | 11.6ms |
| 0 | 1 | 1 | 1024/fs | 128ms | 64ms | 23.2ms |
| 1 | 0 | 0 | 2048/fs | 256ms | 128ms | 46.4ms |
| 1 | 0 | 1 | 4096/fs | 512ms | 256ms | 92.9ms |
| 1 | 1 | 0 | 8192/fs | 1024ms | 512ms | 185.8ms |
| 1 | 1 | 1 | 16384/fs | 2048ms | 1024ms | 371.5ms |

Table 31. ALC Recovery Operation Waiting Period

| RGAIN1 | RGAIN0 | GAIN STEP | | (default) |
|--------|--------|-----------|---------|-----------|
| 0 | 0 | 1 step | 0.375dB | |
| 0 | 1 | 2 step | 0.750dB | |
| 1 | 0 | 3 step | 1.125dB | |
| 1 | 1 | 4 step | 1.500dB | |

Table 32. ALC Recovery GAIN Step

| REF7-0 | GAIN(dB) | Step |
|--------|----------|-------------------|
| F1H | +36.0 | 0.375dB (default) |
| F0H | +35.625 | |
| EFH | +35.25 | |
| : | : | |
| E2H | +30.375 | |
| E1H | +30.0 | |
| E0H | +29.625 | |
| : | : | |
| 03H | -53.25 | |
| 02H | -53.625 | |
| 01H | -54.0 | |
| 00H | MUTE | |

Table 33. Reference Level at ALC Recovery operation

| RFST1 bit | RFST0 bit | Recovery Speed |
|-----------|-----------|-------------------|
| 0 | 0 | 4 times (default) |
| 0 | 1 | 8 times |
| 1 | 0 | 16times |
| 1 | 1 | N/A |

Table 34. Fast Recovery Speed Setting (N/A: Not available)

3. Example of ALC Operation

Table 35 shows the examples of the ALC setting for mic recording.

| Register Name | Comment | fs=8kHz | | fs=44.1kHz | |
|-------------------|---|---------|-----------|------------|-----------|
| | | Data | Operation | Data | Operation |
| LMTH1-0 | Limiter detection Level | 01 | -4.1dBFS | 01 | -4.1dBFS |
| ZELMN | Limiter zero crossing detection | 0 | Enable | 0 | Enable |
| ZTM1-0 | Zero crossing timeout period | 01 | 32ms | 11 | 23.2ms |
| WTM2-0 | Recovery waiting period *WTM2-0 bits should be the same or longer data as ZTM1-0 bits. | 001 | 32ms | 011 | 23.2ms |
| REF7-0 | Maximum gain at recovery operation | E1H | +30dB | E1H | +30dB |
| IVL7-0, IVR7-0 | Gain of IVOL | E1H | +30dB | E1H | +30dB |
| LMAT1-0 | Limiter ATT step | 00 | 1 step | 00 | 1 step |
| RGAIN1-0 | Recovery GAIN step | 00 | 1 step | 00 | 1 step |
| RFST1-0 | Fast Recovery Speed | 00 | 4 times | 00 | 4 times |
| ALC | ALC enable | 1 | Enable | 1 | Enable |

Table 35. Example of the ALC setting

The following registers should not be changed during the ALC operation. These bits should be changed after the ALC operation is finished by ALC bit = "0" or PMADL=PMADR bits = "0".

- LMTH1-0, LMAT1-0, WTM2-0, ZTM1-0, RGAIN1-0, REF7-0, ZELMN, RFST1-0

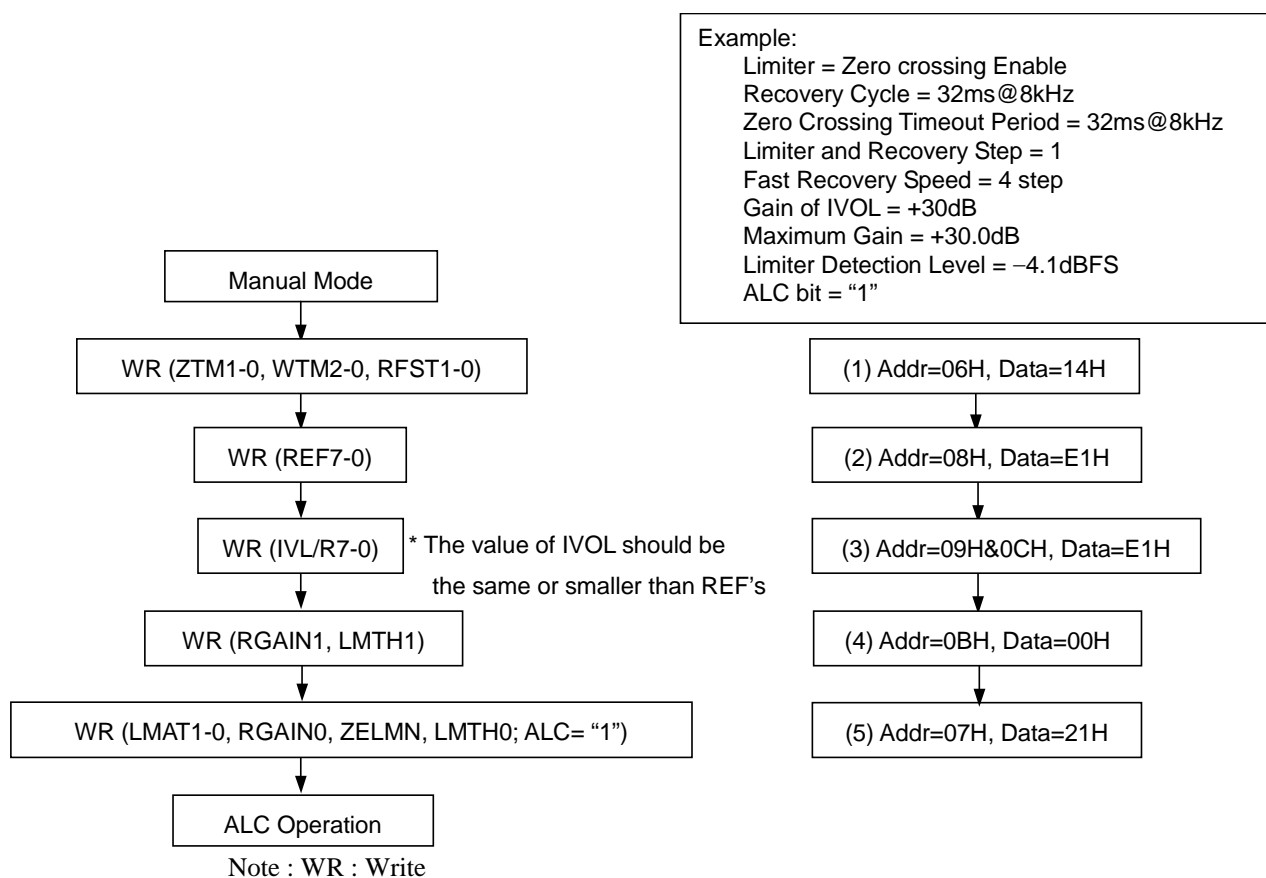


Figure 35. Registers set-up sequence at ALC operation

■ Input Digital Volume (Manual Mode)

The input digital volume becomes manual mode when ALC bit is “0”. This mode is used in the case shown below.

1. After exiting reset state, set-up the registers for the ALC operation (ZTM1-0, LMTH1-0 and etc)
2. When the registers for the ALC operation (Limiter period, Recovery period and etc) are changed.
For example; when the sampling frequency is changed.
3. When IVOL is used as a manual volume.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 36). The IVOL value is changed at zero crossing or timeout. Zero crossing timeout period is set by ZTM1-0 bits. If IVL7-0 or IVR7-0 bits are written during PMADL=PMADR bits = “0”, IVOL operation starts with written values at the end of the ADC initialization cycle after PMADL or PMADR bit is changed to “1”.

Even if the path is switched from recording to playback, the register setting of IVOL remains. Therefore, IVL7-0 and IVR7-0 bits should be set to “91H” (0dB).

| IVL7-0 IVR7-0 | GAIN (dB) | Step |
|------------------|-----------|-------------------|
| F1H | +36.0 | 0.375dB (default) |
| F0H | +35.625 | |
| EFH | +35.25 | |
| : | : | |
| E2H | +30.375 | |
| E1H | +30.0 | |
| E0H | +29.625 | |
| : | : | |
| 03H | -53.25 | |
| 02H | -53.625 | |
| 01H | -54 | |
| 00H | MUTE | |

Table 36. Input Digital Volume Setting

When writing to the IVL7-0 and IVR7-0 bits continuously, the control register should be written in an interval more than zero crossing timeout. If not, IVL and IVR are not changed since zero crossing counter is reset at every write operation. If the same register value as the previous write operation is written to IVL and IVR, this write operation is ignored and zero crossing counter is not reset. Therefore, IVL and IVR can be written by an interval less than zero crossing timeout.


| | | | |
|--------------|--|--------------------------------|-------------------|
| ALC bit |  | | |
| ALC Status | Disable | Enable | Disable |
| IVL7-0 bits | E1H(+30dB) | | |
| IVR7-0 bits | C6H(+20dB) | | |
| Internal IVL | E1H(+30dB) | E1(+30dB) --> F1(+36dB) | E1(+30dB) |
| Internal IVR | C6H(+20dB) | (1) E1(+30dB) --> F1(+36dB) | (2) C6H(+20dB) |

Figure 36. IVOL value during ALC operation

- (1) The IVL value becomes the start value if the IVL and IVR are different when the ALC starts. The wait time from ALC bit = "1" to ALC operation start by IVL7-0 bits is at most recovery time (WTM2-0 bits) plus zerocross timeout period (ZTM1-0 bits).
- (2) Writing to IVL and IVR registers (09H and 0CH) is ignored during ALC operation. After ALC is disabled, the IVOL changes to the last written data by zero crossing or timeout. When ALC is enabled again, ALC bit should be set to "1" in an interval more than zero crossing timeout period after ALC bit = "0".

■ De-emphasis Filter

The AK4673 includes the digital de-emphasis filter ($t_c = 50/15\mu s$) by IIR filter. Setting the DEM1-0 bits enables the de-emphasis filter (Table 37).

| DEM1 | DEM0 | Mode |
|------|------|---------|
| 0 | 0 | 44.1kHz |
| 0 | 1 | OFF |
| 1 | 0 | 48kHz |
| 1 | 1 | 32kHz |

(default)

Table 37. De-emphasis Control

■ Bass Boost Function

The BST1-0 bits control the amount of low frequency boost applied to the DAC output signal (Table 38). If the BST1-0 bits are set to “01” (MIN Level), use a $47\mu F$ capacitor for AC-coupling. If the boosted signal exceeds full scale, the analog output clips to the full scale. Figure 37 shows the boost frequency response at -20dB signal input.

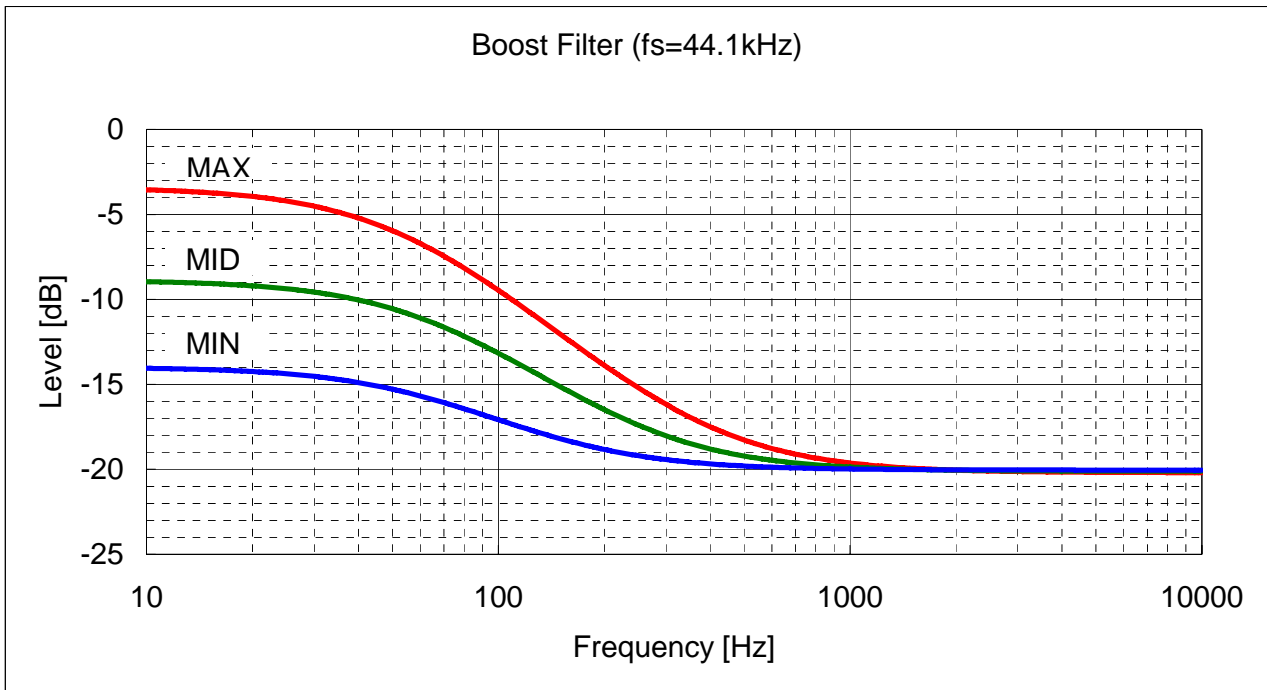


Figure 37. Bass Boost Frequency Response ($f_s=44.1\text{kHz}$)

| BST1 | BST0 | Mode |
|------|------|------|
| 0 | 0 | OFF |
| 0 | 1 | MIN |
| 1 | 0 | MID |
| 1 | 1 | MAX |

(default)

Table 38. Bass Boost Control

■ Digital Output Volume

The AK4673 has a digital output volume (256 levels, 0.5dB step, Mute). The volume can be set by the DVL7-0 and DVR7-0 bits. The volume is included in front of a DAC block. The input data of DAC is changed from +12 to -115dB or MUTE. When the DVOLC bit = "1", the DVL7-0 bits control both Lch and Rch attenuation levels. When the DVOLC bit = "0", the DVL7-0 bits control Lch level and DVR7-0 bits control Rch level. This volume has a soft transition function. The DVTM bit sets the transition time between set values of DVL/R7-0 bits as either 1061/fs or 256/fs (Table 40). When DVTM bit = "0", a soft transition between the set values occurs (1062 levels). It takes 1061/fs (=24ms@fs=44.1kHz) from 00H (+12dB) to FFH (MUTE).

| DVL/R7-0 | Gain | Step |
|----------|--------------------|--------------------|
| 00H | +12.0dB | 0.5dB (default) |
| 01H | +11.5dB | |
| 02H | +11.0dB | |
| : | : | |
| 18H | 0dB | |
| : | : | |
| FDH | -114.5dB | |
| FEH | -115.0dB | |
| FFH | MUTE ($-\infty$) | |

Table 39. Digital Volume Code Table

| DVTM bit | Transition time between DVL/R7-0 bits = 00H and FFH | | |
|----------|---|---------|------------|
| | Setting | fs=8kHz | fs=44.1kHz |
| 0 | 1061/fs | 133ms | 24ms |
| 1 | 256/fs | 32ms | 6ms |

Table 40. Transition Time Setting of Digital Output Volume

■ Soft Mute

Soft mute operation is performed in the digital domain. When the SMUTE bit goes to “1”, the output signal is attenuated to $-\infty$ (“0”) during the cycle set by the DVTM bit. When the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to the value set by the DVL/R7-0 bits during the cycle set of the DVTM bit. If the soft mute is cancelled within the cycle set by the DVTM bit after starting the operation, the attenuation is discontinued and returned to the value set by the DVL/R7-0 bits. The soft mute is effective for changing the signal source without stopping the signal transmission (Figure 38).

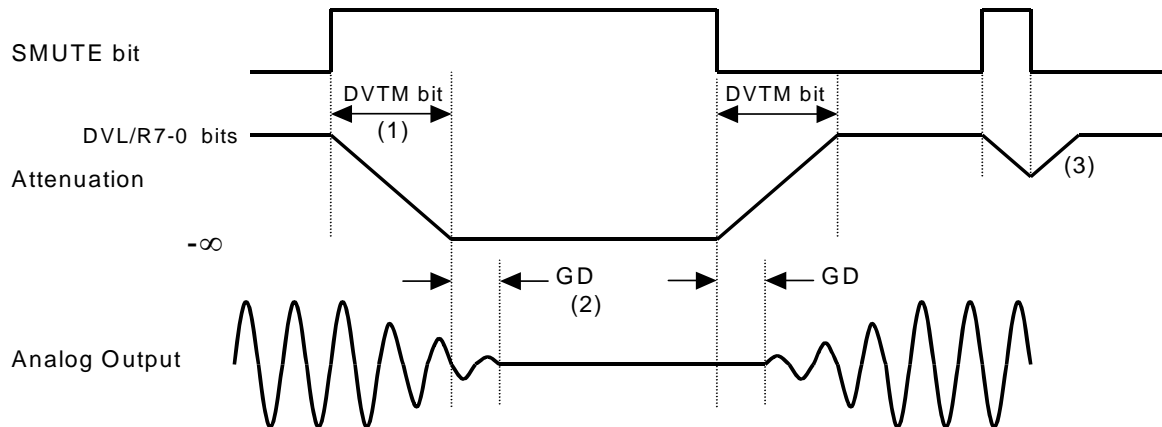


Figure 38. Soft Mute Function

- (1) The output signal is attenuated until $-\infty$ (“0”) by the cycle set by the DVTM bit.
- (2) Analog output corresponding to digital input has the group delay (GD).
- (3) If the soft mute is cancelled within the cycle set by the DVTM bit, the attenuation is discontinued and returned to the value set by the DVL/R7-0 bits.

■ Analog Mixing: Stereo Input (LIN2/RIN2/LIN4/RIN4, AIN3 bit = “1”): LIN3/RIN3 pins)

When PMAINL2=PMAINR2 bits = “1”, LIN2 and RIN2 pins can be used as stereo line input for analog mixing. When the LINH2 and RINH2 bits are set to “1”, the input signal from the LIN2/RIN2 pins is output to Headphone-Amp. When the LINL2/RINR2 bits are set to “1”, the input signal from the LIN2/RIN2 pins is output to the stereo line output amplifier.

When PMAINL4=PMAINR4 bits = “1”, LIN4 and RIN4 pins can be used as stereo line input for analog mixing. When the LINH4 and RINH4 bits are set to “1”, the input signal from the LIN4/RIN4 pins is output to Headphone-Amp. When the LINL4/RINR4 bits are set to “1”, the input signal from the LIN4/RIN4 pins is output to the stereo line output amplifier.

When the analog mixing is used, A/D converter is also available if PMADL or PMADR bit is “1”. In this case, the input resistance of LIN2/RIN2/LIN4/RIN4 pins become 30kΩ (typ) at MGAIN1-0 bits = “00” and 20kΩ (typ) at MGAIN1-0 bits = “01”, “10” or “11”, respectively.

When AIN3 bit = “1”, the MIN and VCOC pins become LIN3 and RIN3 pins, respectively. In this case, PLL is not available. When PMAINL3=PMAINR3 bits = “1”, LIN3 and RIN3 pins can be used as stereo line input for analog mixing. When PMMICL=PMMICR=MICL3=MICR3 bits = “1”, analog mixing source is changed from LIN3/RIN3 input to MIC-Amp output signal. When the LINH3 and RINH3 bits are set to “1”, the input signal from the LIN3/RIN3 pins is output to Headphone-Amp. When the LINL3/RINR3 bits are set to “1”, the input signal from the LIN3/RIN3 pins is output to the stereo line output amplifier.

When the analog mixing is used, A/D converter is also available if PMADL or PMADR bit is “1”. When the analog mixing is used at MICL3=MICR3 bits = “0”, the input resistance of LIN3/RIN3 pins becomes 30kΩ (typ) at MGAIN1-0 bits = “00” and 20kΩ (typ) at MGAIN1-0 bits = “01”, “10” or “11”, respectively. When the analog mixing is used at MICL3=MICR3 bits = “1”, the input resistance of LIN3/RIN3 pins becomes 60kΩ (typ) at MGAIN1-0 bits = “00” and 30kΩ (typ) at MGAIN1-0 bits = “01”, “10” or “11”, respectively.

Table 41, Table 42 and Table 43 show the typical gain.

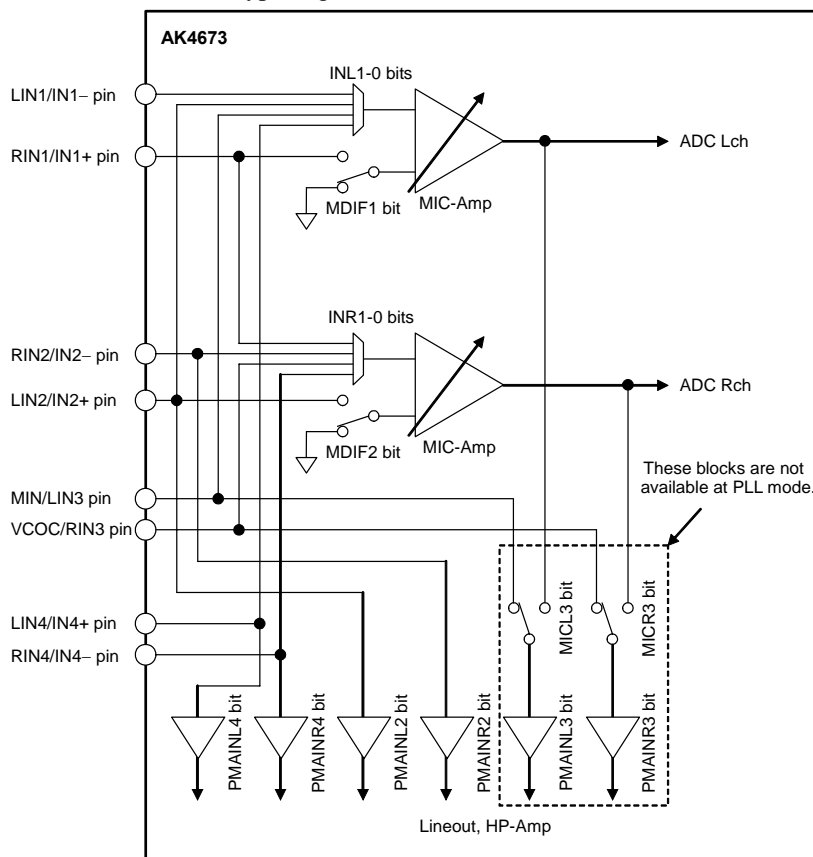


Figure 39. Analog Mixing Circuit (Stereo Input)

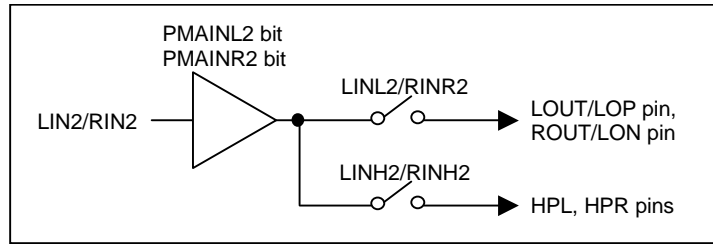


Figure 40. Analog Mixing Circuit (LIN2/RIN2)

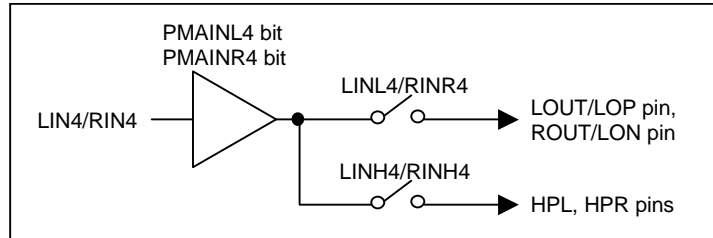


Figure 41. Analog Mixing Circuit (LIN4/RIN4)

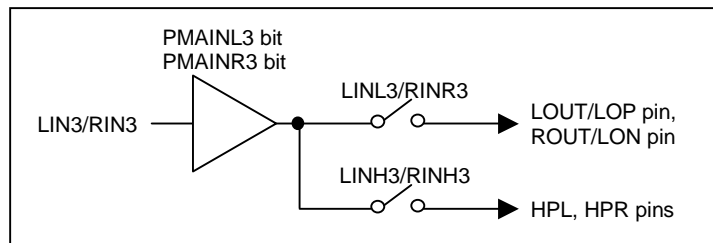


Figure 42. Analog Mixing Circuit (LIN3/RIN3: PLL is not available.)

| LOVL bit | LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 → LOUT/ROUT | (default) |
|----------|--|-----------|
| 0 | 0dB | |
| 1 | +2dB | |

Table 41. LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 Input → LOUT/ROUT Output Gain (typ)

| LOVL bit | LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 → LOP/LON | (default) |
|----------|--|-----------|
| 0 | 0dB | |
| 1 | +2dB | |

Table 42. LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 Input → LOP/LON Output Gain (typ)

| HPG bit | LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 → HPL/HPR | (default) |
|---------|--|-----------|
| 0 | 0dB | |
| 1 | +3.6dB | |

Table 43. LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 Input → Headphone-Amp Output Gain (typ)

■ Analog Mixing: Full-differential Mono Input (L4DIF bit = “1”: IN4+/IN4– pins)

When L4DIF bit = “1”, LIN4 and RIN4 pins becomes IN4+ and IN4– pins, respectively.

When PMAINL4 bit = “1”, IN4+ and IN4– pins can be used as full-differential mono line input for analog mixing. When the LINH4 and RINH4 bits are set to “1”, the input signal from the IN4+/IN4– pins is output to Headphone-Amp. When the LINL4/RINR4 bits are set to “1”, the input signal from the IN4+/IN4– pins is output to the stereo line output amplifier.

Table 44, Table 45 and Table 46 show the typical gain. Input signal amplitude is defined as (IN4+) – (IN4–).

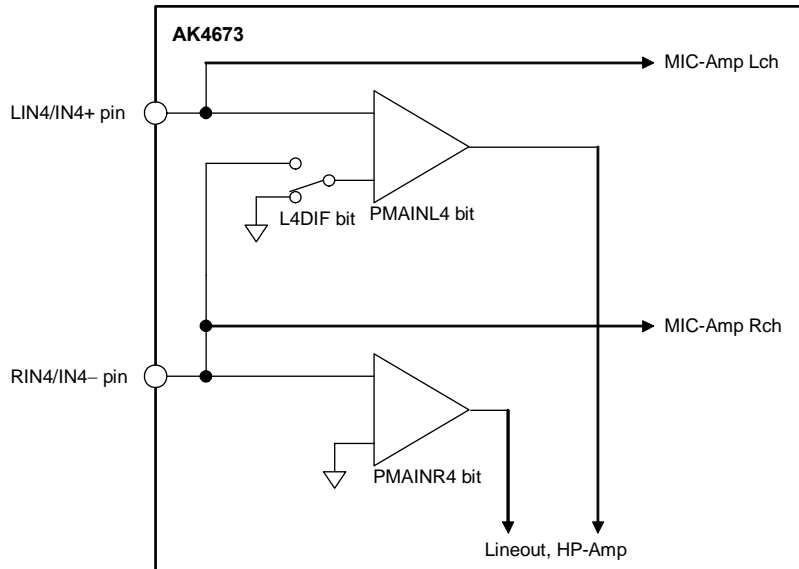


Figure 43. Full-differential Mono Analog Mixing Circuit

| LOVL bit | IN4+/IN4– → LOUT/ROUT | (default) |
|----------|-----------------------|-----------|
| 0 | -6dB | |
| 1 | -4dB | |

Table 44. IN4+/IN4– Input → LOUT/ROUT Output Gain (typ)

| LOVL bit | IN4+/IN4– → LOP/LON | (default) |
|----------|---------------------|-----------|
| 0 | 0dB | |
| 1 | +2dB | |

Table 45. IN4+/IN4– Input → LOP/LON Output Gain (typ)

| HPG bit | IN4+/IN4– → HPL/HPR | (default) |
|---------|---------------------|-----------|
| 0 | -6dB | |
| 1 | -2.4dB | |

Table 46. IN4+/IN4– Input → Headphone-Amp Output Gain (typ)

■ Analog Mixing: Mono Input (AIN3 bit = "0": MIN pin)

When AIN3 bit = "0", the MIN pin is used as mono input for analog mixing. When the PMMIN bit is set to "1", the mono input is powered-up. When the MINH bit is set to "1", the input signal from the MIN pin is output to Headphone-Amp. When the MINL bit is set to "1", the input signal from the MIN pin is output to the stereo line output amplifier. The external resistor R_i adjusts the signal level of MIN input. Table 47, Table 48 and Table 49 show the typical gain example at $R_i = 20k\Omega$. This gain is in inverse proportion to R_i .

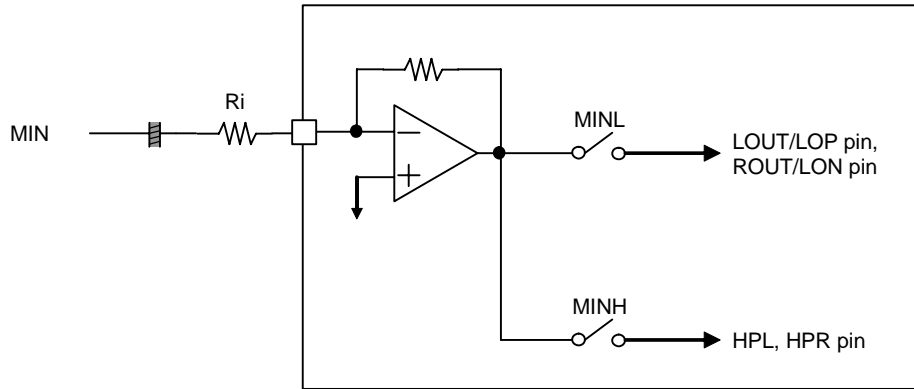


Figure 7. Block Diagram of MIN pin

| LOVL bit | MIN → LOUT/ROUT | (default) |
|----------|-----------------|-----------|
| 0 | 0dB | |
| 1 | +2dB | |

Table 47. MIN Input → LOUT/ROUT Output Gain (typ) at $R_i = 20k\Omega$

| LOVL bit | MIN → LOP/LON | (default) |
|----------|---------------|-----------|
| 0 | +6dB | |
| 1 | +8dB | |

Table 48. MIN Input → LOP/LON Output Gain (typ) at $R_i = 20k\Omega$

| HPG bit | MIN → HPL/HPR | (default) |
|---------|---------------|-----------|
| 0 | -20dB | |
| 1 | -16.4dB | |

Table 49. MIN Input → Headphone-Amp Output Gain (typ) at $R_i = 20k\Omega$

■ Stereo Line Output (LOUT/ROUT pins)

When DACL bit is “1”, single-ended Lch/Rch signal of DAC is output from the LOUT/ROUT pins. When DACL bit is “0”, output signal is muted and LOUT/ROUT pins output VCOM voltage. The load impedance is 10kΩ (min.). When the PMLO=LOPS bits = “0”, the stereo line output enters power-down mode and the output is pulled-down to VSS1 by 100kΩ(typ). When the LOPS bit is “1”, stereo line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO bit at LOPS bit = “1”. In this case, output signal line should be pulled-down to VSS1 by 20kΩ after AC coupled as [Figure 45](#). Rise/Fall time is 300ms(max) at C=1μF and AVDD=3.3V. When PMLO bit = “1” and LOPS bit = “0”, stereo line output is in normal operation.

LOVL bit set the gain of stereo line output.

When LOM bit = “1”, DAC output signal is output to LOUT and ROUT pins as (L+R)/2 mono signal.

When LOM3 bit = “1”, the signal selected by MICL3 and MICR3 bits (LIN3/RIN3 inputs or MIC-Amp outputs) to LOUT and ROUT pins as (L+R)/2 mono signal.

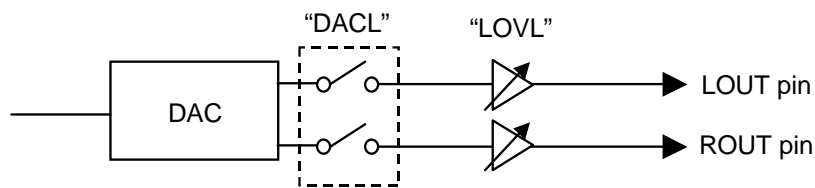


Figure 44. Stereo Line Output

| LOPS | PMLO | Mode | LOUT/ROUT pin |
|------|------|------------------|-------------------|
| 0 | 0 | Power-down | Pull-down to VSS1 |
| | 1 | Normal Operation | Normal Operation |
| 1 | 0 | Power-save | Fall down to VSS1 |
| | 1 | Power-save | Rise up to VCOM |

(default)

Table 50. Stereo Line Output Mode Select (x: Don't care)

| LOVL | Gain | Output Voltage (typ) |
|------|------|----------------------|
| 0 | 0dB | 0.6 x AVDD |
| 1 | +2dB | 0.757 x AVDD |

(default)

Table 51. Stereo Line Output Volume Setting

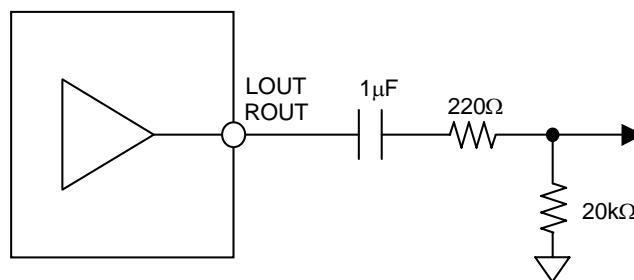


Figure 45. External Circuit for Stereo Line Output (in case of using Pop Reduction Circuit)

<Stereo Line Output Control Sequence (in case of using Pop Reduction Circuit)>

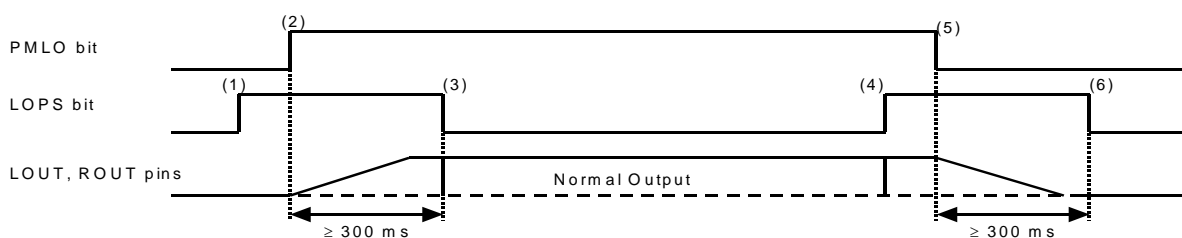


Figure 46. Stereo Line Output Control Sequence (in case of using Pop Reduction Circuit)

- (1) Set LOPS bit = "1". Stereo line output enters the power-save mode.
- (2) Set PMLO bit = "1". Stereo line output exits the power-down mode.
LOUT and ROUT pins rise up to VCOM voltage. Rise time is 200ms (max 300ms) at C=1 μ F and AVDD=3.3V.
- (3) Set LOPS bit = "0" after LOUT and ROUT pins rise up. Stereo line output exits the power-save mode.
Stereo line output is enabled.
- (4) Set LOPS bit = "1". Stereo line output enters power-save mode.
- (5) Set PMLO bit = "0". Stereo line output enters power-down mode.
LOUT and ROUT pins fall down to VSS1. Fall time is 200ms (max 300ms) at C=1 μ F and AVDD=3.3V.
- (6) Set LOPS bit = "0" after LOUT and ROUT pins fall down. Stereo line output exits the power-save mode.

<Analog Mixing Circuit for Stereo Line Output>

When AIN3 bit = "0", DACL, MINL, LINL2, RINR2, LINL4 and RINR4 bits controls each path switch. MIN path mixing gain is 0dB(typ)@LOVL bit = "0" when the external input resistance is 20kΩ. LIN2, RIN2, LIN4, RIN4 and DAC pathes mixing gain is 0dB(typ)@LOVL bit = "0".

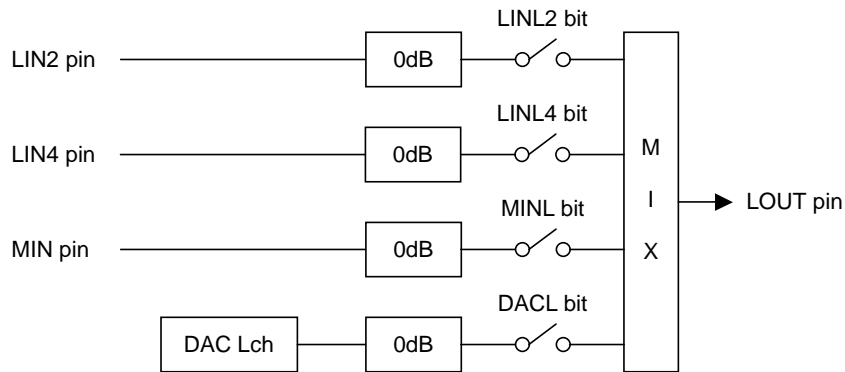


Figure 47. LOUT Mixing Circuit (AIN3 bit = "0", LOVL bit = "0")

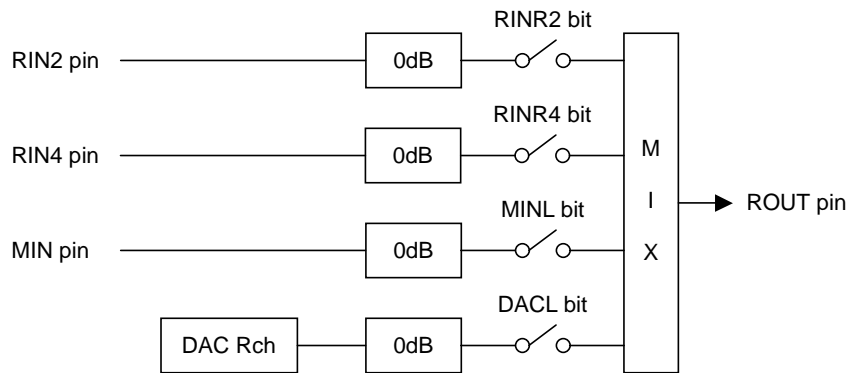


Figure 48. ROUT Mixing Circuit (AIN3 bit = "0", LOVL bit = "0")

When AIN3 bit = "1", DACL, LINL2, RINR2, LINL3, RINR3, LINL4, RINR4, MICL3 and MICR3 bits controls each path switch.

All paths mixing gain is 0dB(typ)@LOVL bit = "0".

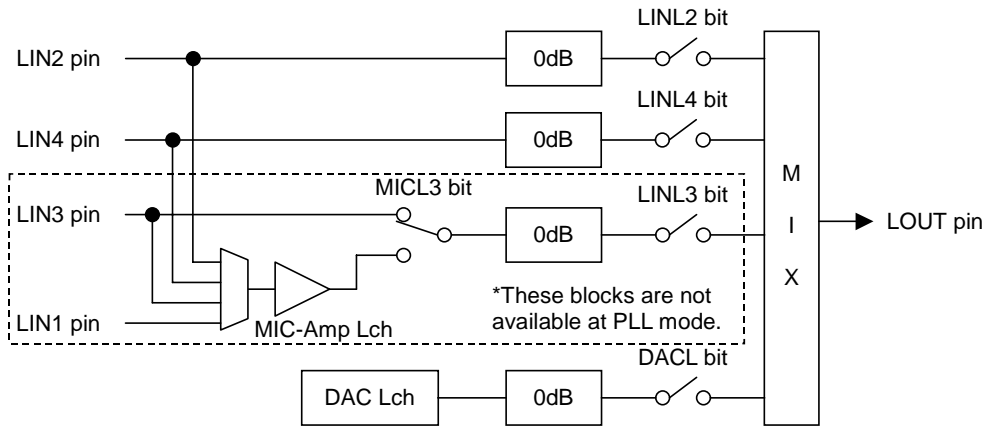


Figure 49. LOUT Mixing Circuit (AIN3 bit = "1", LOVL bit = "0")

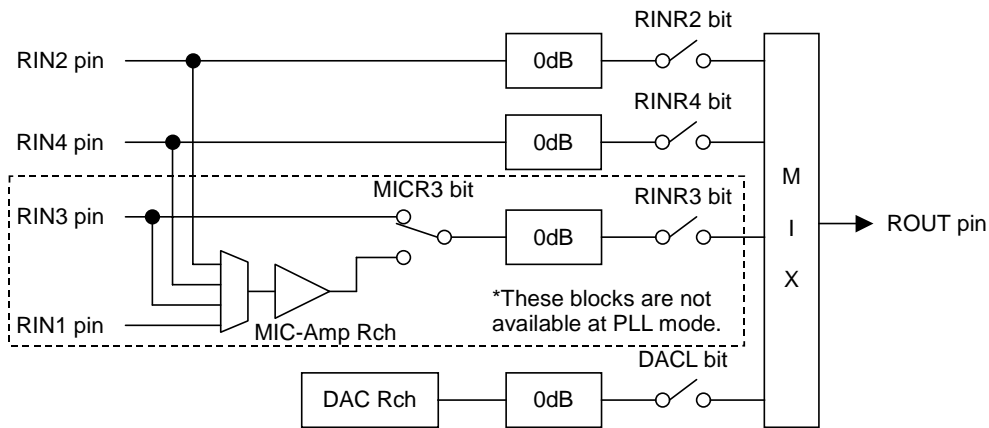


Figure 50. ROUT Mixing Circuit (AIN3 bit = "1", LOVL bit = "0")

■ Full-differential Mono Line Output (LOP/LON pins)

When LODIF bit = “1”, LOUT/ROUT pins become LOP/LON pins, respectively. Lch/Rch signal of DAC or LIN2/RIN2/LIN3/RIN3/LIN4/RIN4 is output from the LOP/LON pins which is full-differential as $(L+R)/2$ signal. The load impedance is 10k Ω (min) for LOP and LON pins, respectively. When the PMLO bit = “0”, the mono line output enters power-down mode and the output is Hi-Z. When the PMLO bit is “1” and LOPS bit is “1”, mono line output enters power-save mode. Pop noise at power-up/down can be reduced by changing PMLO bit at LOPS bit = “0”. When PMLO bit = “1” and LOPS bit = “0”, mono line output enters in normal operation. LOVL bit set the gain of mono line output.

When L4DIF=LODIF bits = “1”, full-differential output signal is as follows: $(LOP) - (LON) = (IN4+) - (IN4-)$.

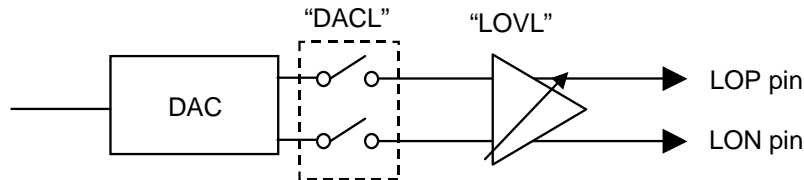


Figure 51. Mono Line Output

| LOVL | Gain | Output Voltage (typ) | |
|------|------|----------------------|-----------|
| 0 | +6dB | 1.2 x AVDD | (default) |
| 1 | +8dB | 1.5 x AVDD | |

Table 52. Mono Line Output Volume Setting

| PMLO | LOPS | Mode | LOP | LON | |
|------|------|------------------|------------------|------------------|-----------|
| 0 | x | Power-down | Hi-Z | Hi-Z | (default) |
| 1 | 1 | Power-save | Hi-Z | VCOM/2 | |
| | 0 | Normal Operation | Normal Operation | Normal Operation | |

Table 53. Mono Line Output Mode Setting (x: Don't care)

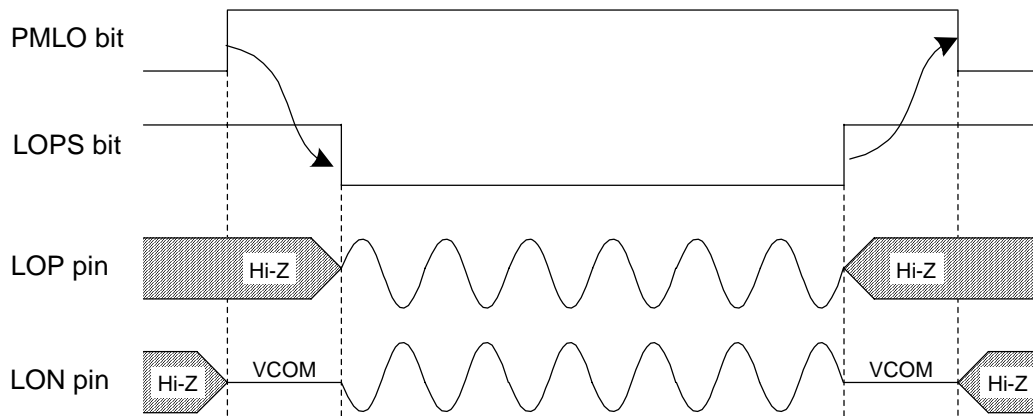


Figure 52. Power-up/Power-down Timing for Mono Line Output

<Analog Mixing Circuit for Mono Line Output>

When AIN3 bit = "0", DACL, MINL, LINL2, RINR2, LINL4 and RINR4 bits controls each path switch. MIN path mixing gain is +6dB(typ)@LOVL bit = "0" when the external input resistance is 20kΩ. LIN2, RIN2, LIN4, RIN4 and DAC pathes mixing gain is 0dB(typ)@LOVL bit = "0".

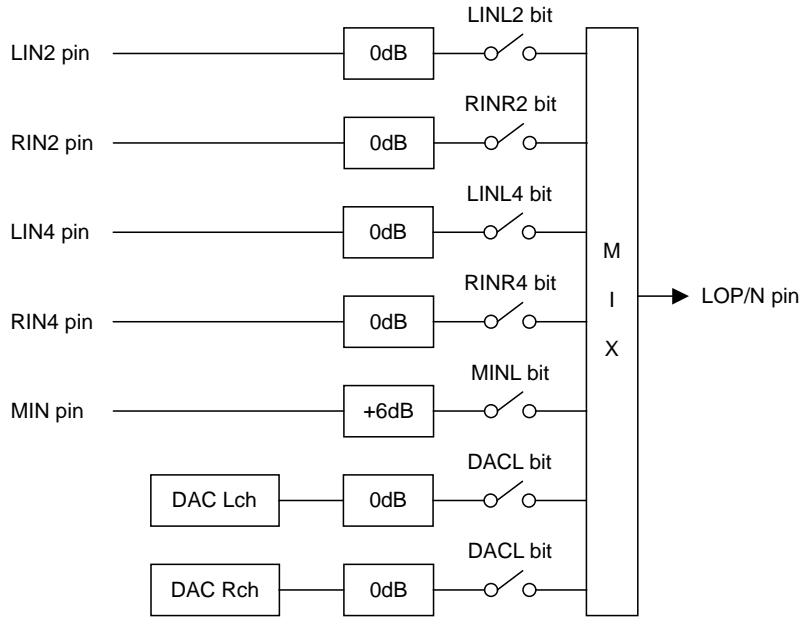


Figure 53. Mono Line Output Mixing Circuit (AIN3 bit = "0", LOVL bit = "0")

When AIN3 bit = "1", DACL, LINL2, RINR2, LINL3, RINR3, LINL4, RINR4, MICL3 and MICR3 bits controls each path switch. All pathes mixing gain is 0dB(typ)@LOVL bit = "0".

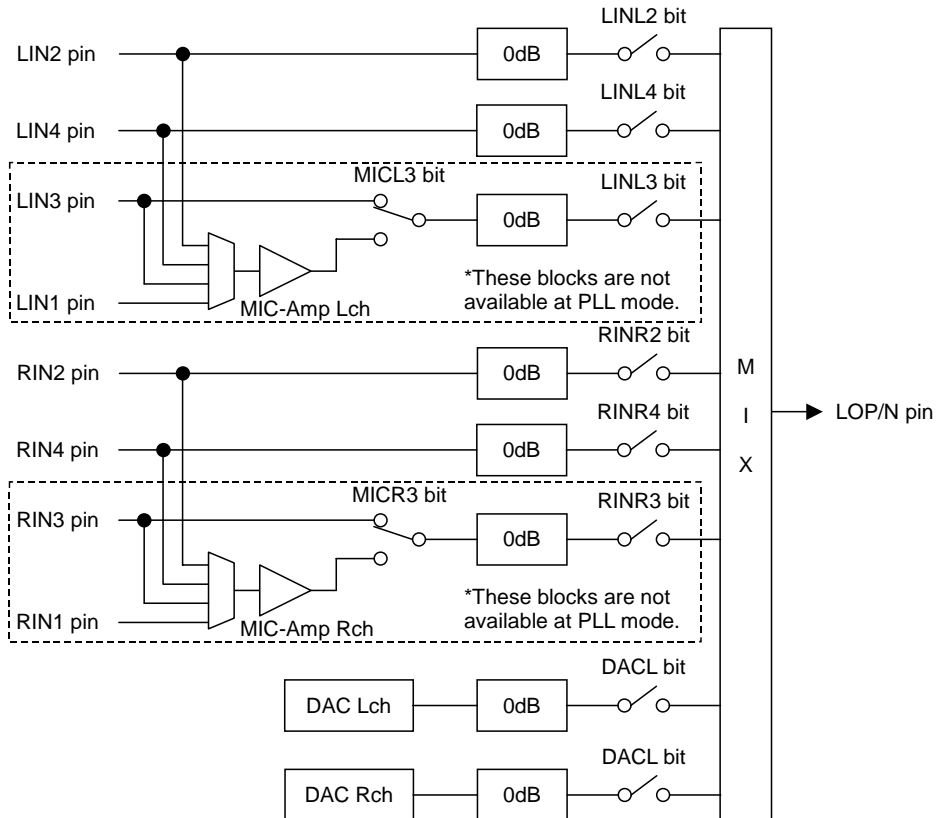


Figure 54. Mono Line Output Mixing Circuit (AIN3 bit = "1", LOVL bit = "0")

■ Headphone Output

Power supply voltage for the Headphone-Amp is supplied from the HVDD pin and centered on the HVDD/2 voltage at VBAT bit = "0". The load resistance is 16Ω (min). HPG bit selects the output voltage (Table 54).

When HPM bit = "1", DAC output signal is output to HPL and HPR pins as (L+R)/2 mono signal.

When HPM3 bit = "1", the signal selected by MICL3 and MICR3 bits (LIN3/RIN3 inputs or MIC-Amp outputs) to HPL and HPR pins as (L+R)/2 mono signal.

| HPG bit | 0 | 1 |
|----------------------|------------|-------------|
| Output Voltage [Vpp] | 0.6 x AVDD | 0.91 x AVDD |

Table 54. Headphone-Amp Output Voltage

When the HPMTN bit is "0", the common voltage of Headphone-Amp falls and the outputs (HPL and HPR pins) go to "L" (VSS2). When the HPMTN bit is "1", the common voltage rises to HVDD/2 at VBAT bit = "0". A capacitor between the MUTET pin and ground reduces pop noise at power-up. Rise/Fall time constant is in proportional to HVDD voltage and the capacitor at the MUTET pin.

[Example]: A capacitor between the MUTET pin and ground = 1.0μF, HVDD=3.3V:

Rise/fall time constant: $\tau = 100\text{ms}(\text{typ}), 250\text{ms}(\text{max})$

Time until the common goes to VSS2 when HPMTN bit = "1" → "0": 500ms(max)

When PMHPL and PMHPR bits are "0", the Headphone-Amp is powered-down, and the outputs (HPL and HPR pins) go to "L" (VSS2).

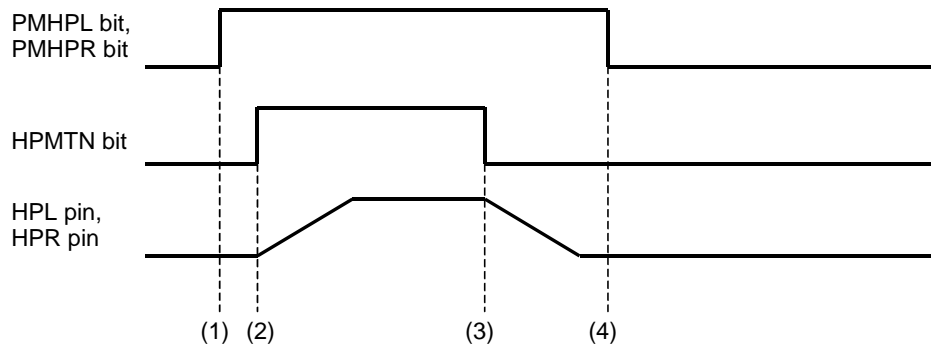


Figure 55. Power-up/Power-down Timing for Headphone-Amp

- (1) Headphone-Amp power-up (PMHPL, PMHPR bit = "1"). The outputs are still VSS2.
- (2) Headphone-Amp common voltage rises up (HPMTN bit = "1"). Common voltage of Headphone-Amp is rising.
- (3) Headphone-Amp common voltage falls down (HPMTN bit = "0"). Common voltage of Headphone-Amp is falling.
- (4) Headphone-Amp power-down (PMHPL, PMHPR bit = "0"). The outputs are VSS2. If the power supply is switched off or Headphone-Amp is powered-down before the common voltage goes to VSS2, some POP noise occurs.

<External Circuit of Headphone-Amp >

When BOOST=OFF, the cut-off frequency (f_c) of Headphone-Amp depends on the external resistor and capacitor. This f_c can be shifted to lower frequency by using bass boost function. Table 55 shows the cut off frequency and the output power for various resistor/capacitor combinations. The headphone impedance R_L is 16Ω. Output powers are shown at HVDD = 3.0, 3.3 and 5.0V. The output voltage of headphone is 0.6 x AVDD (Vpp) @HPG bit = "0" and 0.91 x AVDD (Vpp) @HPG bit = "1".

When an external resistor R is smaller than 12Ω, put an oscillation prevention circuit (0.22μF±20% capacitor and 10Ω±20% resistor) because it has the possibility that the Headphone-Amp oscillates.

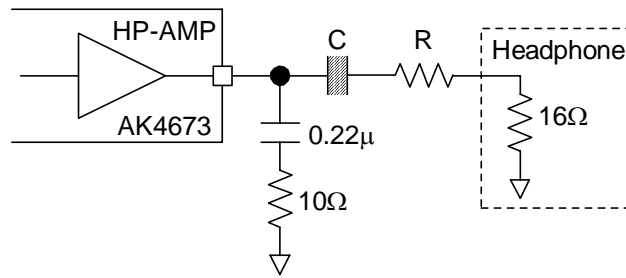


Figure 56. External Circuit Example of Headphone

| HPG bit | R [Ω] | C [μF] | fc [Hz] BOOST =OFF | fc [Hz] BOOST =MIN @fs=44.1kHz | Output Power [mW]@0dBFS | | |
|---------|-------|--------|--------------------------|---|-------------------------|------------------------|----------------------|
| | | | | | HVDD=3.0V AVDD=3.0V | HVDD=3.3V AVDD=3.3V | HVDD=5V AVDD=3.3V |
| 0 | 0 | 220 | 45 | 17 | 25.3 | 30.6 | 30.6 |
| | | 100 | 100 | 43 | | | |
| | 6.8 | 100 | 70 | 28 | 12.5 | 15.1 | 15.1 |
| | | 47 | 149 | 78 | | | |
| | 16 | 100 | 50 | 19 | 6.3 | 7.7 | 7.7 |
| | | 47 | 106 | 47 | | | |
| 1 | 0 | 220 | 45 | 17 | 51 (Note 41) | 62 (Note 41) | 70 |
| | | 100 | 100 | 43 | | | |
| | 100 | 22 | 62 | 25 | 1.1 | 1.3 | 1.3 |
| | | 10 | 137 | 69 | | | |

Note 40. Output power at 16Ω load.

Note 41. Output signal is clipped.

Table 55. External Circuit Example

<Headphone-Amp PSRR>

When HVDD is directly supplied from the battery in the mobile phone system, RF noise may influence headphone output performance. When VBAT bit is set to “1”, HP-Amp PSRR for the noise applied to HVDD is improved. In this case, HP-Amp common voltage is 0.64 x AVDD (typ). When AVDD is 3.3V, common voltage is 2.1V. Therefore, when HVDD voltage becomes lower than 4.2V, the output signal will be clipped easily.

| VBAT bit | 0 | 1 |
|--------------------|------------|-------------|
| Common Voltage [V] | 0.5 x HVDD | 0.64 x AVDD |

Table 56. HP-Amp Common Voltage

<Wired OR with External Headphone-Amp>

When PMVCM=PMHPL=PMHPR bits = “0” and HPZ bit = “1”, HP-Amp is powered-down and HPL/R pins are pulled-down to VSS2 by 200kΩ (typ). In this setting, it is available to connect HP-Amp of AK4673 and external single supply HP-Amp by “wired OR”. In this mode, power supply current is 20μA(typ).

| PMVCM | PMHPL/R | HPMTN | HPZ | Mode | HPL/R pins | |
|-------|---------|-------|-----|-------------------|--------------------|-----------|
| x | 0 | x | 0 | Power-down & Mute | VSS2 | (default) |
| 0 | 0 | x | 1 | Power-down | Pull-down by 200kΩ | |
| 1 | 1 | 0 | x | Mute | VSS2 | |
| 1 | 1 | 1 | x | Normal Operation | Normal Operation | |

Table 57. HP-Amp Mode Setting (x: Don't care)

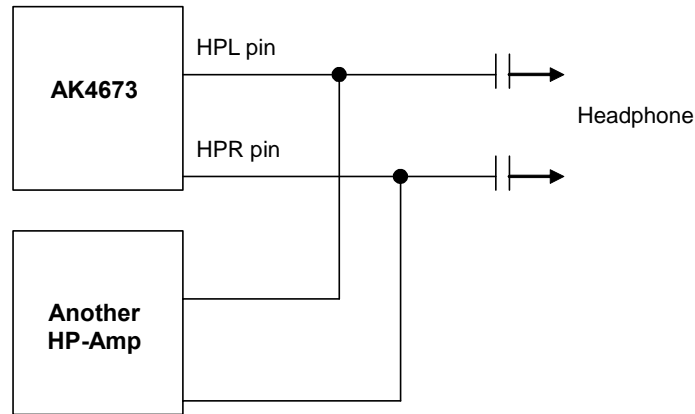


Figure 57. Wired OR with External HP-Amp

<Analog Mixing Circuit for Headphone Output>

When AIN3 bit = "0", DACH, MINH, LINH2, RINH2, LINH4 and RINH4 bits controls each path switch. MIN path mixing gain is -20dB(typ)@HPG bit = "0" when the external input resistance is 20kΩ. LIN2, RIN2, LIN4, RIN4 and DAC pathes mixing gain is 0dB(typ)@HPG bit = "0".

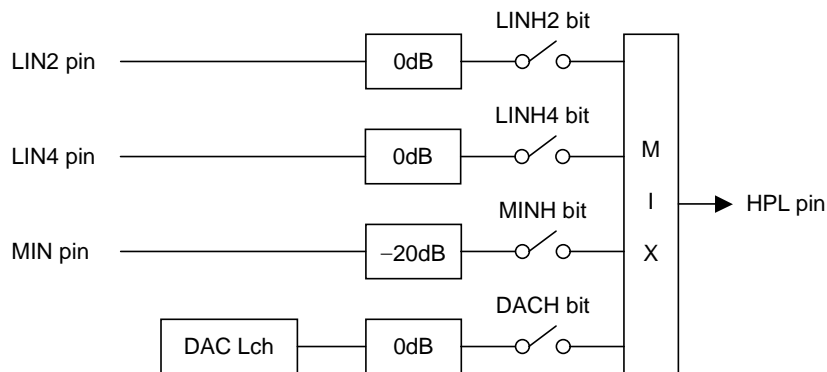


Figure 58. HPL Mixing Circuit (AIN3 bit = "0", HPG bit = "0")

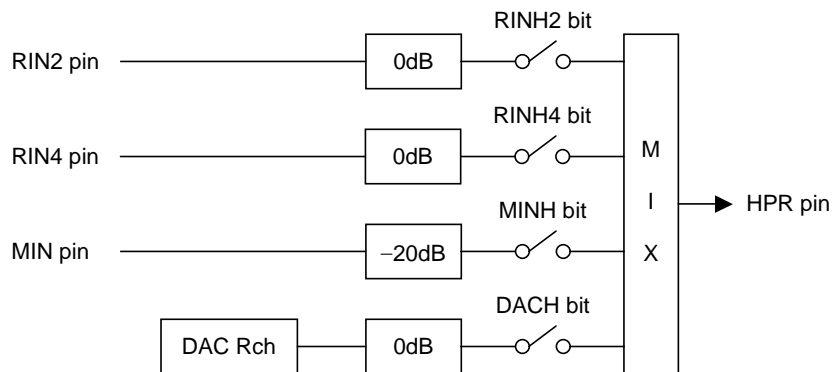


Figure 59. HPR Mixing Circuit (AIN3 bit = "0", HPG bit = "0")

When AIN3 bit = "1", DACH, LINH2, RINH2, LINH3, RINH3, LINH4, RINH4, MICL3 and MICR3 bits controls each path switch.

All paths mixing gain is 0dB(typ)@HPG bit = "0".

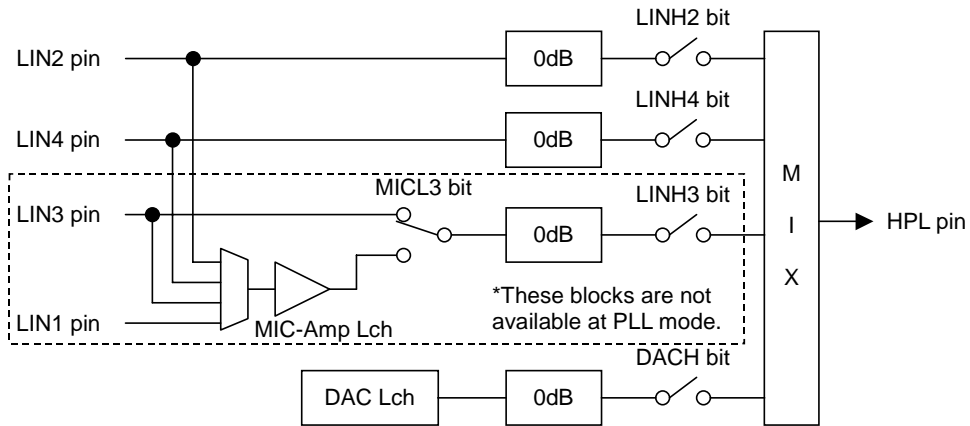


Figure 60. HPL Mixing Circuit (AIN3 bit = "1", HPG bit = "0")

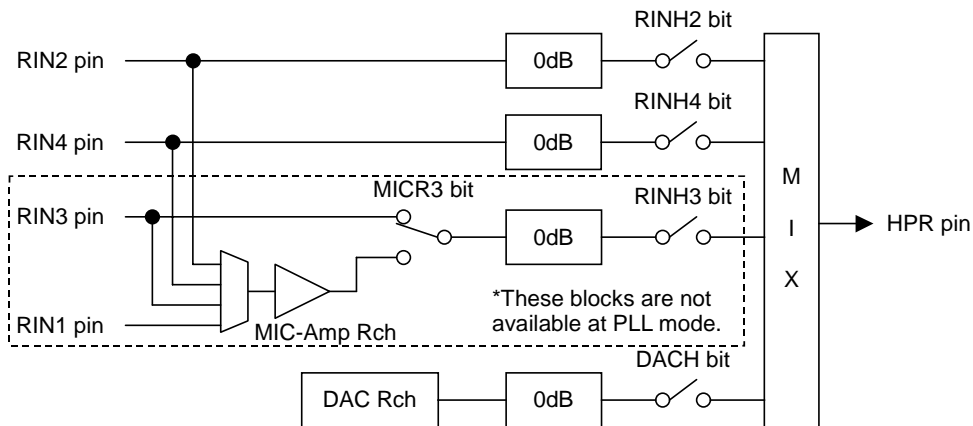


Figure 61. HPR Mixing Circuit (AIN3 bit = "1", HPG bit = "0")

TSC OPERATION OVERVIEW

■ A/D Converter for Touch Screen

The AK4673 incorporates a 12-bit successive approximation resistor (SAR) A/D converter for position measurement. The architecture is based on a capacitive redistribution algorithm, and an internal capacitor array functions as the sample/hold (S/H) circuit.

The SAR A/D converter output is a straight binary format as shown below:

| Input Voltage | Output Code |
|--|-------------|
| $(\Delta VREF - 1.5LSB) \sim \Delta VREF$ | FFFH |
| $(\Delta VREF - 2.5LSB) \sim (\Delta VREF - 1.5LSB)$ | FFE H |
| ----- | ----- |
| 0.5LSB \sim 1.5LSB | 001H |
| 0 \sim 0.5LSB | 000H |

$$\Delta VREF: (VREF+) - (VREF-)$$

Table 58 Output Code

■ The Block Diagram of TSC block

Figure 62 shows the block diagram in touch screen controller block that consists of the 12bit ADC and control block of the driver switches and peninterrupt output.

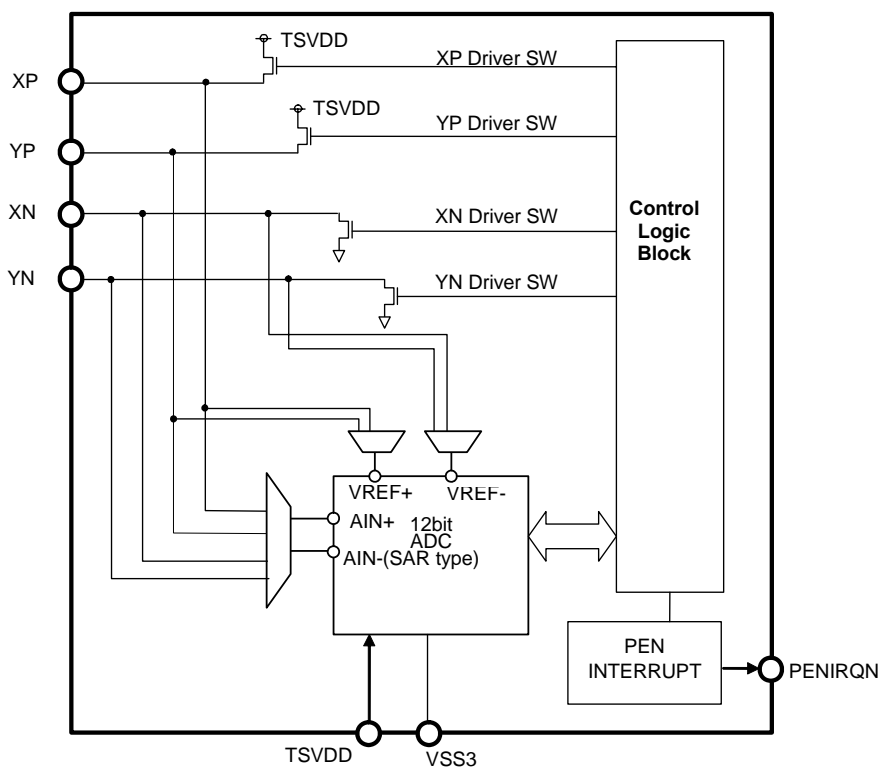


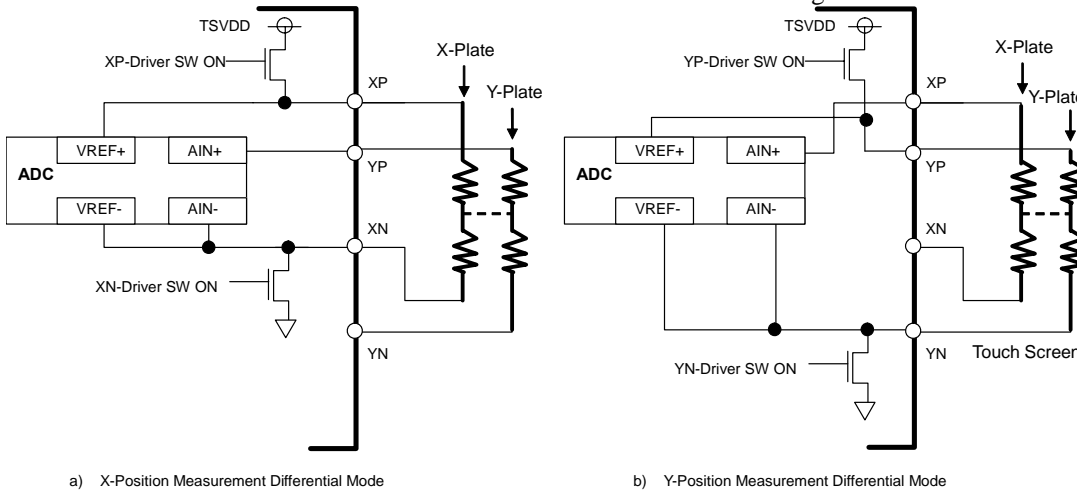
Figure 62 Touch Screen Controller Block Diagram

■ The Position Detection of Touch Screen

A position detecting (X, Y position) on the touch panel is selected by the control command via the A2, A1, A0 bits in the control register. The mode of the position detecting is differential mode, the full scale (ΔV_{REF}) is the differential voltage between the non-inverting terminal and the inverting terminal of the measured axis (e.g. X-axis measurement: $\Delta V_{REF} = V_{XP} - V_{XN}$). The voltage difference on the A/D converter (ΔAIN) is the voltage between non-inverting terminals of the non-measured axis and the inverting terminal of the measured axis. (E.g. $\Delta AIN = (AIN+) - (AIN-) = V_{YP} - V_{XN}$) The voltage difference (ΔAIN) is charged to the internal capacitor array during the sampling period. No current flows into the internal capacitor after the capacitor has been charged completely.

The required settling time to charge the internal capacitor array depends on the source impedance (R_{in}). If the source impedance is 600 ohm, the settling time needs at least $2.5\mu s$ (1 clock cycle period of SCL 400 KHz)

The position on the touch screen is detected by taking the voltage of one axis when the voltage is supplied between the two terminals of another axis. At least two A/D conversions are needed to get the two-dimensional (X/Y axis) position.



The X-plate and Y-plate are connected on the dotted line when the panel is touched.

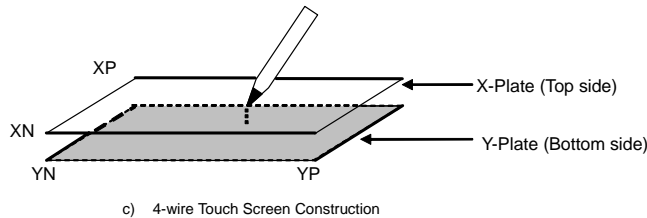


Figure 63 Axis Measurements

The differential mode position detection is typically more accurate than the single-ended mode. As the full scale of single-ended mode is fixed to the VCC, input voltage may exceed the full-scale reference voltage. This problem does not occur in differential mode. In addition to this, the differential mode is less influenced by power supply voltage variation due to the ratio-metric measurement.

■ The Pen Pressure Measurement

The touch screen pen pressure can be derived from the measurement of the contact resistor between two plates. The contact resistance depends on the size of the depressed area and the pressure. The area of the spot is proportional to the contact resistance. This resistance (R_{touch}) can be calculated using two different methods.

The first method is applied when the total resistance of the X-plate sheet is already known. The resistance, R_{touch} , is calculated from the results of three conversions, X-position, Z1-Position, and Z2-Position, and then using the following formula:

$$R_{touch} = (R_{xplate}) * (X_{position}/4096) * [(Z2/Z1) - 1]$$

The second method is applied when both the resistances of the X-plate and Y-plate are known. The resistance, R_{touch} , is calculated from the results of three conversions, X-position, Y-Position, and Z1-Position, and then using the following formula:

$$R_{touch} = (R_{xplate} * X_{position}/4096) * [(4096/Z1) - 1] - R_{yplate} * [1 - (Y_{position}/4096)]$$

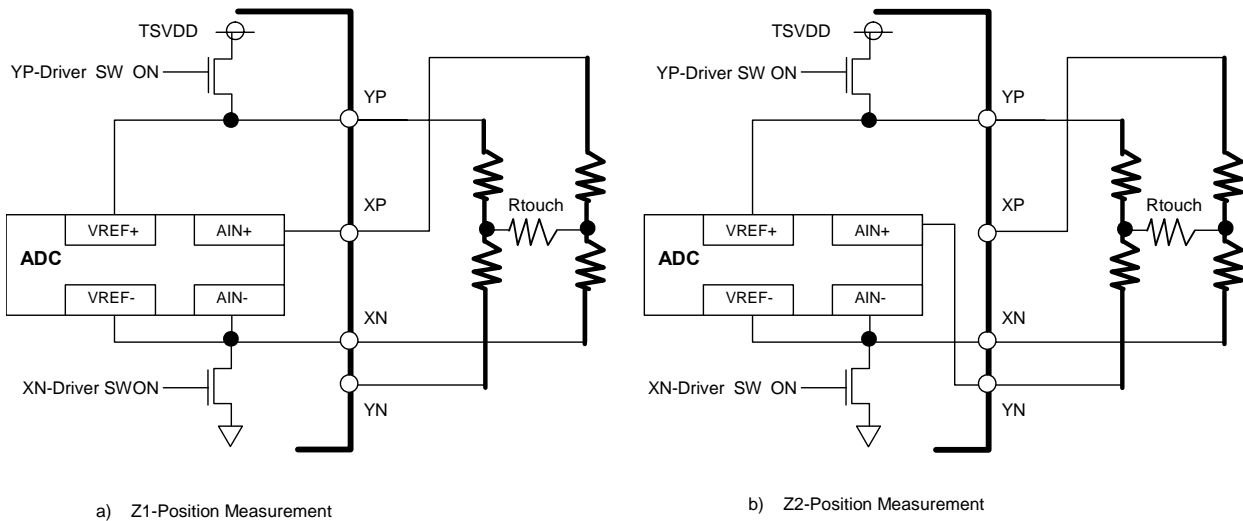


Figure 64 Pen Pressure Measurements

■ Digital I/F

The AK4673 operates with uP via I²C bus and supports the standard-mode (100 KHz) and the fast-mode (400KHz). Please note that the AK4673 operates in those two modes and does not support a High speed mode I²C-bus system (3.4MHz). The AK4673 can operate as a slave device on the I²C bus network.

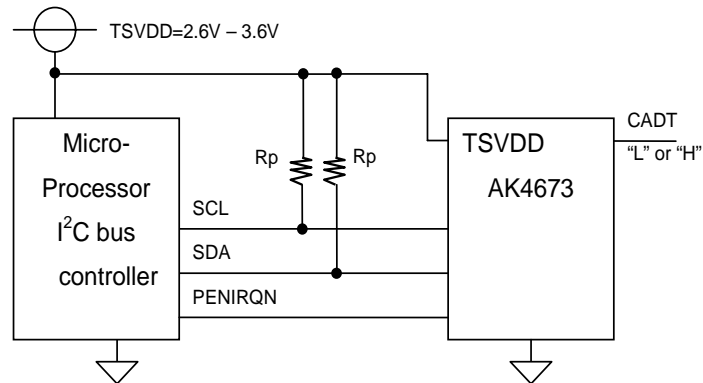


Figure 65 Digital I/F

■ Serial Control Interface

The AK4673 supports the fast-mode I²C-bus (max: 400 kHz). Pull-up resistors at the SDA and the SCL pins should be connected to (TVDD1/ TSVDD +0.3) V or less voltage. The TVDD1 pin and the TSVDD pin should be connected together on the same I2C bus.

[Start condition and Stop condition]

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. All sequences start by the START condition or Repeated Start Condition. Repeated Start condition is the same signal tradition as Start condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. All sequences are terminated by the STOP or Repeated Start condition. Repeated Start is also the Start condition of next transfer so that I²C bus cannot be idle.

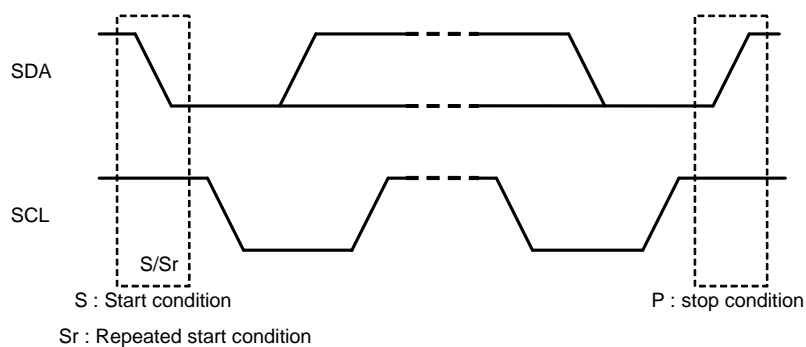


Figure 66 START and STOP Conditions

[Data transfer]

All commands are preceded by a START condition. After the START condition, a slave address is sent. After the AK4673 recognizes the START condition, the device interfaced to the bus waits for the slave address to be transmitted over the SDA line. If the transmitted slave address matches an address for one of the devices, the designated slave device pulls the SDA line to LOW (ACKNOWLEDGE). The data transfer is always terminated by a STOP condition generated by the master device.

[Data validity]

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW except for the START and the STOP condition.

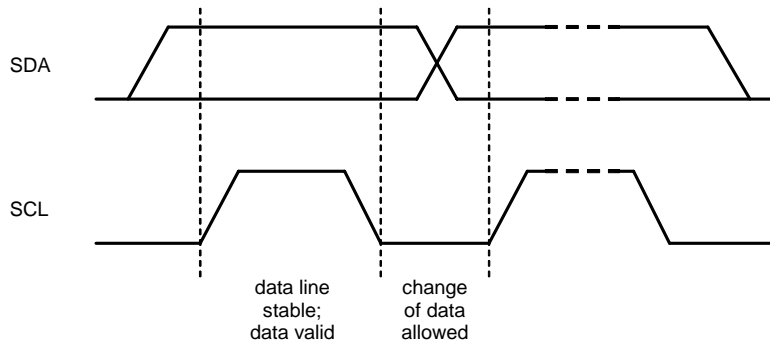


Figure 67 Bit Transfer on the I2C-Bus

[ACKNOWLEDGE]

ACKNOWLEDGE is a software convention used to indicate successful data transfers. The transmitting device will release the SDA line (HIGH) after transmitting eight bits. The receiver must pull down the SDA line during the acknowledge clock pulse so that that it remains stable “L” during “H” period of this clock pulse. The AK4673 will generate an acknowledge after each byte is received.

In the read mode, the slave, AK4673 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no STOP condition is generated by the master, the slave will continue to transmitting the data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the STOP condition.

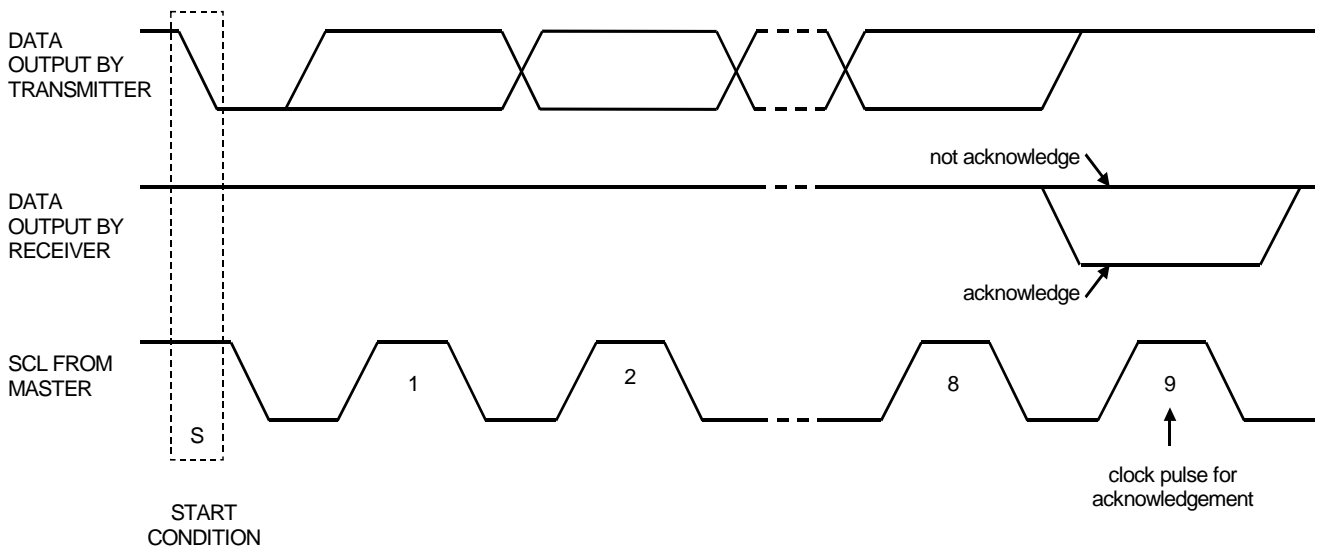
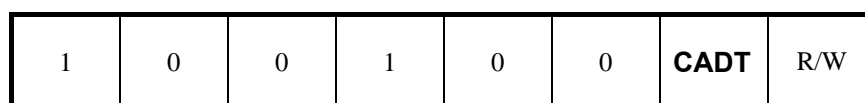


Figure 68 Acknowledge

A) TSC Control
[Address Byte]

The sequence of writing data is shown [Figure 71](#). The address byte, which includes seven bits of slave address and one bit of R/W bit, is sent after the START condition. If the transmitted slave address matches an address for one of the device, the receiver which was addressed pulls down the SDA line (acknowledge).

The most significant six bits of the slave address are fixed as “100100”. The next one bit is CADT (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CADT pin) sets CADT bit. The eighth bit (LSB) of the address byte (R/W bit) defines whether the master requests a write or read operation. A “1” indicates that the read operation is to be executed. A “0” indicates that the write operation is to be executed.



(CADT should match with CADT pins)

Figure 69 Address Byte

[WRITE Operations]

The second byte that followed by address byte consists of the control command byte of the AK4673. The operational mode is determined by control command. The bit format is MSB first and 8 bits width. Control command is described in the [Table 60](#). The AK4673 generates an acknowledge after each byte is received. A control command transfer is terminated by a STOP condition or Repeated Start condition generated by the master. Refer to the [Table 60](#) in detail.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|-----|------|----|
| S | A2 | A1 | A0 | X1 | PD0 | MODE | X2 |

Figure 70 Control Command Byte (X1, X2 : Don't care)

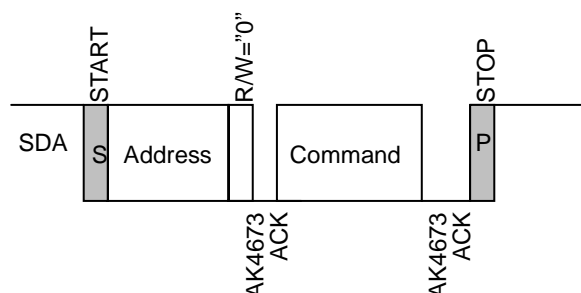


Figure 71 Single Write Transmission Sequence

[READ Operation]

The operation mode is determined by the write command just before read operation.

AK4673 features two methods of read operation, single read operation and continuous read operation. The continuous read operation is a series of single read operation. Each single read operation in continuous read operation makes the AK4673 updated A/D conversion on each read operation. Write operation does not need to issue before each read operations are executed.

The channel selection of the AK4673 is defined by the control command just before READ operation. When the address byte with R/W = "1" read operations are executed. A/D readout format is MSB first, 1byte or 2bytes width. Upper 8bits are valid on 8-bit mode and upper 12 bits are valid, and lower 4 bits are filled with zero on 12-bit mode.

[Single READ mode]

Read operation begins with a START condition followed by the address byte with R/W = "1". When the address matches address byte of the AK4673 ([Figure 68](#)), the AK4673 generates ACK. After transmission of the address byte, the master receives upper 8bit A/D data first, and generates ACK. The AK4673 transmits the remaining 4-bit A/D data and followed by 4-bit zero data (12bit mode). Master device receives 8bit A/D data (8bit mode). The master then generates NACK and stop condition or repeated start condition.

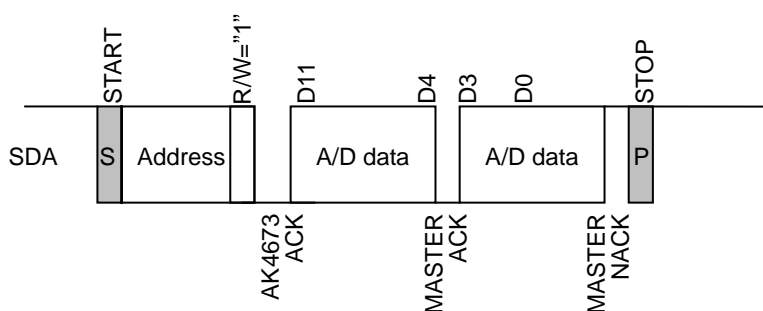


Figure 72 Single A/D data Read Sequence (12-bit mode)

[Continuous Read mode]

This continuous read operation enables the higher sampling rate and lower processor load than a single read operation. Because once control command is sent, it does not need to update control command on each read operation until another control command is rewritten.

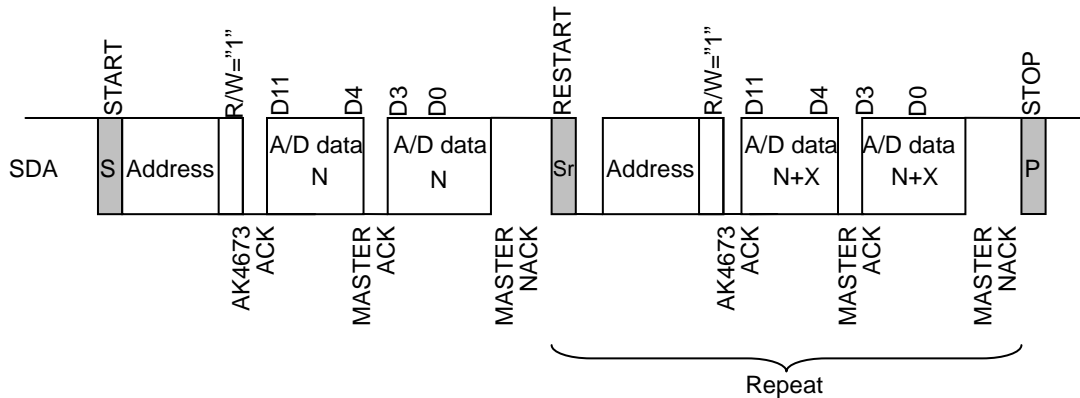


Figure 73 Continuous A/D data Read Sequence

■ Power on Sequence

It is recommended that the control command must be sent to fix the internal register when power up. This initiates all registers such as A2-0 bit, PD0 bit, and MODE bit. Once sending command to fix the internal register after first power up, the state of the AK4673 is held on the known-condition of state to ensure that the AK4673 is going into desire mode to realize lowest mode. A command with PD0= “0” should be sent so that the AK4673 will be set in the lowest power down mode.

■ Sleep mode

The AK4673 supports the sleep mode that enables touch panel interface to put open state and disables pen interrupt function. The AK4673 goes into the sleep mode when control command is sent to the AK4673 as shown Table 59. The selection of the sleep mode is set by “MODE” bit of the control command. The state of both the output of the PENIRQ pin and the connection with touch panel interface (XP, YP, XN, and YN) are the following Table 59. AK4673 keeps the sleep mode until next control command is sent.

| Command | MODE bit | PENIRQ | Touch panel |
|----------|----------|------------|-------------|
| 0111XX1X | 1 | Hi-z | Open |
| 0111XX0X | 0 | “H” output | Open |

Table 59 Sleep Command Setting

The timing of going into the sleep mode is the rising edge of the 16th SCL of the write operation. A/D conversion does not execute when the sleep command is sent. The SDA pin is “H” since SDA is pull up. In order to go to normal mode from sleep mode, the command (S= “1”) is sent. The timing of going back to normal mode is the rising edge of the 16th SCL. When the sleep command is sent again under the sleep mode the mode continues the same as before. The initial state after power up is in normal mode.

■ Control Command

The control command, 8 bits, provided to the AK4673 via SDA, is shown in the following table. This command includes start bit, channel selection bit, power-down bit and resolution bit. The AK4673 latches the serial command at the rising edge of SCL. Refer to the detailed information regarding the bit order, function, the status of driver switch, ADC input as shown in [Table 60](#).

| BIT | Name | Function |
|-----|-------|---|
| 7 | S | Start Bit. “1” Accelerate and Axis Command, “0”: Sleep mode Command |
| 6-4 | A2-A0 | Channel Selection Bits. Analog inputs to the A/D converter and the activated driver switches are selected. Please see the following table for the detail. |
| 3 | X1 | Don't care |
| 2 | PD0 | Power down bit (refer to power-down control) |
| 1 | MODE | Resolution of A/D converter. “0”: 12 bit output “1”: 8 bit output when S bit is “1”. Sleep mode selection when S bit is “0”. |
| 0 | X2 | Don't care |

| S | Input | | | Status of Driver Switch | | | | ADC input (Δ AIN) | | Reference Voltage (Δ VREF) | | Note |
|---|-------|----|----|-------------------------|-----|-----|-----|---------------------------|------|------------------------------------|-------|--------------------------|
| | A2 | A1 | A0 | XP | XN | YP | YN | AIN+ | AIN- | VREF+ | VREF- | |
| 0 | 1 | 1 | 1 | | | | | | | | | Sleep |
| 1 | 0 | 0 | 0 | ON | ON | OFF | OFF | YP | XN | XP | XN | Accelerate X-Driver |
| 1 | 0 | 0 | 1 | OFF | OFF | ON | ON | XP | YN | YP | YN | Accelerate Y-Driver |
| 1 | 0 | 1 | 0 | OFF | ON | ON | OFF | XP | XN | YP | XN | Accelerate Y+, X- Driver |
| 1 | 0 | 1 | 1 | OFF | ON | ON | OFF | YN | XN | YP | XN | |
| 1 | 1 | 0 | 0 | ON | ON | OFF | OFF | YP | XN | XP | XN | X-axis |
| 1 | 1 | 0 | 1 | OFF | OFF | ON | ON | XP | YN | YP | YN | Y-axis |
| 1 | 1 | 1 | 0 | OFF | ON | ON | OFF | XP (Z1) | XN | YP | XN | Z1 (Pen Pressure) |
| 1 | 1 | 1 | 1 | OFF | ON | ON | OFF | YN (Z2) | XN | YP | XN | Z2 (Pen Pressure) |

Table 60 Control Command List

■ Power-down Control

A/D converter and power-down control of touch driver switch are determined by PD0 bit.

| PD0 | PENIRQN | Function |
|-----|----------|---|
| 0 | Enabled | Auto power-down Mode A/D converter is automatically powered up at the start of the conversion, and goes to power-down state automatically at the end of the conversion. All touch screen driver switches except for YN switch are turned off and relative pins are open state. Only YN driver switch is turned ON and the YN pin is forced to the ground in this case. PEN interrupt function is enabled except for the sampling time and conversion time. |
| 1 | Disabled | ADC ON Mode When X-axis or Y-axis are selected on the write operation with PD0 = “1” A/D converter and touch panel driver are always powered up until next conversion. This mode is effective if more settling time is required to suppress the electrical bouncing of touch plate. PEN interrupt function is disabled and PENIRQN is forced to “L” state |

Table 61 Power -Down Control

■ WRITE Operation Sequence

The selection of channel input of the AK4673 is determined by a command byte. When accelerate command (A2= "0") is sent, the switch on timing of the driver switch is 18th falling edge of SCL regardless of PD0 bit. The accelerate command is to accelerate the timing of desired driver SW ON to ensure that AK4673 needs more settling time. Actually sampling timing is on the time of READ operation, it is possible to take settling time longer even when the impedance of the touch screen is large.

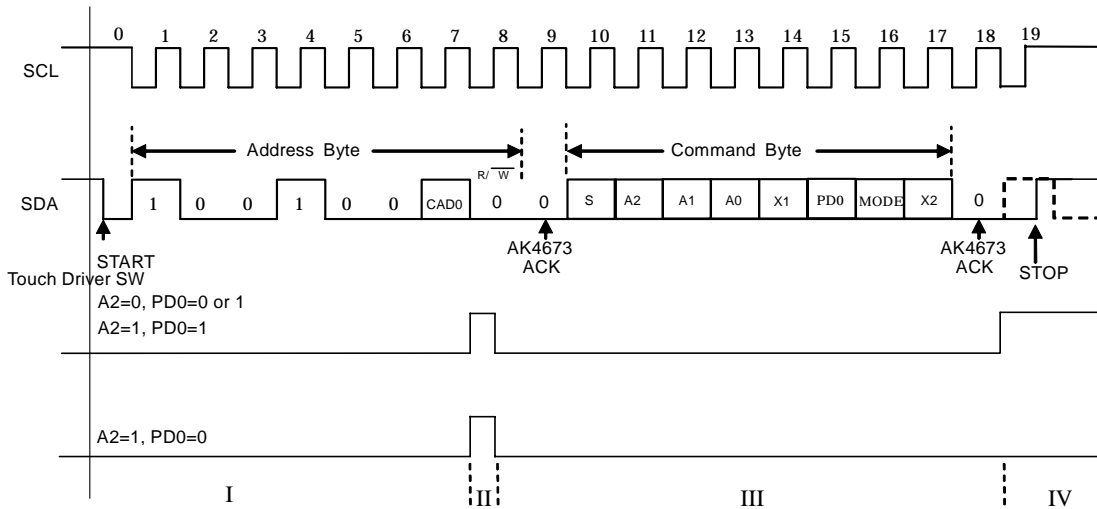


Figure 74 write operation and Driver SW timing

■ READ Operation Sequence

A/D conversion is synchronized with SCL. Sampling time is the one SCL clock period (SCL7↓~ SCL8↓) on the end of writing address byte and then hold. A/D conversion is held on the next 12 SCL period (except MASTER ACK). After address byte is sent, the readout sequence starts with an acknowledge, which is the response of the AK4673 when the address matches. The MSB data byte will follow (D11~D4) then issued acknowledge by master. The LSB data byte (D3~D0, followed four "0") will be followed by NOT acknowledge bit (NACK) from master in order to terminate the read transfer. The master will then issued STOP that ends read operation or Repeated Start condition that keeps write or read operation. The master will issue Repeated Start Condition or START condition followed by read operation again. AK4673 repeats A/D data updated [continuous read operation]. Master must issue STOP condition after terminating the last read out of A/D data.

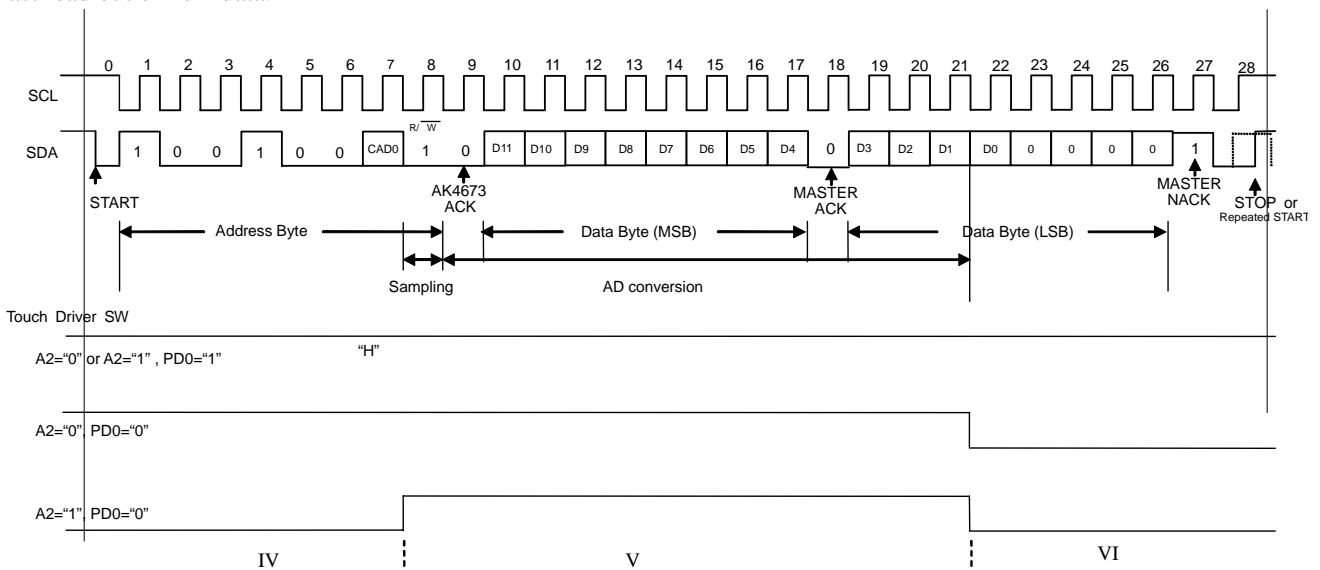


Figure 75 Read data Sequence

■ Pen Interrupt

The AK4673 has a pen-interrupt function to detect the pen touch on the touch panel. This function will be used as the interrupt of the microprocessor. Pen interrupt function is enabled at power-down state. YN driver is on and this pin is connected to GND at the power down state. And the XP pin is pulled up via an internal resistor (R_i), typically $10k\Omega$. If the touch plate is touched by pen or stylus, the current flows via $\langle VCC \rangle - \langle R_i \rangle - \langle XP \rangle - \langle \text{the plates} \rangle - \langle YN \rangle - \langle GND \rangle$. The resistance of the plate is generally $1k\Omega$ or less, the PENIRQN pin is force to “L” level. If the pen is released, the PENIRQN pin returns “H” level because two plates are disconnected, and the current does not flow via two plates. The transition of PENIRQN is related to PD0 bit. PD0 bit is updated as shown below. (Please see “power-down control” for the detail. Once the control command PD0= “1” is sent the pen-interrupt function is disabled.

The clock number under the write and the read operation refer to [Figure 74](#) and [Figure 14](#).

- I. The period from start condition to SCL7 \downarrow
The level transition of the PENIRQN pin is determined by PD0 bit of the previous command. When the previous command with PD0= “0” the pen-interrupt function will be enabled. The PENIRQN pin is low when the panel is touch, the PENIRQN pin is “H” when the panel is untouched. When the previous command with PD0= “1” is sent PENIRQN pin is low regardless of pen-touch
- II. The period SCL7 \downarrow to SCL8 \uparrow on the write operation
The level of the PENIRQN pin is always low regardless of PD0 bit and the state of panel (touched/untouched)
- III. The period from SCL8 \uparrow to SCL18 \downarrow on the write operation
The level transition of the PENIRQN pin is determined by PD0 bit of the previous command. When the previous command with PD0= “0” the pen-interrupt function will be enabled. The PENIRQN pin is low when the panel is touch, the PENIRQN pin is “H” when the panel is untouched. When the previous command with PD0= “1” is sent PENIRQN pin is low regardless of pen-touch
- IV. The period from SCL18 \downarrow on the write operation to SCL7 \downarrow on the read operation
The level of PENIRQN pin is determined by the A2 bit and PD0 bit of the present command. The PENIRQN pin is always low regardless pen-touch when command with A2 = “1” or PD0 = “1” is set. The PENIRQN is determined by the pen-touch (touched/untouched) when command with A2= “1” and PD0= “1” is sent.
- V. The period from SCL7 \downarrow to SCL21 \downarrow on the write operation
The AD input will sample the hold and the conversion will be done during this period. PENIRQN is always low.
- VI. The period after SCL21 \downarrow on the read operation
The level transition of the PENIRQN pin is determined by PD0 bit of the present command. When the present command PD0= “0” is sent the pen-interrupt function will be enabled. The PENIRQN pin is low when the panel is touched. The PENIRQN pin is “H” when the panel is untouched. When the present command PD0= “1” are sent the PENIRQN pin is low regardless of pen-touch.

It is recommended that the processor will mask the pseudo interrupt while the control command is issued or AD data is sent to processor.

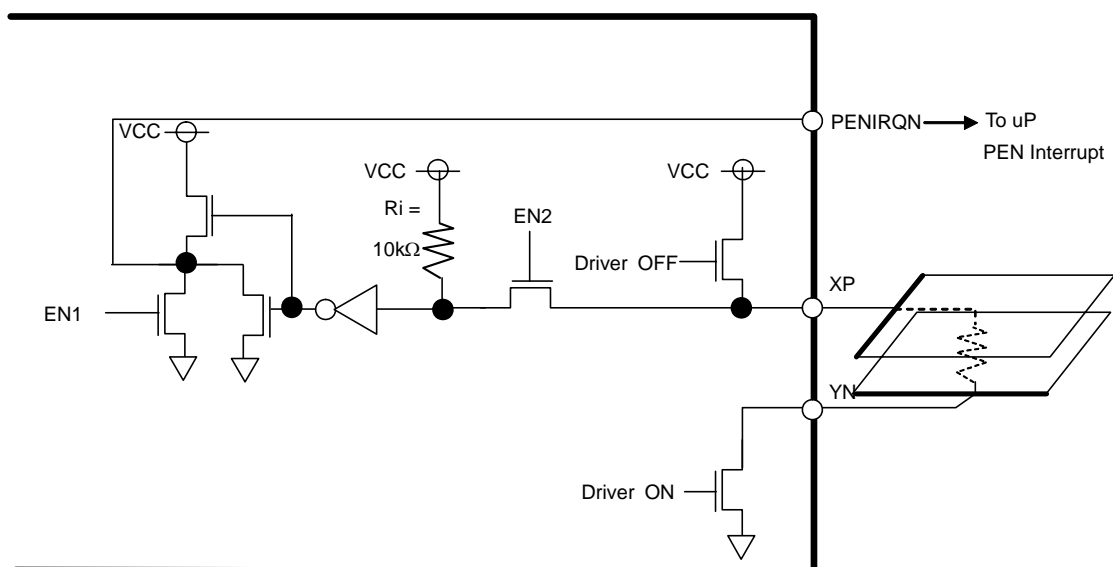


Figure 76 Pen interrupt function block

B) Audio Control

(1)-1. WRITE Operations

Figure 77 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 66). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant six bits of the slave address are fixed as “001001”. The next bit is CADA (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CADA pin) sets these device address bits (Figure 78). If the slave address matches that of the AK4673, the AK4673 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 68). A R/W bit value of “1” indicates that the read operation is to be executed. A “0” indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4673. The format is MSB first, and those most significant 2-bits are fixed to zeros (Figure 79). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 80). The AK4673 generates an acknowledge after each byte is received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 66).

The AK4673 can perform more than one byte write operation per sequence. After receiving of the third byte the AK4673 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 24H prior to generating a stop condition, the address counter will “roll over” to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 67) except for the START and STOP conditions.

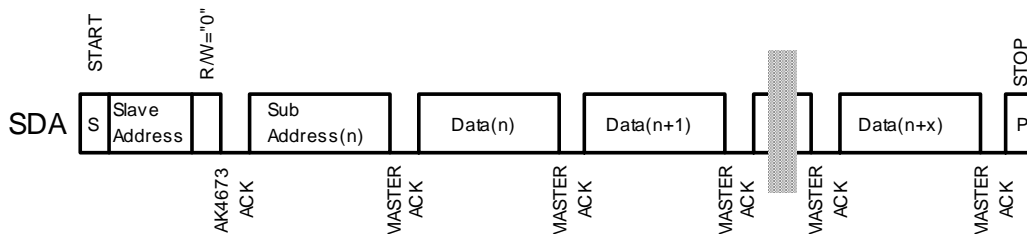
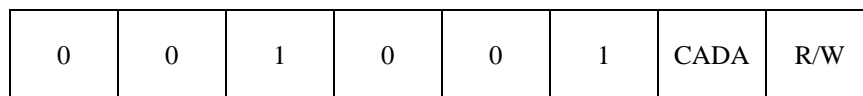


Figure 77. Data Transfer Sequence at the I²C-Bus Mode



(CADA should match with CADA pins)

Figure 78. The First Byte

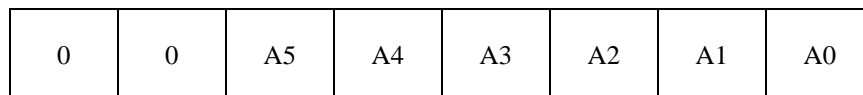


Figure 79. The Second Byte

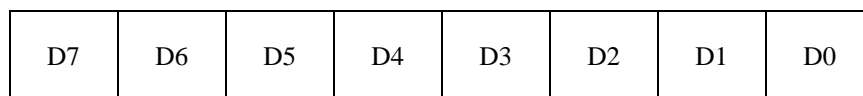


Figure 80. Byte Structure after the second byte

(1)-2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4673. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after receiving of the first data word. After receiving each data packet the internal 6-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 24H prior to generating a stop condition, the address counter will "roll over" to 00H and the data of 00H will be read out.

The AK4673 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

(1)-2-1. CURRENT ADDRESS READ

The AK4673 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receiving of the slave address with R/W bit set to "1", the AK4673 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4673 ceases transmission.

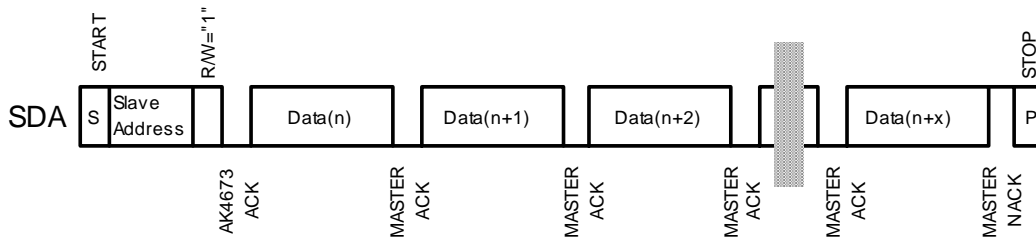


Figure 81. CURRENT ADDRESS READ

(1)-2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit set to "1". The AK4673 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4673 ceases transmission.

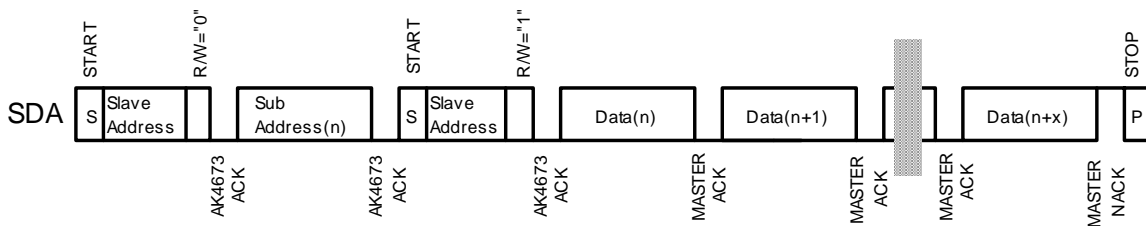


Figure 82. RANDOM ADDRESS READ

■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------------------|---------|---------|---------|---------|---------|---------|--------|--------|
| 00H | Power Management 1 | 0 | PMVCM | PMMIN | 0 | PMLO | PMDAC | 0 | PMADL |
| 01H | Power Management 2 | HPZ | HPMTN | PMHPL | PMHPR | M/S | 0 | MCKO | PMPLL |
| 02H | Signal Select 1 | 0 | 0 | 0 | DACL | 0 | PMMP | 0 | MGAIN0 |
| 03H | Signal Select 2 | LOVL | LOPS | MGAIN1 | 0 | 0 | MINL | 0 | 0 |
| 04H | Mode Control 1 | PLL3 | PLL2 | PLL1 | PLL0 | BCKO | 0 | DIF1 | DIF0 |
| 05H | Mode Control 2 | PS1 | PS0 | FS3 | MSBS | BCKP | FS2 | FS1 | FS0 |
| 06H | Timer Select | DVTM | WTM2 | ZTM1 | ZTM0 | WTM1 | WTM0 | RFST1 | RFST0 |
| 07H | ALC Mode Control 1 | 0 | 0 | ALC | ZELMN | LMAT1 | LMAT0 | RGAIN0 | LMTH0 |
| 08H | ALC Mode Control 2 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| 09H | Lch Input Volume Control | IVL7 | IVL6 | IVL5 | IVL4 | IVL3 | IVL2 | IVL1 | IVL0 |
| 0AH | Lch Digital Volume Control | DVL7 | DVL6 | DVL5 | DVL4 | DVL3 | DVL2 | DVL1 | DVL0 |
| 0BH | ALC Mode Control 3 | RGAIN1 | LMTH1 | 0 | 0 | 0 | 0 | VBAT | 0 |
| 0CH | Rch Input Volume Control | IVR7 | IVR6 | IVR5 | IVR4 | IVR3 | IVR2 | IVR1 | IVR0 |
| 0DH | Rch Digital Volume Control | DVR7 | DVR6 | DVR5 | DVR4 | DVR3 | DVR2 | DVR1 | DVR0 |
| 0EH | Mode Control 3 | 0 | LOOP | SMUTE | DVOLC | BST1 | BST0 | DEM1 | DEM0 |
| 0FH | Mode Control 4 | 0 | 0 | 0 | 0 | IVOLC | HPM | MINH | DACH |
| 10H | Power Management 3 | INR1 | INL1 | HPG | MDIF2 | MDIF1 | INR0 | INL0 | PMADR |
| 11H | Digital Filter Select | GN1 | GN0 | 0 | FIL1 | EQ | FIL3 | 0 | 0 |
| 12H | FIL3 Co-efficient 0 | F3A7 | F3A6 | F3A5 | F3A4 | F3A3 | F3A2 | F3A1 | F3A0 |
| 13H | FIL3 Co-efficient 1 | F3AS | 0 | F3A13 | F3A12 | F3A11 | F3A10 | F3A9 | F3A8 |
| 14H | FIL3 Co-efficient 2 | F3B7 | F3B6 | F3B5 | F3B4 | F3B3 | F3B2 | F3B1 | F3B0 |
| 15H | FIL3 Co-efficient 3 | 0 | 0 | F3B13 | F3B12 | F3B11 | F3B10 | F3B9 | F3B8 |
| 16H | EQ Co-efficient 0 | EQA7 | EQA6 | EQA5 | EQA4 | EQA3 | EQA2 | EQA1 | EQA0 |
| 17H | EQ Co-efficient 1 | EQA15 | EQA14 | EQA13 | EQA12 | EQA11 | EQA10 | EQA9 | EQA8 |
| 18H | EQ Co-efficient 2 | EQB7 | EQB6 | EQB5 | EQB4 | EQB3 | EQB2 | EQB1 | EQB0 |
| 19H | EQ Co-efficient 3 | 0 | 0 | EQB13 | EQB12 | EQB11 | EQB10 | EQB9 | EQB8 |
| 1AH | EQ Co-efficient 4 | EQC7 | EQC6 | EQC5 | EQC4 | EQC3 | EQC2 | EQC1 | EQC0 |
| 1BH | EQ Co-efficient 5 | EQC15 | EQC14 | EQC13 | EQC12 | EQC11 | EQC10 | EQC9 | EQC8 |
| 1CH | FIL1 Co-efficient 0 | F1A7 | F1A6 | F1A5 | F1A4 | F1A3 | F1A2 | F1A1 | F1A0 |
| 1DH | FIL1 Co-efficient 1 | F1AS | 0 | F1A13 | F1A12 | F1A11 | F1A10 | F1A9 | F1A8 |
| 1EH | FIL1 Co-efficient 2 | F1B7 | F1B6 | F1B5 | F1B4 | F1B3 | F1B2 | F1B1 | F1B0 |
| 1FH | FIL1 Co-efficient 3 | 0 | 0 | F1B13 | F1B12 | F1B11 | F1B10 | F1B9 | F1B8 |
| 20H | Power Management 4 | PMAINR4 | PMAINL4 | PMAINR3 | PMAINL3 | PMAINR2 | PMAINL2 | PMMICR | PMMICL |
| 21H | Mode Control 5 | 0 | 0 | MICR3 | MICL3 | L4DIF | MIX | AIN3 | LODIF |
| 22H | Lineout Mixing Select | LOM | LOM3 | RINR4 | LINL4 | RINR3 | LINL3 | RINR2 | LINL2 |
| 23H | HP Mixing Select | 0 | HPM3 | RINH4 | LINH4 | RINH3 | LINH3 | RINH2 | LINH2 |
| 24H | Reserved | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Note 42. PDN pin = "L" resets the registers to their default values.

Note 43. Unused bits must contain a "0" value.

■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|----|-------|-------|----|------|-------|----|-------|
| 00H | Power Management 1 | 0 | PMVCM | PMMIN | 0 | PMLO | PMDAC | 0 | PMADL |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMADL: MIC-Amp Lch and ADC Lch Power Management

0: Power-down (default)

1: Power-up

When the PMADL or PMADR bit is changed from “0” to “1”, the initialization cycle ($1059/f_s=24\text{ms}$ @44.1kHz) starts. After initializing, digital data of the ADC is output.

PMDAC: DAC Power Management

0: Power-down (default)

1: Power-up

PMLO: Stereo Line Out Power Management

0: Power-down (default)

1: Power-up

PMMIN: MIN Input Power Management

0: Power-down (default)

1: Power-up

PMMIN or PMAINL3 bit should be set to “1” for playback.

PMVCM: VCOM Power Management

0: Power-down (default)

1: Power-up

When any blocks are powered-up, the PMVCM bit must be set to “1”. PMVCM bit can be set to “0” only when all power management bits of 00H, 01H, 02H, 10H, 20H and MCKO bits are “0”.

Each block can be powered-down respectively by writing “0” in each bit of this address. When the PDN pin is “L”, all blocks are powered-down regardless of setting of this address. In this case, register is initialized to the default value.

When all power management bits are “0” in the 00H, 01H, 02H, 10H and 20H addresses and MCKO bit is “0”, all blocks are powered-down. The register values remain unchanged. Power supply current is $20\mu\text{A}$ (typ) in this case. For fully shut down (typ. $1\mu\text{A}$), the PDN pin should be “L”.

When neither ADC nor DAC are used, external clocks may not be present. When ADC or DAC is used, external clocks must always be present.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|-----|-------|-------|-------|-----|----|------|-------|
| 01H | Power Management 2 | HPZ | HPMTN | PMHPL | PMHPR | M/S | 0 | MCKO | PMPLL |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMPLL: PLL Power Management

0: EXT Mode and Power-Down (default)

1: PLL Mode and Power-up

MCKO: Master Clock Output Enable

0: Disable: MCKO pin = "L" (default)

1: Enable: Output frequency is selected by PS1-0 bits.

M/S: Master / Slave Mode Select

0: Slave Mode (default)

1: Master Mode

PMHPR: Headphone-Amp Rch Power Management

0: Power-down (default)

1: Power-up

PMHPL: Headphone-Amp Lch Power Management

0: Power-down (default)

1: Power-up

HPMTN: Headphone-Amp Mute Control

0: Mute (default)

1: Normal operation

HPZ: Headphone-Amp Pull-down Control

0: Shorted to GND (default)

1: Pulled-down by 200kΩ (typ)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------|----|----|----|-------|----|------|----|--------|
| 02H | Signal Select 1 | 0 | 0 | 0 | DAACL | 0 | PMMP | 0 | MGAIN0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

MGAIN1-0: MIC-Amp Gain Control ([Table 23](#))

MGAIN1 bit is D5 bit of 03H.

PMMP: MPWR pin Power Management

0: Power-down: Hi-Z (default)

1: Power-up

DAACL: Switch Control from DAC to Line Output

0: OFF (default)

1: ON

When PMLO bit is "1", DAACL bit is enabled. When PMLO bit is "0", the LOUT/ROUT pins go to VSS1.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------|------|------|--------|----|----|------|----|----|
| 03H | Signal Select 2 | LOVL | LOPS | MGAIN1 | 0 | 0 | MINL | 0 | 0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

MINL: Switch Control from MIN pin to Stereo Line Output

0: OFF (default)

1: ON

When PMLO bit is “1”, MINL bit is enabled. When PMLO bit is “0”, the LOUT/ROUT pins go to VSS1.

MGAIN1: MIC-Amp Gain Control ([Table 23](#))

LOPS: Stereo Line Output Power-Save Mode

0: Normal Operation (default)

1: Power-Save Mode

LOVL: Stereo Line Output Gain Select ([Table 51](#), [Table 52](#))

0: 0dB/+6dB (default)

1: +2dB/+8dB

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------|------|------|------|------|------|----|------|------|
| 04H | Mode Control 1 | PLL3 | PLL2 | PLL1 | PLL0 | BCKO | 0 | DIF1 | DIF0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

DIF1-0: Audio Interface Format ([Table 17](#))

Default: “10” (Left justified)

BCKO: BICK Output Frequency Select at Master Mode ([Table 11](#))

PLL3-0: PLL Reference Clock Select ([Table 5](#))

Default: “0000”(LRCK pin)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------|-----|-----|-----|------|------|-----|-----|-----|
| 05H | Mode Control 2 | PS1 | PS0 | FS3 | MSBS | BCKP | FS2 | FS1 | FS0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

FS3-0: Sampling Frequency Select ([Table 6](#) and [Table 7.](#)) and MCKI Frequency Select ([Table 12.](#))

FS3-0 bits select sampling frequency at PLL mode and MCKI frequency at EXT mode.

BCKP: BICK Polarity at DSP Mode ([Table 18](#))

“0”: SDTO is output by the rising edge (“↑”) of BICK and SDTI is latched by the falling edge (“↓”). (default)

“1”: SDTO is output by the falling edge (“↓”) of BICK and SDTI is latched by the rising edge (“↑”).

MSBS: LRCK Polarity at DSP Mode ([Table 18](#))

“0”: The rising edge (“↑”) of LRCK is half clock of BICK before the channel change. (default)

“1”: The rising edge (“↑”) of LRCK is one clock of BICK before the channel change.

PS1-0: MCKO Output Frequency Select ([Table 10](#))

Default: “00”(256fs)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|------|------|------|------|------|------|-------|-------|
| 06H | Timer Select | DVTM | WTM2 | ZTM1 | ZTM0 | WTM1 | WTM0 | RFST1 | RFST0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RFST1-0: ALC First recovery Speed ([Table 34](#))
 Default: "00"(4times)

WTM2-0: ALC Recovery Waiting Period ([Table 31.](#))
 Default: "000" (128/fs)

ZTM1-0: ALC Limiter/Recovery Operation Zero Crossing Timeout Period ([Table 30.](#))
 Default: "00" (128/fs)

DVTM: Digital Volume Transition Time Setting ([Table 40.](#))
 0: 1061/fs (default)
 1: 256/fs

This is the transition time between DVL/R7-0 bits = 00H and FFH.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|----|----|-----|-------|-------|-------|--------|-------|
| 07H | ALC Mode Control 1 | 0 | 0 | ALC | ZELMN | LMAT1 | LMAT0 | RGAIN0 | LMTH0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level ([Table 28.](#))
 Default: "00"
 LMTH1 bit is D6 bit of 0BH.

RGAIN1-0: ALC Recovery GAIN Step ([Table 32.](#))
 Default: "00"
 RGAIN1 bit is D7 bit of 0BH.

LMAT1-0: ALC Limiter ATT Step ([Table 29.](#))
 Default: "00"

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation
 0: Enable (default)
 1: Disable

ALC: ALC Enable
 0: ALC Disable (default)
 1: ALC Enable

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|------|------|------|------|------|------|------|------|
| 08H | ALC Mode Control 2 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| | Default | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

REF7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level ([Table 33.](#))
 Default: "E1H" (+30.0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|--------------------------|------|------|------|------|------|------|------|------|
| 09H | Lch Input Volume Control | IVL7 | IVL6 | IVL5 | IVL4 | IVL3 | IVL2 | IVL1 | IVL0 |
| 0CH | Rch Input Volume Control | IVR7 | IVR6 | IVR5 | IVR4 | IVR3 | IVR2 | IVR1 | IVR0 |
| Default | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

IVL7-0, IVR7-0: Input Digital Volume; 0.375dB step, 242 Level (Table 36.)
 Default: "E1H" (+30.0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|----------------------------|------|------|------|------|------|------|------|------|
| 0AH | Lch Digital Volume Control | DVL7 | DVL6 | DVL5 | DVL4 | DVL3 | DVL2 | DVL1 | DVL0 |
| 0DH | Rch Digital Volume Control | DVR7 | DVR6 | DVR5 | DVR4 | DVR3 | DVR2 | DVR1 | DVR0 |
| Default | | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

DVL7-0, DVR7-0: Output Digital Volume (Table 39.)
 Default: "18H" (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|--------------------|--------|-------|----|----|----|----|------|----|
| 0BH | ALC Mode Control 3 | RGAIN1 | LMTH1 | 0 | 0 | 0 | 0 | VBAT | 0 |
| Default | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

VBAT: HP-Amp Common Voltage (Table 56.)
 0: 0.5 x HVDD (default)
 1: 0.64 x AVDD

LMTH1: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 28.)

RGAIN1: ALC Recovery GAIN Step (Table 32.)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|----------------|----|------|-------|-------|------|------|------|------|
| 0EH | Mode Control 3 | 0 | LOOP | SMUTE | DVOLC | BST1 | BST0 | DEM1 | DEM0 |
| Default | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

DEM1-0: De-emphasis Frequency Select (Table 37)
 Default: "01" (OFF)

BST1-0: Bass Boost Function Select (Table 38)
 Default: "00" (OFF)

DVOLC: Output Digital Volume Control Mode Select

0: Independent

1: Dependent (default)

When DVOLC bit = "1", DVL7-0 bits control both Lch and Rch volume level, while register values of DVL7-0 bits are not written to DVR7-0 bits. When DVOLC bit = "0", DVL7-0 bits control Lch level and DVR7-0 bits control Rch level, respectively.

SMUTE: Soft Mute Control

0: Normal Operation (default)

1: DAC outputs soft-muted

LOOP: Digital Loopback Mode

0: SDTI → DAC (default)

1: SDTO → DAC

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------|----|----|----|----|-------|-----|------|------|
| 0FH | Mode Control 4 | 0 | 0 | 0 | 0 | IVOLC | HPM | MINH | DACH |
| | Default | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

DACH: Switch Control from DAC to Headphone-Amp

- 0: OFF (default)
- 1: ON

MINH: Switch Control from MIN pin to Headphone-Amp

- 0: OFF (default)
- 1: ON

HPM: Headphone-Amp Mono Output Select

- 0: Stereo (default)
- 1: Mono

When the HPM bit = "1", DAC output signal is output to Lch and Rch of the Headphone-Amp as (L+R)/2.

IVOLC: Input Digital Volume Control Mode Select

- 0: Independent
- 1: Dependent (default)

When IVOLC bit = "1", IVL7-0 bits control both Lch and Rch volume level, while register values of IVL7-0 bits are not written to IVR7-0 bits. When IVOLC bit = "0", IVL7-0 bits control Lch level and IVR7-0 bits control Rch level, respectively.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|------|------|-----|-------|-------|------|------|-------|
| 10H | Power Management 3 | INR1 | INL1 | HPG | MDIF2 | MDIF1 | INR0 | INL0 | PMADR |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMADR: MIC-Amp Lch and ADC Rch Power Management

- 0: Power-down (default)
- 1: Power-up

INL1-0: ADC Lch Input Source Select ([Table 20](#))

Default: 00 (LIN1 pin)

INR1-0: ADC Rch Input Source Select ([Table 20](#))

Default: 00 (RIN1 pin)

MDIF1: Single-ended / Full-differential Input Select 1

- 0: Single-ended input (LIN1/RIN1 pins: Default)
 - 1: Full-differential input (IN1+/IN1- pins)
- MDIF1 bit selects the input type of pins #32 and #31.

MDIF2: Single-ended / Full-differential Input Select 2

- 0: Single-ended input (LIN2/RIN2 pins: Default)
 - 1: Full-differential input (IN2+/IN2- pins)
- MDIF2 bit selects the input type of pins #30 and #29.

HPG: Headphone-Amp Gain Select ([Table 54.](#))

- 0: 0dB (default)
- 1: +3.6dB

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------------|-----|-----|----|------|----|------|----|----|
| 11H | Digital Filter Select | GN1 | GN0 | 0 | FIL1 | EQ | FIL3 | 0 | 0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

GN1-0: Gain Select at GAIN block (Table 26.)

Default: "00"

FIL3: FIL3 (Stereo Separation Emphasis Filter) Coefficient Setting Enable

0: Disable (default)

1: Enable

When FIL3 bit is "1", the settings of F3A13-0 and F3B13-0 bits are enabled. When FIL3 bit is "0", FIL3 block is OFF (MUTE).

EQ: EQ (Gain Compensation Filter) Coefficient Setting Enable

0: Disable (default)

1: Enable

When EQ bit is "1", the settings of EQA15-0, EQB13-0 and EQC15-0 bits are enabled. When EQ bit is "0", EQ block is through (0dB).

FIL1: FIL1 (Wind-noise Reduction Filter) Coefficient Setting Enable

0: Disable (default)

1: Enable

When FIL1 bit is "1", the settings of F1A13-0 and F1B13-0 bits are enabled. When FIL1 bit is "0", FIL1 block is through (0dB).

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------------|-------|-------|-------|-------|-------|-------|------|------|
| 12H | FIL3 Co-efficient 0 | F3A7 | F3A6 | F3A5 | F3A4 | F3A3 | F3A2 | F3A1 | F3A0 |
| 13H | FIL3 Co-efficient 1 | F3AS | 0 | F3A13 | F3A12 | F3A11 | F3A10 | F3A9 | F3A8 |
| 14H | FIL3 Co-efficient 2 | F3B7 | F3B6 | F3B5 | F3B4 | F3B3 | F3B2 | F3B1 | F3B0 |
| 15H | FIL3 Co-efficient 3 | 0 | 0 | F3B13 | F3B12 | F3B11 | F3B10 | F3B9 | F3B8 |
| 16H | EQ Co-efficient 0 | EQA7 | EQA6 | EQA5 | EQA4 | EQA3 | EQA2 | EQA1 | EQA0 |
| 17H | EQ Co-efficient 1 | EQA15 | EQA14 | EQA13 | EQA12 | EQA11 | EQA10 | EQA9 | EQA8 |
| 18H | EQ Co-efficient 2 | EQB7 | EQB6 | EQB5 | EQB4 | EQB3 | EQB2 | EQB1 | EQB0 |
| 19H | EQ Co-efficient 3 | 0 | 0 | EQB13 | EQB12 | EQB11 | EQB10 | EQB9 | EQB8 |
| 1AH | EQ Co-efficient 4 | EQC7 | EQC6 | EQC5 | EQC4 | EQC3 | EQC2 | EQC1 | EQC0 |
| 1BH | EQ Co-efficient 5 | EQC15 | EQC14 | EQC13 | EQC12 | EQC11 | EQC10 | EQC9 | EQC8 |
| 1CH | FIL1 Co-efficient 0 | F1A7 | F1A6 | F1A5 | F1A4 | F1A3 | F1A2 | F1A1 | F1A0 |
| 1DH | FIL1 Co-efficient 1 | F1AS | 0 | F1A13 | F1A12 | F1A11 | F1A10 | F1A9 | F1A8 |
| 1EH | FIL1 Co-efficient 2 | F1B7 | F1B6 | F1B5 | F1B4 | F1B3 | F1B2 | F1B1 | F1B0 |
| 1FH | FIL1 Co-efficient 3 | 0 | 0 | F1B13 | F1B12 | F1B11 | F1B10 | F1B9 | F1B8 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

F3A13-0, F3B13-0: FIL3 (Stereo Separation Emphasis Filter) Coefficient (14bit x 2)

Default: "0000H"

F3AS: FIL3 (Stereo Separation Emphasis Filter) Select

0: HPF (default)

1: LPF

EQA15-0, EQB13-0, EQC15-0: EQ (Gain Compensation Filter) Coefficient (14bit x 2 + 16bit x 1)

Default: "0000H"

F1A13-0, F1B13-0: FIL1 (Wind-noise Reduction Filter) Coefficient (14bit x 2)

Default: "0000H"

F1AS: FIL1 (Wind-noise Reduction Filter) Select

0: HPF (default)

1: LPF

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|--------------------|---------|---------|---------|---------|---------|---------|--------|--------|
| 20H | Power Management 4 | PMAINR4 | PMAINL4 | PMAINR3 | PMAINL3 | PMAINR2 | PMAINL2 | PMMICR | PMMICL |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMMICL: MIC-Amp Lch Power Management

0: Power down (default)

1: Power up

PMMICR: MIC-Amp Rch Power Management

0: Power down (default)

1: Power up

PMAINL2: LIN2 Mixing Circuit Power Management

0: Power down (default)

1: Power up

PMAINR2: RIN2 Mixing Circuit Power Management

0: Power down (default)

1: Power up

PMAINL3: LIN3 Mixing Circuit Power Management

0: Power down (default)

1: Power up

PMAINR3: RIN3 Mixing Circuit Power Management

0: Power down (default)

1: Power up

PMAINL4: LIN4 Mixing Circuit Power Management

0: Power down (default)

1: Power up

PMAINR4: RIN4 Mixing Circuit Power Management

0: Power down (default)

1: Power up

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------|----|----|-------|-------|-------|-----|------|-------|
| 21H | Mode Control 5 | 0 | 0 | MICR3 | MICL3 | L4DIF | MIX | AIN3 | LODIF |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LODIF: Lineout Select

- 0: Single-ended Stereo Line Output (LOUT/ROUT pins) (default)
- 1: Full-differential Mono Line Output (LOP/LON pins)

AIN3: Analog Mixing Select

- 0: Mono Input (MIN pin) (default)
- 1: Stereo Input (LIN3/RIN3 pins): PLL is not available.

MIX: Mono Recording

- 0: Stereo (default)
- 1: Mono: (L+R)/2

L4DIF: Line Input Type Select

- 0: Stereo Single-ended Input: LIN4/RIN4 pins (default)
- 1: Mono Full-differential Input: IN4+/- pins

MICL3: Switch Control from MIC-Amp Lch to Analog Output

- 0: LIN3 input signal is selected. (default)
- 1: MIC-Amp Lch output signal is selected.

MICR3: Switch Control from MIC-Amp Rch to Analog Output

- 0: RIN3 input signal is selected. (default)
- 1: MIC-Amp Rch output signal is selected.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|-----------------------|-----|------|-------|-------|-------|-------|-------|-------|
| 22H | Lineout Mixing Select | LOM | LOM3 | RINR4 | LINL4 | RINR3 | LINL3 | RINR2 | LINL2 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LINL2: Switch Control from LIN2 pin to Stereo Line Output (without MIC-Amp)

0: OFF (default)

1: ON

RINR2: Switch Control from RIN2 pin to Stereo Line Output (without MIC-Amp)

0: OFF (default)

1: ON

LINL3: Switch Control from LIN3 pin (or MIC-Amp Lch) to Stereo Line Output

0: OFF (default)

1: ON

RINR3: Switch Control from RIN3 pin (or MIC-Amp Lch) to Stereo Line Output

0: OFF (default)

1: ON

LINL4: Switch Control from LIN4 pin to Stereo Line Output (without MIC-Amp)

0: OFF (default)

1: ON

RINR4: Switch Control from RIN4 pin to Stereo Line Output (without MIC-Amp)

0: OFF (default)

1: ON

LOM3: Mono Mixing from MIC-Amp (or LIN3/RIN3) to Stereo Line Output

0: Stereo Mixing (default)

1: Mono Mixing

LOM: Mono Mixing from DAC to Stereo Line Output

0: Stereo Mixing (default)

1: Mono Mixing

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------------|----|------|-------|-------|-------|-------|-------|-------|
| 23H | HP Mixing Select | 0 | HPM3 | RINH4 | LINH4 | RINH3 | LINH3 | RINH2 | LINH2 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LINH2: Switch Control from LIN2 pin to Headphone Output (without MIC-Amp)

0: OFF (default)

1: ON

RINH2: Switch Control from RIN2 pin to Headphone Output (without MIC-Amp)

0: OFF (default)

1: ON

LINH3: Switch Control from LIN3 pin (or MIC-Amp Lch) to Headphone Output

0: OFF (default)

1: ON

RINH3: Switch Control from RIN3 pin (or MIC-Amp Lch) to Headphone Output

0: OFF (default)

1: ON

LINH4: Switch Control from LIN4 pin to Headphone Output (without MIC-Amp)

0: OFF (default)

1: ON

RINH4: Switch Control from RIN4 pin to Headphone Output (without MIC-Amp)

0: OFF (default)

1: ON

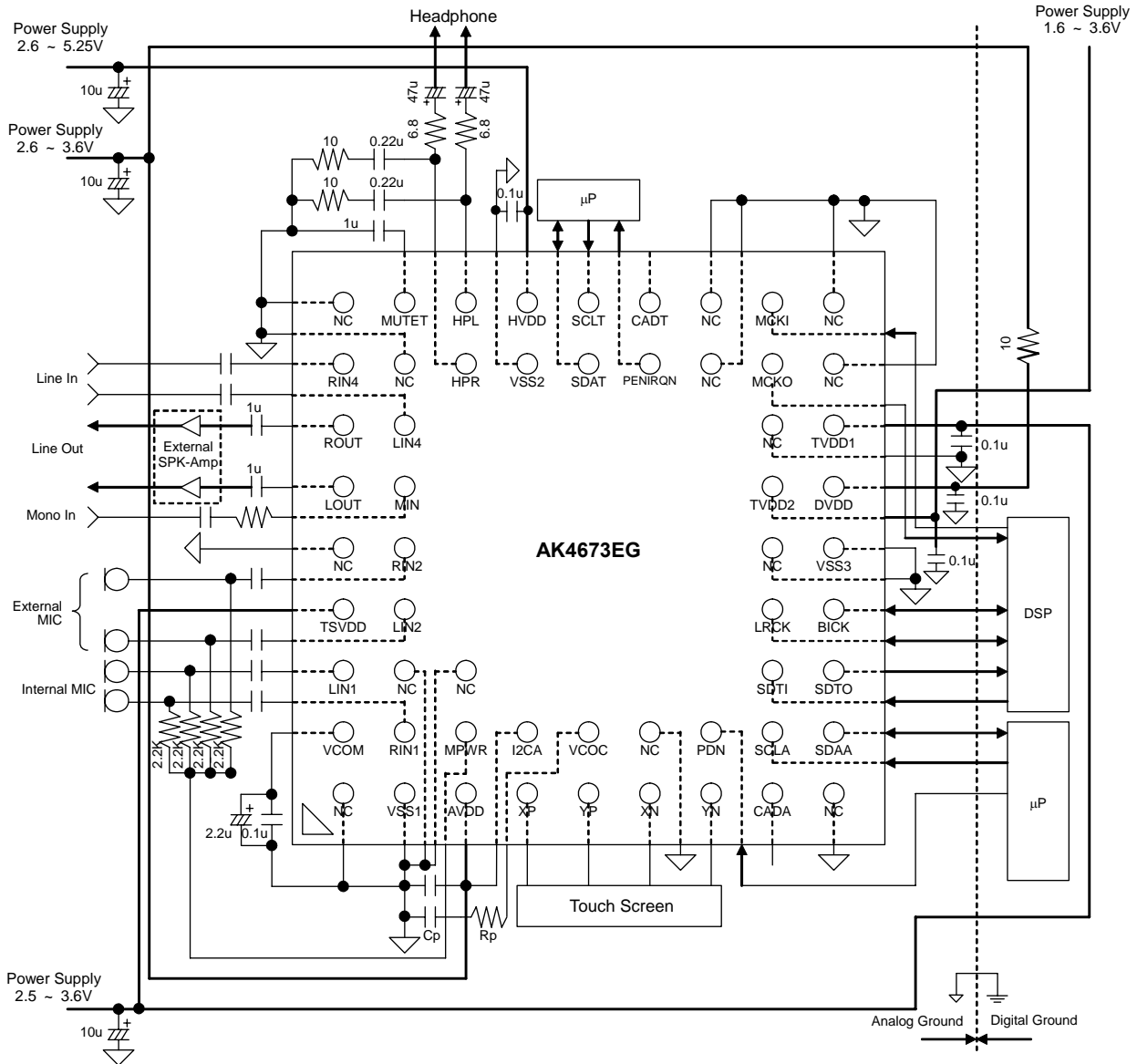
HPM3: Mono Mixing from MIC-Amp (or LIN3/RIN3) to Headphone Output

0: Stereo Mixing (default)

1: Mono Mixing

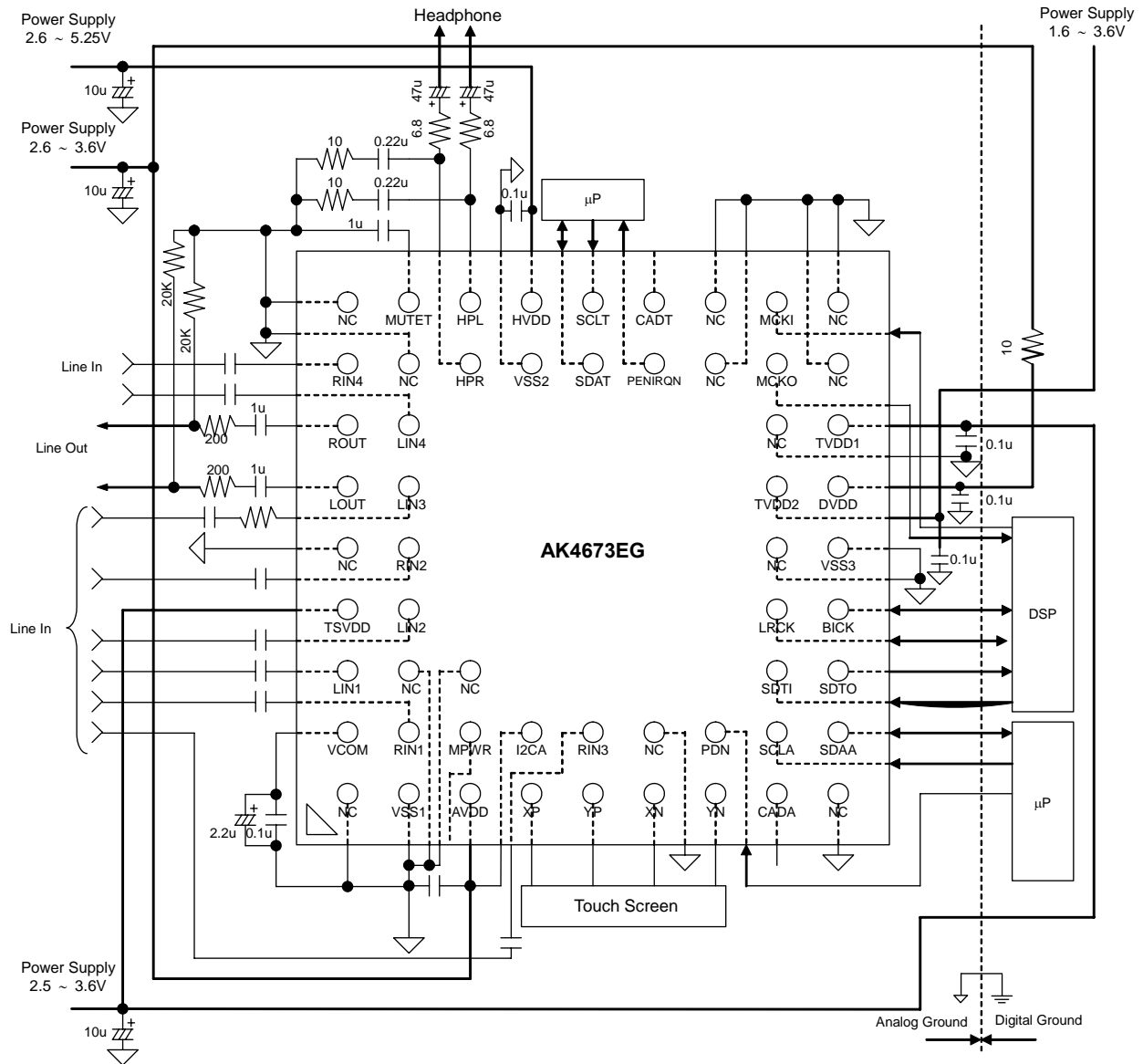
SYSTEM DESIGN

Figure 83 and Figure 84 shows the system connection diagram for the AK4673. The evaluation board [AKD4673] is demonstrates the optimum layout, power supply arrangements and measurement results.


Notes:

- VSS1, VSS2 and VSS3 pins of the AK4673 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When the AK4673 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of the VCOC/RIN3 pin is not needed.
- When the AK4673 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of the VCOC/RIN3 pin should be connected as shown in Table 5.
- When the AK4673 is used as master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, 100kΩ around pull-up resistor should be connected to LRCK and BICK pins of the AK4673.
- 0.1μF ceramic capacitor should be attached to each supply pins. The type of other capacitors is not critical.
- When DVDD is supplied from AVDD via 10Ω series resistor, the capacitor larger than 0.1μF should not be connected between DVDD and the ground.

Figure 83. Typical Connection Diagram (AIN3 bit = "0", MIC Input)


Notes:

- VSS1, VSS2 and VSS3 pins of the AK4673 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When AIN3 bit = "1", PLL is not available.
- When the AK4673 is used at master mode, LRCK and BICK pins are floating before M/S bit is changed to "1". Therefore, 100kΩ around pull-up resistor should be connected to LRCK and BICK pins of the AK4673.
- 0.1µF ceramic capacitor should be attached to each supply pins. The type of other capacitors is not critical.
- When DVDD is supplied from AVDD via 10Ω series resistor, a capacitor larger than 0.1µF should not be connected between DVDD and the ground.

Figure 84. Typical Connection Diagram (AIN3 bit = "1": PLL is not available, Line Input)

1. Grounding and Power Supply Decoupling

The AK4673 requires careful attention to power supply and grounding arrangements. AVDD, DVDD, TVDD1, TVDD2, HVDD and TSVDD are usually supplied from the system's analog supply. If AVDD, DVDD, TVDD1, TVDD2, HVDD and TSVDD are supplied separately, the power-up sequence is not critical. The PDN pin should be held to "L" upon power-up. The PDN pin should be set to "H" after all power supplies are powered-up. In case that the pop noise should be avoided at line output and headphone output, the AK4673 should be operated by the following recommended power-up/down sequence.

1) Power-up

- The PDN pin should be held to "L" upon power-up. The AK4673 should be reset by bringing the PDN pin "L" for 150ns or more.
- In case that the power supplies are separated in two or more groups, the power supply including TVDD1 and TVDD2 should be powered ON at first. Regarding the relationship between DVDD and HVDD, the power supply including DVDD should be powered ON prior to the power supply including HVDD.

2) Power-down

- Each power supplies should be powered OFF after the PDN pin is set to "L".
- In case that the power supplies are separated in two or more groups, the power supply including TVDD1 and TVDD2 should be powered OFF at last. Regarding the relationship between DVDD and HVDD, the power supply including HVDD should be powered OFF prior to the power supply including DVDD.

VSS1, VSS2 and VSS3 of the AK4673 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4673 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2 μ F electrolytic capacitor in parallel with a 0.1 μ F ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4673.

3. Analog Inputs

The Mic, Line and MIN inputs are single-ended. The input signal range scales with nominally at 0.06 x AVDD Vpp(typ) @MGAIN1-0 bits = "01", 0.03 x AVDD Vpp(typ) @MGAIN1-0 bits = "10", 0.015 x AVDD Vpp(typ) @MGAIN1-0 bits = "11" or 0.6 x AVDD Vpp(typ) @MGAIN1-0 bits = "00" for the Mic/Line input and 0.6 x AVDD Vpp (typ) for the MIN input, centered around the internal common voltage (0.45 x AVDD). Usually the input signal is AC coupled using a capacitor. The cut-off frequency is $f_c = 1 / (2\pi RC)$. The AK4673 can accept input voltages from VSS1 to AVDD.

4. Analog Outputs

The input data format for the DAC is 2's complement. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal output is VCOM voltage for 0000H(@16bit). Stereo Line Output is centered at 0.45 x AVDD. The Headphone-Amp output is centered at HVDD/2.

CONTROL SEQUENCE

■ Clock Set up

When ADC or DAC is powered-up, the clocks must be supplied.

1. PLL Master Mode.

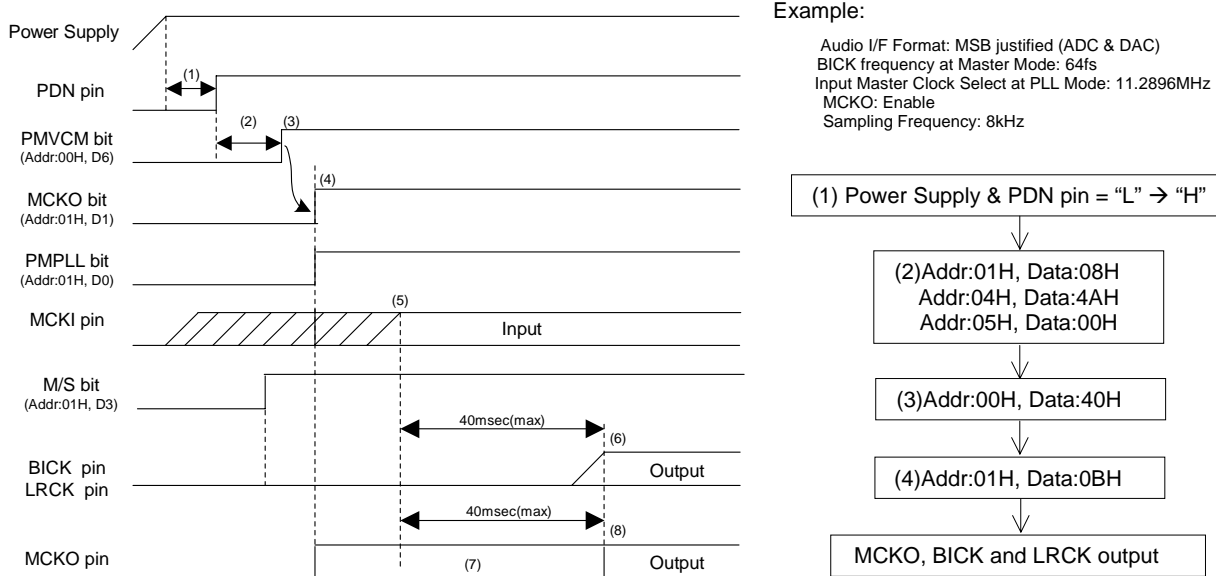


Figure 85. Clock Set Up Sequence (1)

<Example>

- (1) After Power Up, the PDN pin = "L" → "H". "L" time of 150ns or more is needed to reset the AK4673. The AK4673 should be operated by the recommended power-up/down sequence shown in "System Design (Grounding and Power Supply Decoupling)" to avoid the pop noise at line output and headphone output.
- (2) DIF1-0, PLL3-0, FS3-0, BCKO and M/S bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
 VCOM should first be powered-up before the other block operates.
- (4) In case of using MCKO output: MCKO bit = "1"
 In case of not using MCKO output: MCKO bit = "0"
- (5) PLL lock time is 40ms(max) after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source.
- (6) The AK4673 starts to output the LRCK and BICK clocks after the PLL becomes stable. Then normal operation starts.
- (7) The invalid frequency is output from MCKO pin during this period if MCKO bit = "1".
- (8) The normal clock is output from MCKO pin after the PLL is locked if MCKO bit = "1".

2. PLL Slave Mode (LRCK or BICK pin)

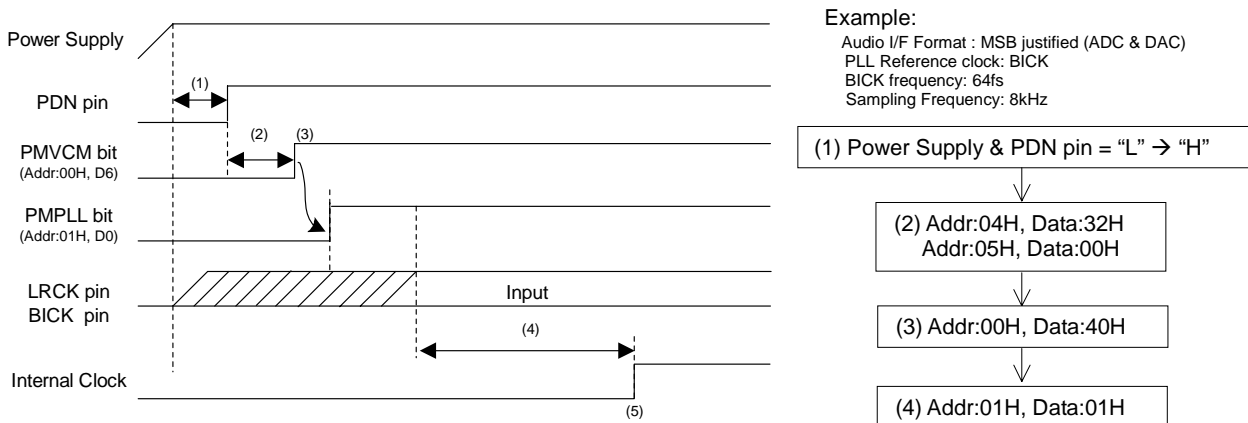


Figure 86. Clock Set Up Sequence (2)

<Example>

- (1) After Power Up: The PDN pin "L" → "H". "L" time of 150ns or more is needed to reset the AK4673. The AK4673 should be operated by the recommended power-up/down sequence shown in "System Design (Grounding and Power Supply Decoupling)" to avoid pop noise at line output and headphone output.
- (2) DIF1-0, FS3-0 and PLL3-0 bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
 VCOM should first be powered up before the other block operates.
- (4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (LRCK or BICK pin) is supplied. PLL lock time is 160ms(max) when LRCK is a PLL reference clock. And PLL lock time is 2ms(max) when BICK is a PLL reference clock.
- (5) Normal operation starts after that the PLL is locked.

3. PLL Slave Mode (MCKI pin)

Example:

Audio I/F Format: MSB justified (ADC & DAC)
 BICK frequency at Master Mode: 64fs
 Input Master Clock Select at PLL Mode: 11.2896MHz
 MCKO: Enable
 Sampling Frequency: 8kHz

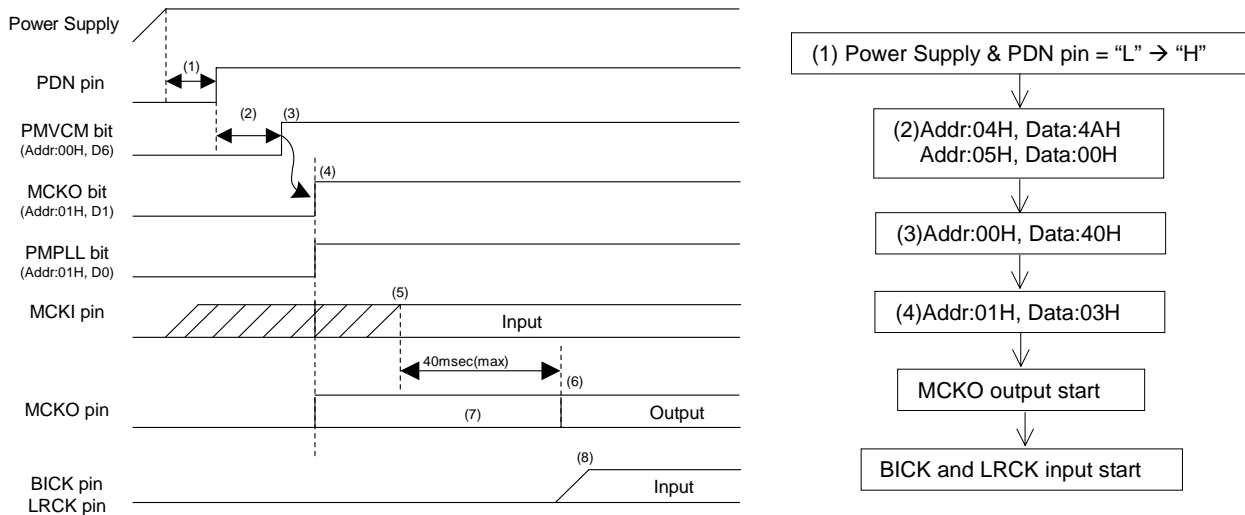


Figure 87. Clock Set Up Sequence (3)

<Example>

- (1) After Power Up: The PDN pin "L" → "H". "L" time of 150ns or more is needed to reset the AK4673. The AK4673 should be operated by the recommended power-up/down sequence shown in "System Design (Grounding and Power Supply Decoupling)" to avoid pop noise at line output and headphone output.
- (2) DIF1-0, PLL3-0 and FS3-0 bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.
- (4) Enable MCKO output: MCKO bit = "1"
- (5) PLL starts after that the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied. PLL lock time is 40ms(max).
- (6) The invalid frequency is output from MCKO during this period.
- (7) The normal clock is output from MCKO after PLL is locked.
- (8) BICK and LRCK clocks should be synchronized with MCKO clock.

4. EXT Slave Mode

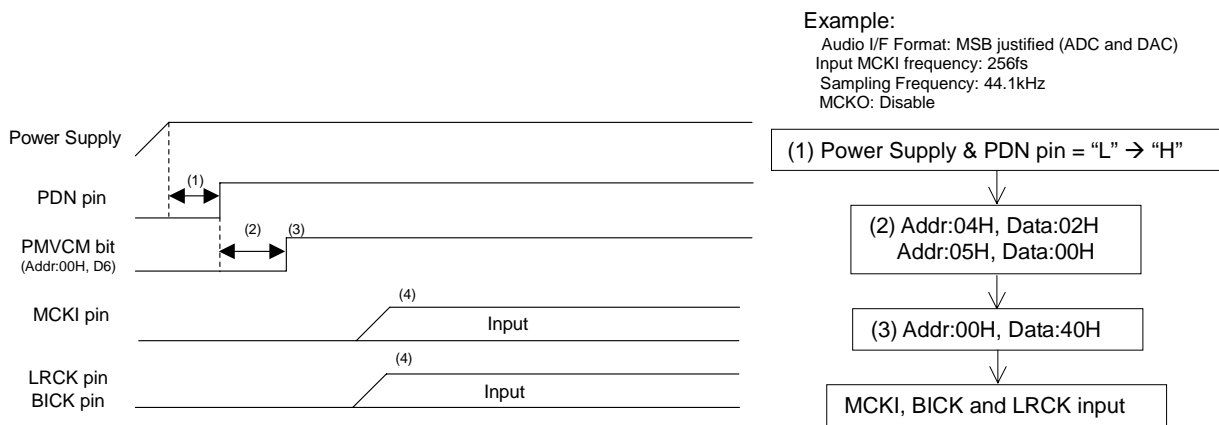


Figure 88. Clock Set Up Sequence (4)

<Example>

- (1) After Power Up: The PDN pin "L" → "H". "L" time of 150ns or more is needed to reset the AK4673.
 The AK4673 should be operated by the recommended power-up/down sequence shown in "System Design (Grounding and Power Supply Decoupling)" to avoid pop noise at line output and headphone output.
- (2) DIF1-0 and FS1-0 bits should be set during this period.
- (3) Power Up VCOM: PMVCM bit = "0" → "1"
 VCOM should first be powered up before the other block operates.
- (4) Normal operation starts after the MCKI, LRCK and BICK are supplied.

5. EXT Master Mode

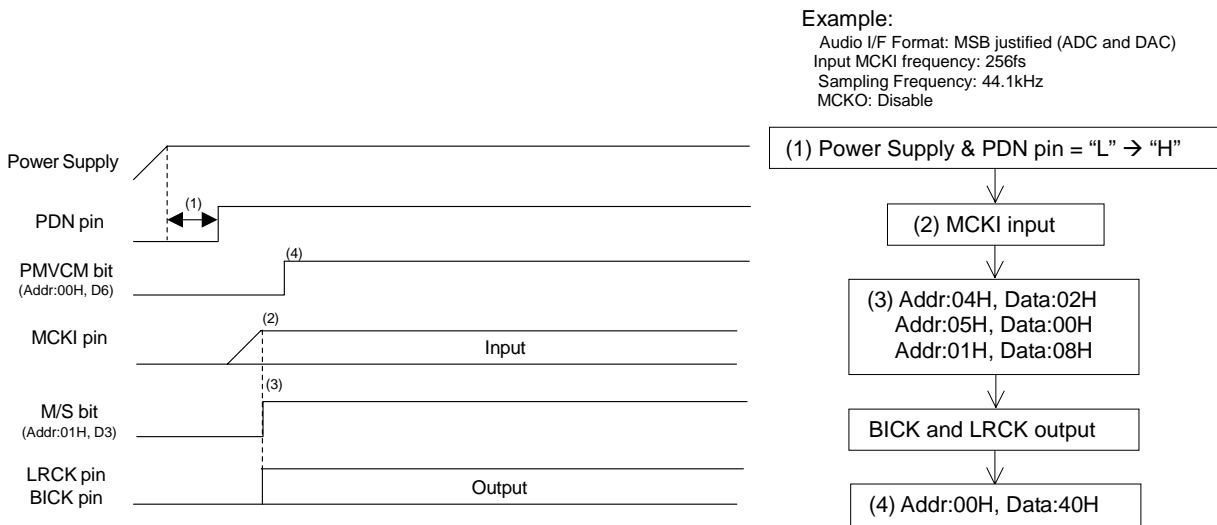


Figure 89. Clock Set Up Sequence (5)

<Example>

- (1) After Power Up: The PDN pin "L" → "H". "L" time of 150ns or more is needed to reset the AK4673.
 The AK4673 should be operated by the recommended power-up/down sequence shown in "System Design (Grounding and Power Supply Decoupling)" to avoid pop noise at line output and headphone output.
- (2) MCKI should be input.
- (3) After DIF1-0 and FS1-0 bits are set, M/S bit should be set to "1". Then LRCK and BICK are output.
- (4) Power Up VCOM: PMVCM bit = "0" → "1"
 VCOM should first be powered up before the other block operates.

■ MIC Input Recording (Stereo)

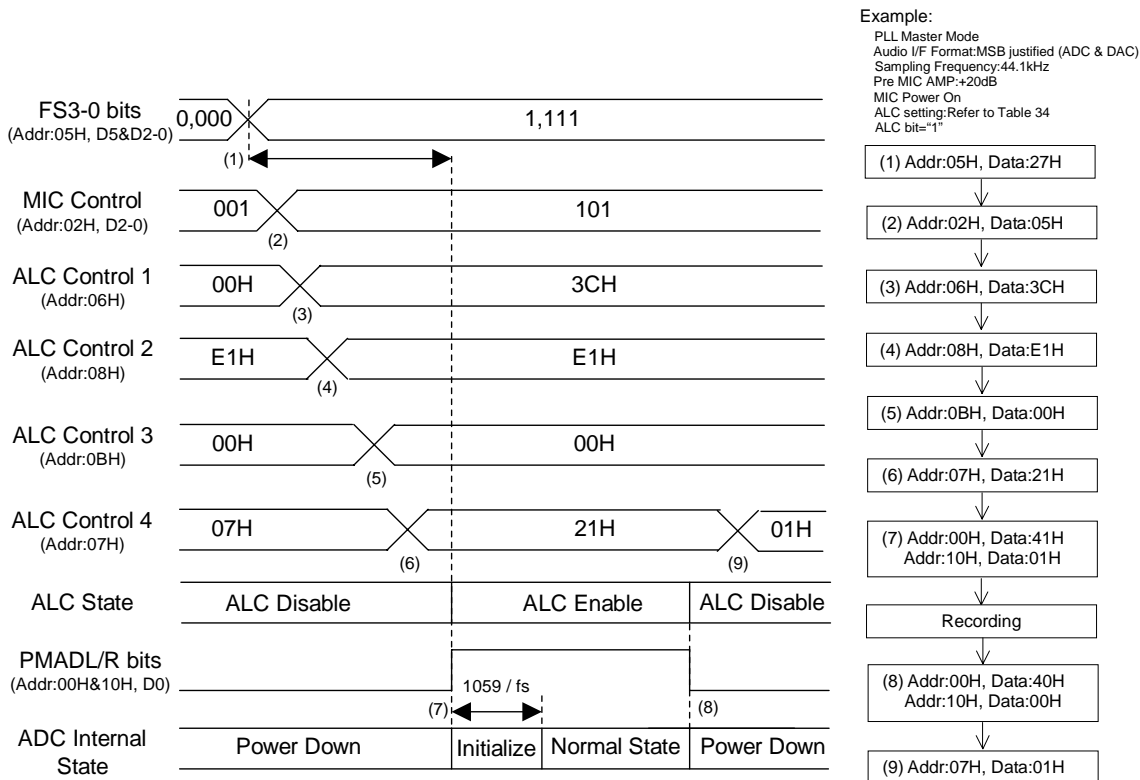


Figure 90. MIC Input Recording Sequence

<Example>

This sequence is an example of ALC setting at $f_s=44.1\text{kHz}$. If the parameter of the ALC is changed, please refer to “[Figure 35. Registers set-up sequence at ALC operation](#)”

At first, clocks should be supplied according to “Clock Set Up” sequence.

- (1) Set up a sampling frequency (FS3-0 bit). When the AK4673 is PLL mode, MIC and ADC should be powered-up in consideration of PLL lock time after a sampling frequency is changed.
- (2) Set up MIC input (Addr: 02H)
- (3) Set up Timer Select for ALC (Addr: 06H)
- (4) Set up REF value for ALC (Addr: 08H)
- (5) Set up LMTH1 and RGAIN1 bits (Addr: 0BH)
- (6) Set up LMTH0, RGAIN0, LMAT1-0 and ALC bits (Addr: 07H)
- (7) Power Up MIC and ADC: PMADL = PMADR bits = “0” → “1”

The initialization cycle time of ADC is $1059/f_s=24\text{ms}@f_s=44.1\text{kHz}$.

After the ALC bit is set to “1” and MIC&ADC block is powered-up, the ALC operation starts from IVOL default value (+30dB).

The time of offset voltage going to “0” after the ADC initialization cycle depends on both the time of analog input pin going to the common voltage and the time constant of the offset cancel digital HPF. This time can be shorter by using the following sequence:

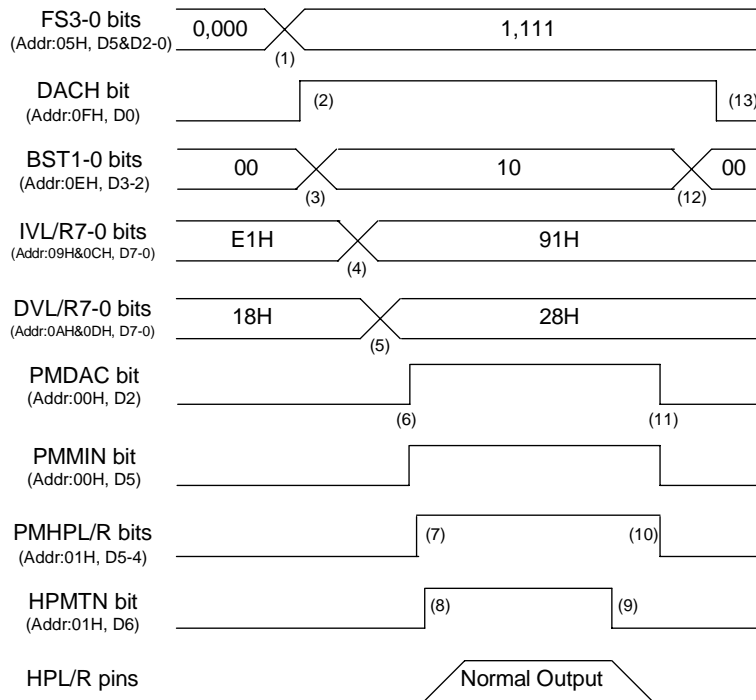
At first, PMVCM and PMMP bits should set to “1”. Then, the ADC should be powered-up. The wait time to power-up the ADC should be longer than 4 times of the time constant that is determined by the AC coupling capacitor at analog input pin and the internal input resistance 60k(typ).

- (8) Power Down MIC and ADC: PMADL = PMADR bits = “1” → “0”

When the registers for the ALC operation are not changed, ALC bit may be keeping “1”. The ALC operation is disabled because the MIC&ADC block is powered-down. If the registers for the ALC operation are also changed when the sampling frequency is changed, it should be done after the AK4673 goes to the manual mode (ALC bit = “0”) or MIC&ADC block is powered-down (PMADL=PMADR bits = “0”). IVOL gain is not reset when PMADL=PMADR bits = “0”, and then IVOL operation starts from the setting value when PMADL or PMADR bit is changed to “1”.

- (9) ALC Disable: ALC bit = “1” → “0”

Headphone-amp Output



Example :

PLL Master Mode
 Sampling Frequency: 44.1kHz
 DVOLC bit = "1"(default)
 Digital Volume Level: -8dB
 Bass Boost Level: Middle
 De-emphases response: OFF
 Soft Mute Time: 256/fs

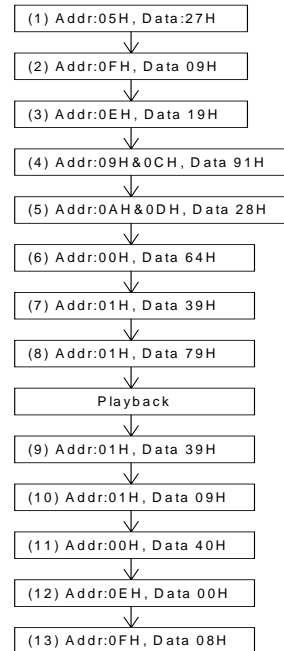


Figure 91. Headphone-Amp Output Sequence

<Example>

At first, clocks should be supplied according to "Clock Set Up" sequence.

- (1) Set up a sampling frequency (FS3-0 bits). When the AK4673 is PLL mode, DAC and Headphone-Amp should be powered-up in consideration of PLL lock time after a sampling frequency is changed.
- (2) Set up the path of "DAC → HP-Amp": DACH bit = "0" → "1"
- (3) Set up the low frequency boost level (BST1-0 bits)
- (4) Set up the input digital volume (Addr: 09H and 0CH)
 When PMADL = PMADR bits = "0", IVL7-0 and IVR7-0 bits should be set to "91H"(0dB).
- (5) Set up the output digital volume (Addr: 0AH and 0DH)
 When DVOLC bit is "1" (default), DVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.
- (6) Power up DAC and MIN-Amp: PMDAC = PMMIN bits = "0" → "1"
 The DAC enters an initialization cycle that starts when the PMDAC bit is changed from "0" to "1" at PMADL and PMADR bits are "0". The initialization cycle time is $1059/fs=24ms@fs=44.1kHz$. During the initialization cycle, the DAC input digital data of both channels are internally forced to a 2's compliment, "0". The DAC output reflects the digital input data after the initialization cycle is complete. When PMADL or PMADR bit is "1", the DAC does not require an initialization cycle. When ALC bit is "1", ALC is disable (ALC gain is set by IVL/R7-0 bits) during an initialization cycle ($1059/fs=24ms@fs=44.1kHz$). After the initialization cycle, ALC operation starts from the gain set by IVL/R7-0 bits.
- (7) Power up headphone-amp: PMHPL = PMHPR bits = "0" → "1"
 Output voltage of headphone-amp is still VSS2.
- (8) Rise up the common voltage of headphone-amp: HPMTN bit = "0" → "1"
 The rise time depends on HVDD and the capacitor value connected with the MUTET pin. When HVDD=3.3V and the capacitor value is 1.0μF, the time constant is $\tau_r = 100ms(\text{typ}), 250ms(\text{max})$.
- (9) Fall down the common voltage of headphone-amp: HPMTN bit = "1" → "0"
 The fall time depends on HVDD and the capacitor value connected with the MUTET pin. When HVDD=3.3V and the capacitor value is 1.0μF, the time constant is $\tau_f = 100ms(\text{typ}), 250ms(\text{max})$.
 If the power supply is powered-off or headphone-Amp is powered-down before the common voltage goes to GND, the pop noise occurs. It takes twice of τ_f that the common voltage goes to GND.
- (10) Power down headphone-amp: PMHPL = PMHPR bits = "1" → "0"
- (11) Power down DAC and MIN-Amp: PMDAC = PMMIN bits = "1" → "0"
- (12) Off the bass boost: BST1-0 bits = "00"
- (13) Disable the path of "DAC → HP-Amp": DACH bit = "1" → "0"

■ Stereo Line Output

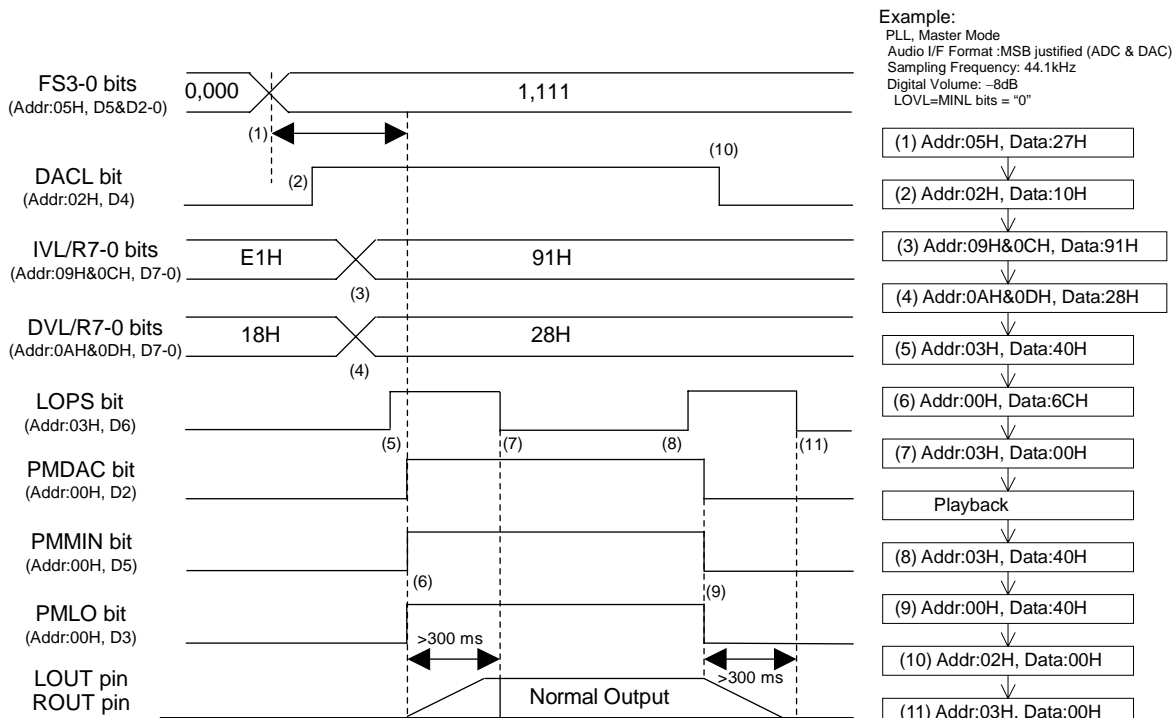


Figure 92. Stereo Lineout Sequence

<Example>

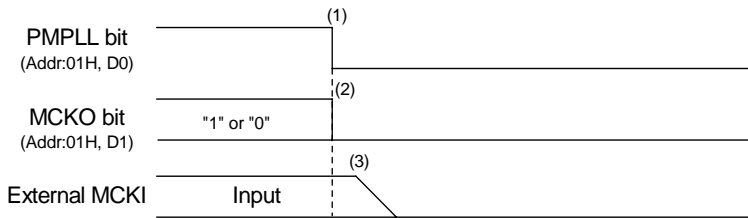
At first, clocks should be supplied according to “Clock Set Up” sequence.

- (1) Set up the sampling frequency (FS3-0 bits). When the AK4673 is PLL mode, DAC and Stereo Line-Amp should be powered-up in consideration of PLL lock time after the sampling frequency is changed.
- (2) Set up the path of “DAC → Stereo Line Amp”: DACL bit = “0” → “1”
- (3) Set up the input digital volume (Addr: 09H and 0CH)
When PMADL = PMADR bits = “0”, IVL7-0 and IVR7-0 bits should be set to “91H”(0dB).
- (4) Set up the output digital volume (Addr: 0AH and 0DH)
When DVOLC bit is “1” (default), DVL7-0 bits set the volume of both channels. After DAC is powered-up, the digital volume changes from default value (0dB) to the register setting value by the soft transition.
- (5) Enter power-save mode of Stereo Line Amp: LOPS bit = “0” → “1”
- (6) Power-up DAC, MIN-Amp and Stereo Line-Amp: PMDAC = PMMIN = PMLO bits = “0” → “1”
The DAC enters an initialization cycle that starts when the PMDAC bit is changed from “0” to “1” at PMADL and PMADR bits are “0”. The initialization cycle time is $1059/fs=24ms@fs=44.1kHz$. During the initialization cycle, the DAC input digital data of both channels are internally forced to a 2's complement, “0”. The DAC output reflects the digital input data after the initialization cycle is complete. When PMADL or PMADR bit is “1”, the DAC does not require an initialization cycle. When ALC bit is “1”, ALC is disable (ALC gain is set by IVL/R7-0 bits) during an initialization cycle ($1059/fs=24ms@fs=44.1kHz$). After the initialization cycle, ALC operation starts from the gain set by IVL/R7-0 bits.
LOUT and ROUT pins rise up to VCOM voltage after PMLO bit is changed to “1”. Rise time is 300ms(max) at $C=1\mu F$ and $AVDD=3.3V$.
- (7) Exit power-save mode of Stereo Line-Amp: LOPS bit = “1” → “0”
LOPS bit should be set to “0” after LOUT and ROUT pins rise up. Stereo Line-Amp goes to normal operation by setting LOPS bit to “0”.
- (8) Enter power-save mode of Stereo Line-Amp: LOPS bit: “0” → “1”
- (9) Power-down DAC, MIN-Amp and Stereo Line-Amp: PMDAC = PMMIN = PMLO bits = “1” → “0”
LOUT and ROUT pins fall down to VSS1. Fall time is 300ms(max) at $C=1\mu F$ and $AVDD=3.3V$.
- (10) Disable the path of “DAC → Stereo Line-Amp”: DACL bit = “1” → “0”
- (11) Exit power-save mode of Stereo Line-Amp: LOPS bit = “1” → “0”
LOPS bit should be set to “0” after LOUT and ROUT pins fall down.

■ Stop of Clock

Master clock can be stopped when ADC and DAC are not used.

1. PLL Master Mode



Example:

Audio I/F Format: MSB justified (ADC & DAC)
 BICK frequency at Master Mode: 64fs
 Input Master Clock Select at PLL Mode: 11.2896MHz
 Sampling Frequency: 8kHz

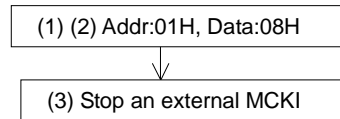
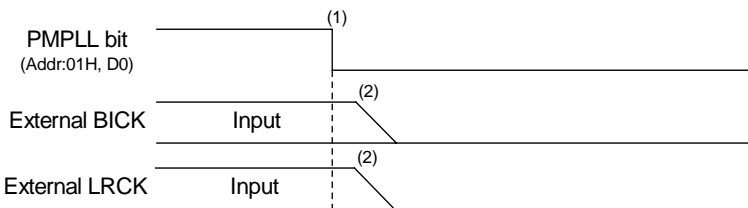


Figure 93. Clock Stopping Sequence (1)

<Example>

- (1) Power down PLL: PMPLL bit = "1" → "0"
- (2) Stop MCKO clock: MCKO bit = "1" → "0"
- (3) Stop an external master clock.

2. PLL Slave Mode (LRCK or BICK pin)



Example

Audio I/F Format : MSB justified (ADC & DAC)
 PLL Reference clock: BICK
 BICK frequency: 64fs
 Sampling Frequency: 8kHz

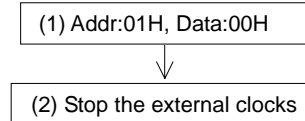
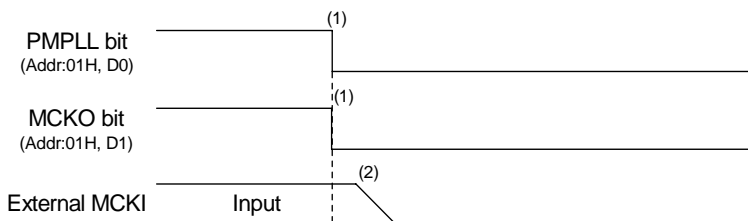


Figure 94. Clock Stopping Sequence (2)

<Example>

- (1) Power down PLL: PMPLL bit = "1" → "0"
- (2) Stop the external BICK and LRCK clocks

3. PLL Slave (MCKI pin)



Example

Audio I/F Format: MSB justified (ADC & DAC)
 PLL Reference clock: MCKI
 BICK frequency: 64fs
 Sampling Frequency: 8kHz

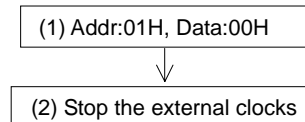


Figure 95. Clock Stopping Sequence (3)

<Example>

- (1) Power down PLL: PMPLL bit = "1" → "0"
- (2) Stop MCKO output: MCKO bit = "1" → "0"
- (3) Stop the external master clock.

4. EXT Slave Mode

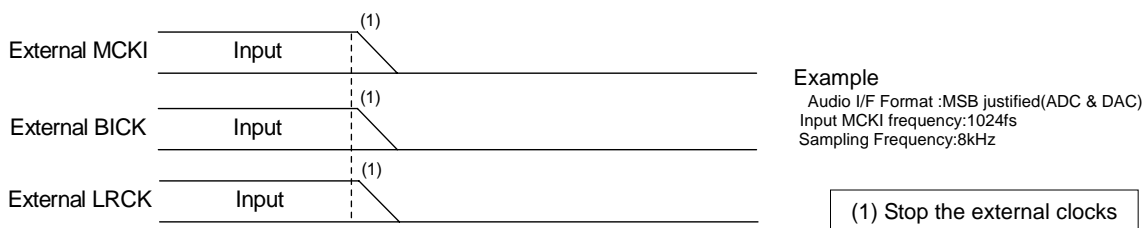


Figure 96. Clock Stopping Sequence (4)

<Example>

- (1) Stop the external MCKI, BICK and LRCK clocks.

5. EXT Master Mode

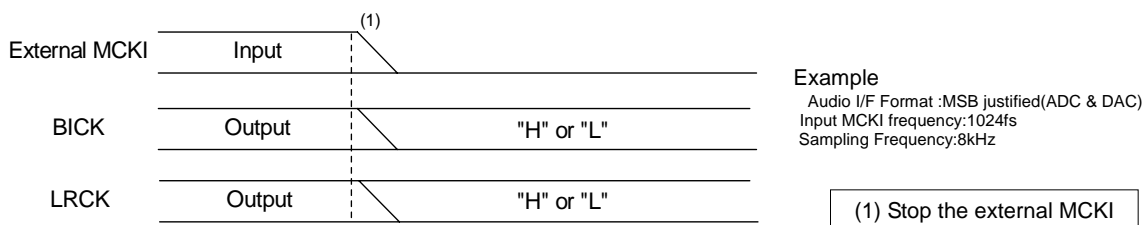


Figure 97. Clock Stopping Sequence (5)

<Example>

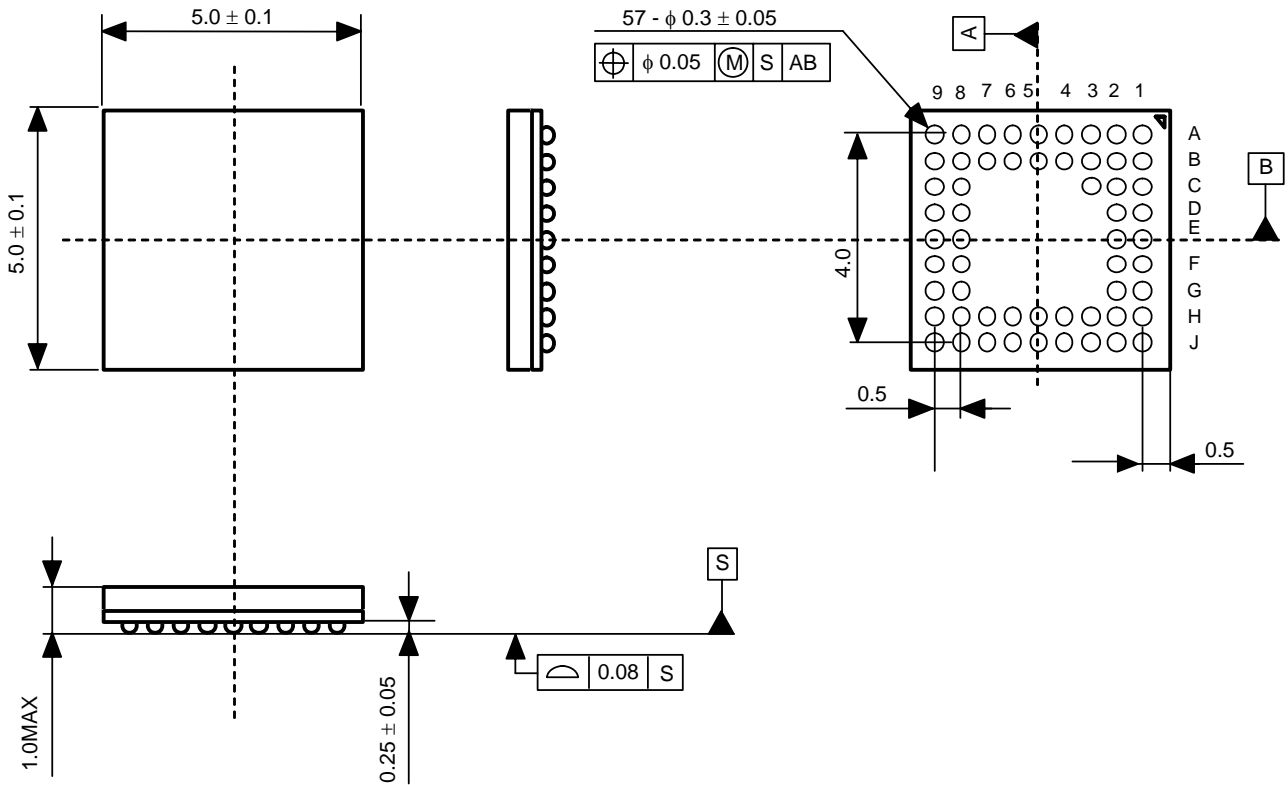
- (1) Stop MCKI clock. BICK and LRCK are fixed to "H" or "L".

■ Power down

Power supply current can be shut down (typ. 20 μ A) by stopping clocks and setting PMVCM bit = "0" after all blocks except for VCOM are powered-down. Power supply current can be also shut down (typ. 1 μ A) by stopping clocks and setting the PDN pin = "L". When the PDN pin = "L", the registers are initialized.

PACKAGE

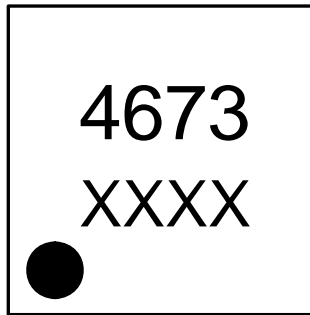
57pin BGA (Unit: mm)



■ **Material & Lead finish**

| | |
|---------------------------|----------|
| Package molding compound: | Epoxy |
| Interposer material: | BT resin |
| Solder ball material: | SnAgCu |

MARKING



XXXX: Date code (4 digit)
Pin #A1 indication

REVISION HISTORY

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|-----------------|----------|---------------|------|----------|
| 07/09/28 | 00 | First Edition | | |

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