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AKD4673-A
Evaluation board Rev.0 for AK4673

GENERAL DESCRIPTION

AKD4673 is an evaluation board for the AK4673, stereo CODEC with built-in MIC/HP amplifier and TSC. The AKD4673 can evaluate A/D converter and D/A converter of the CODEC separately in addition to loopback mode (A/D → D/A). The AKD4673 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector. Moreover, the AKD4673 can also evaluate A/D converter of the TSC with the control software.

■ **Ordering guide**

AKD4673   ---   Evaluation board for AK4673
(Cable for connecting with printer port of IBM-AT, compatible PC and control software are packed with this. This control software does not support Windows NT.)

FUNCTION

- **DIT/DIR with optical input/output**
- **RCA connector for an external clock input**
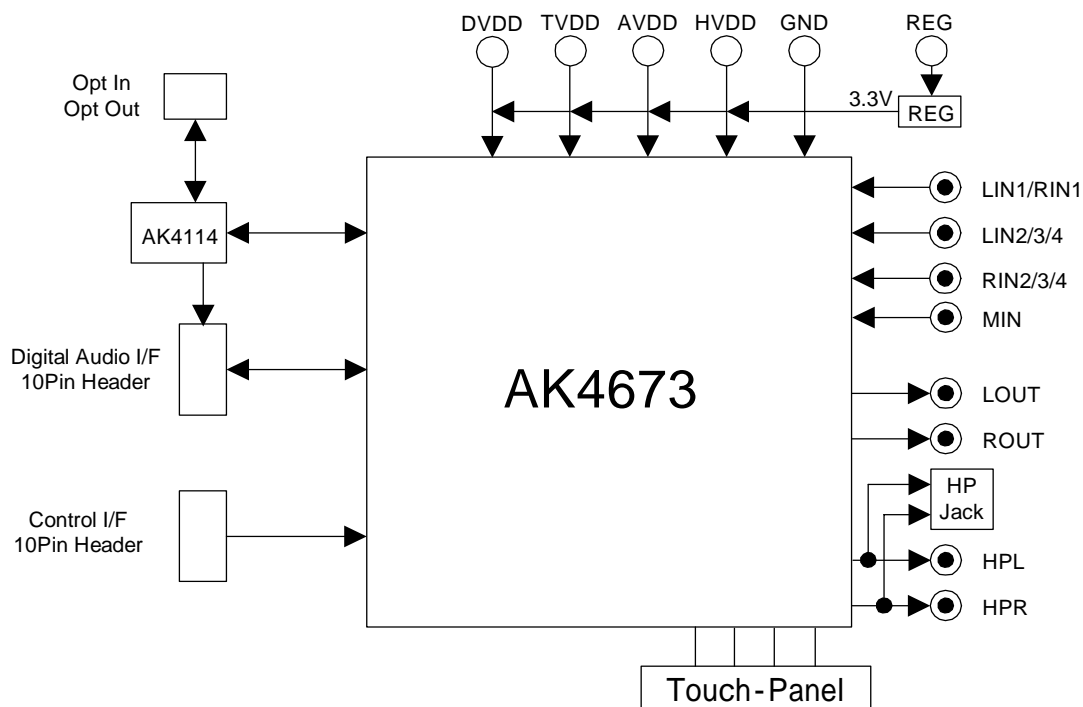- **10pin Header for serial control mode**
- **Touch-Panel I/F**

Figure 1. AKD4673 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual

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■ Operation sequence

(1) Set up the power supply lines.

(1-1) In case of using the regulator.

Set up the jumper pins.

JP	JP3	JP4	JP5	JP6	JP7	JP106	JP107	JP109
	HVDD_SEL	AVDD_SEL	DVDD_SEL	TVDD_SEL	VCC_SEL	TVDD2	TVDD1	TSVDD
State	Short	Short	Short	Short	Short	Short	Short	Short

Set up the power supply lines.
[REG] (red)   = 5.0V   : for regulator (3.3V output : HVDD, AVDD, TVDD1, TVDD2,
                                              TSVDD, DVDD of AK4673)
[D3V] (orange)   = 2.7 ~ 3.6V : for AK4114 and logic (typ. 3.3V)
[AGND] (black)   = 0V   : for analog ground
[DGND] (black)   = 0V   : for logic ground

(1-2) In case of using the power supply connectors.

Set up the jumper pins.

JP	JP3	JP4	JP5	JP6	JP7	JP106	JP107	JP109
	HVDD_SEL	AVDD_SEL	DVDD_SEL	TVDD_SEL	VCC_SEL	TVDD2	TVDD1	TSVDD
State	Open	Open	Open	Open	Open	Short	Short	Short

Set up the power supply lines.
[HVDD] (orange) = 1.6 ~ 3.6V : for HVDD of AK4673 (typ. 3.3V)
[AVDD] (orange) = 1.6 ~ 3.6V : for AVDD and PVDD of AK4673 (typ. 3.3V)
[DVDD] (orange) = 1.6 ~ 3.6V : for DVDD of AK4673 (typ. 3.3V)
[TVDD] (orange) = 1.6 ~ 3.6V : for TVDD1, TVDD2, TSVDD of AK4673 (typ. 3.3V)
[VCC] (orange)   = 1.6 ~ 3.6V : for logic (typ. 3.3V: = DVDD)
[D3V] (orange)   = 2.7 ~ 3.6V : for AK4114 and logic (typ. 3.3V)
[AGND] (black)   = 0V   : for analog ground
[DGND] (black)   = 0V   : for logic ground

* Each supply line should be distributed from the power supply unit.

(2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

(3) Power on.
The AK4673 and AK4114 should be resets once bringing SW1 (PDN) and SW2 (DIR) "L" upon power-up.

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■ **Evaluation mode**

In case of AK4673 evaluation using AK4114, it is necessary to correspond to audio interface format for AK4673 and AK4114. About AK4673's audio interface format, refer to datasheet of AK4673. About AK4114's audio interface format, refer to Table 2 in this manual.

Evaluation of CODEC

(1) External Slave Mode
   (1-1) Evaluation of A/D using DIT of AK4114
   (1-2) Evaluation of D/A using DIR of AK4114
   (1-3) Evaluation of Loop-back using AK4114 <default>
   (1-4) Evaluation of Loop-back that master clock is fed externally, BICK and LRCK are divided with a board

(2) External Master Mode
   (2-1) Evaluation of A/D using DIT of AK4114
   (2-2) Evaluation of D/A using DIR of AK4114
   (2-3) Evaluation of Loop-back using AK4114
   (2-4) Evaluation of Loop-back that master clock is fed externally

(3) PLL Slave Mode
   (3-1) PLL Reference Clock : MCKI pin
      (3-1-1) Evaluation of A/D, D/A using PORT3 (DSP)
      (3-1-2) Evaluation of Loop-back that master clock is fed externally, BICK and LRCK are divided with a board
   (3-2) PLL Reference Clock : BICK or LRCK pin
      (3-2-1) Evaluation of A/D using DIT of AK4114
      (3-2-2) Evaluation of D/A using DIR of AK4114
      (3-2-3) Evaluation of Loop-back using AK4114

(4) PLL Master Mode
   (4-1) Evaluation of Loop-back using AK4114
   (4-2) Evaluation of Loop-back that master clock is fed externally
   (4-3) Evaluation of Internal Loop-back using clock is fed externally

Evaluation of TSC

(1) Position, Pen Pressure

Evaluation of CODEC

JP104, JP102 should be set to short. JP103, JP105 should be set to open.

(1) External Slave Mode

When PMPLL bit is "0", the AK4673 becomes EXT mode. Master clock is input from MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate are MCKI (256fs, 512fs or 1024fs), LRCK (fs) and BICK (≥32fs). The master clock (MCKI) should be synchronized with LRCK. The phase between these clocks does not matter. The input frequency of MCKI is selected by FS1-0 bits.

JP23 (M/S) should be set to "Slave". In addition, the register of AK4673 should be set to "EXT Slave Mode".
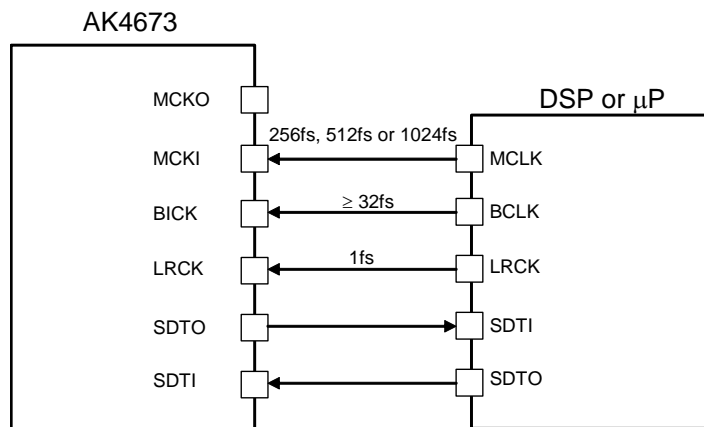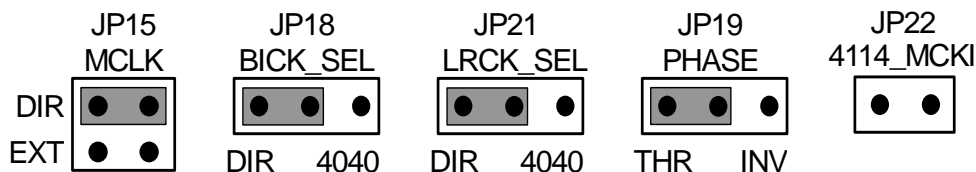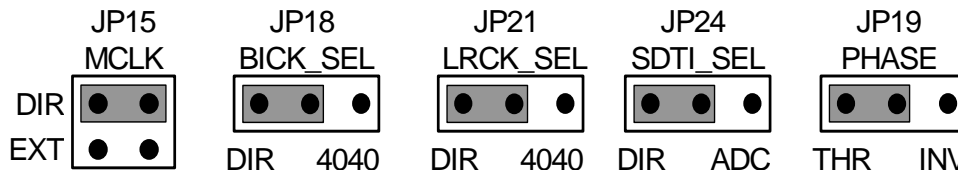

Figure 2. EXT Slave Mode

(1-1) Evaluation of A/D using DIT of AK4114

PORT2 (DIT) and X1 (X'tal) are used. Nothing should be connected to PORT1 (DIR) and PORT3 (DSP). The jumper pins should be set to the following.

(1-2) Evaluation of D/A using DIR of AK4114

PORT1 (DIR) is used. Nothing should be connected to PORT2 (DIT) and PORT3 (DSP). The jumper pins should be set to the following.

When AK4114 is used, JP16 (MKFS) and JP17 (BCFS) are not used. Therefore, JP16 (MKFS) should be set to "256fs" and JP23 (BCFS) should be set to "64fs".

* The AK4114 operates at fs of 32kHz or more. If the fs is slower than 32kHz, this evaluation mode can't be used.

(1-3) Evaluation of Loop-back using AK4114 <Default>

X1 (X'tal) is used. Nothing should be connected to PORT1 (DIR) and PORT3 (DSP).
The jumper pins should be set to the following.

When AK4114 is used, JP16 (MKFS) and JP17 (BCFS) are not used. Therefore, JP16 (MKFS) should be set to "256fs" and JP23 (BCFS) should be set to "64fs".

* The AK4114 operates at fs of 32kHz or more. If the fs is slower than 32kHz, this evaluation mode can't be used.

(1-4) Evaluation of Loop-back where master clock is fed externally, BICK and LRCK are generated by on-board divider.

J11 (EXT) is used. MCKI is supplied from J11 (EXT). BICK and LRCK are generated by 74HC4040 on AKD4671-A. Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT3 (DSP).
The jumper pins should be set as the following.

When a termination (51Ω) is unnecessary, please set JP14 (EXT) open.

JP16 (MKFS), JP17 (BCFS), and JP20 (LRCK) should be set according to the frequency of MCLK, BICK and LRCK.

(2) External Master Mode

The AK4673 becomes EXT Master Mode by setting PMPLL bit = "0" and M/S bit = "1". Master clock can be input via MCKI pin, without using on-chip PLL circuit. The clock required to operate is MCKI (256fs, 512fs, or 1024 fs). The input frequency of MCKI is selected by FS1-0 bits.
JP23 (M/S) should be set to "Master". In addition, the register of AK4673 should be set to "EXT Master Mode".
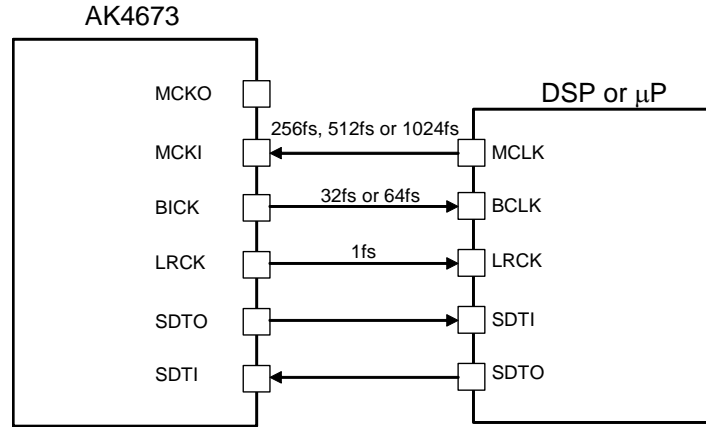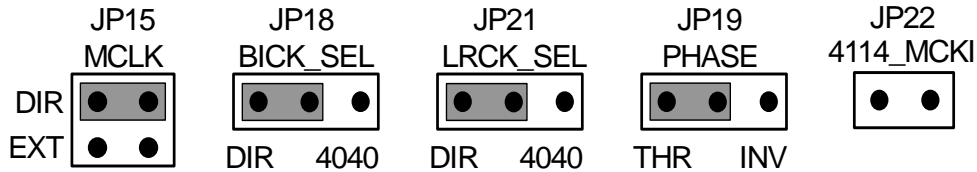
Figure 3. EXT Master Mode
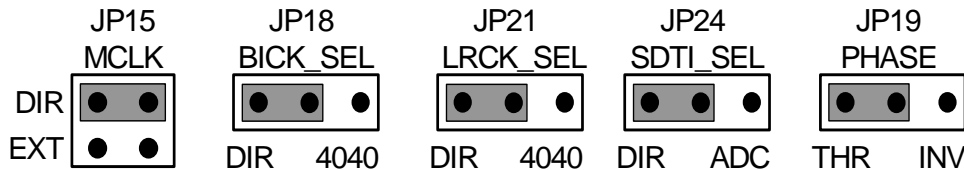
(2-1) Evaluation of A/D using DIT of AK4114

X1 (X'tal) and PORT2 (DIT) are used. Nothing should be connected to PORT1 (DIR) and PORT3 (DSP).
In Master Mode, BICK and LRCK of AK4671 should be input to AK4114. Please refer to Table 2 on page 13.
BCKO bit = "1" (Register Address 04H)
The jumper pins should be set as the following.

* The AK4114 operates at fs of 32kHz or more. If the fs is slower than 32kHz, this evaluation mode can't be used.
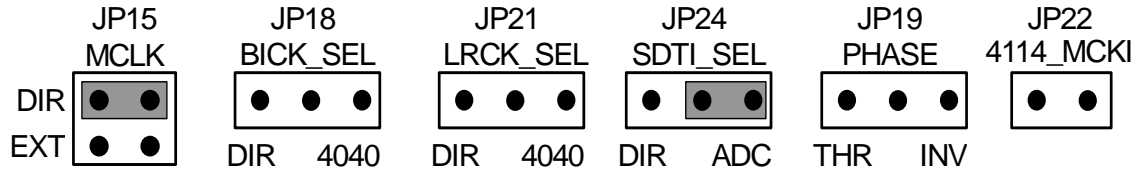
(2-2) Evaluation of D/A using DIR of AK4114

PORT1 (DIR) is used. Nothing should be connected to PORT2 (DIT) and PORT3 (DSP).
In Master Mode, BICK and LRCK of AK4671 should be input to AK4114. Please refer to Table 2 on page 13.
BCKO bit = "1" (Register Address 04H).
The jumper pins should be set as the following.

* The AK4114 operates at fs of 32kHz or more. If the fs is slower than 32kHz, this evaluation mode can't be used.
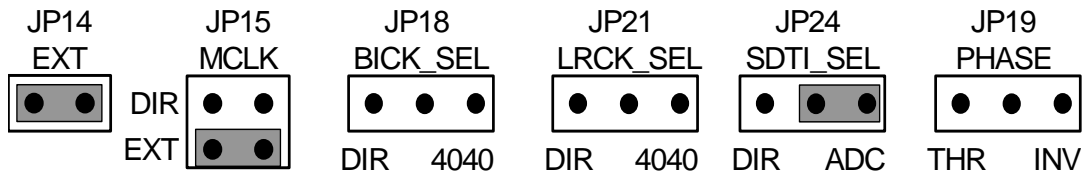
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(2-3) Evaluation of Loop-back using AK4114

X1 (X'tal) is used. Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT3 (DSP).
The jumper pins should be set as the following.

JP15	JP18	JP21	JP24	JP19	JP22
MCLK	BICK_SEL	LRCK_SEL	SDTI_SEL	PHASE	4114_MCKI

DIR / EXT (JP15: DIR shorted)
JP18: DIR — 4040
JP21: DIR — 4040
JP24: DIR — ADC (ADC shorted)
JP19: THR — INV
JP22

JP16 (MKFS) should be set according to the frequency of MCLK.

(2-4) Evaluation of Loop-back where master clock is fed externally

J11 (EXT) is used. MCKI is supplied from J11 (EXT). BICK and LRCK are generated by 74HC4040 on
AKD4671-A. Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT3 (DSP).
The jumper pins should be set as the following.

JP14	JP15	JP18	JP21	JP24	JP19
EXT	MCLK	BICK_SEL	LRCK_SEL	SDTI_SEL	PHASE

JP14: EXT (shorted)
JP15: DIR / EXT (EXT shorted)
JP18: DIR — 4040
JP21: DIR — 4040
JP24: DIR — ADC (ADC shorted)
JP19: THR — INV

*When a termination (51Ω) is unnecessary, please set JP14 (EXT) open.

JP16 (MKFS) should be set according to the frequency of MCLK.

(3) PLL Slave Mode

A reference clock of PLL is selected among the input clocks to MCKI, BICK or LRCK pin. The required clock to the AK4673 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits.
BICK and LRCK inputs should be synchronized with MCKO output. The phase between MCKO and LRCK dose not matter. MCKO pin outputs the frequency selected by PS1-0 bits and the output is enabled by MCKO bit.
Sampling frequency can be selected by FS3-0 bits.
JP23 (M/S) should be set to "Slave". In addition, the register of AK4673 should be set to "PLL Slave Mode".
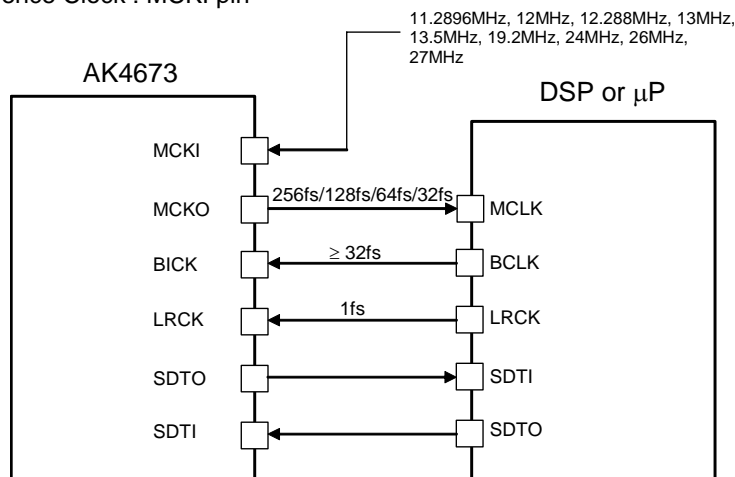
(3-1) PLL Reference Clock : MCKI pin

Figure 4. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

(3-1-1) Evaluation of A/D, D/A using PORT3 (DSP)

PORT3 (DSP) is used. Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and J11 (EXT).
SDTI, SDTO, LRCK and BICK of PORT3 are respectively connected with SDTO, SDTI, LRCK and BICK of DSP. Connect the test pin (MCKO) to DSP when MCKO is supplied to DSP.
The jumper pins should be set as the following.
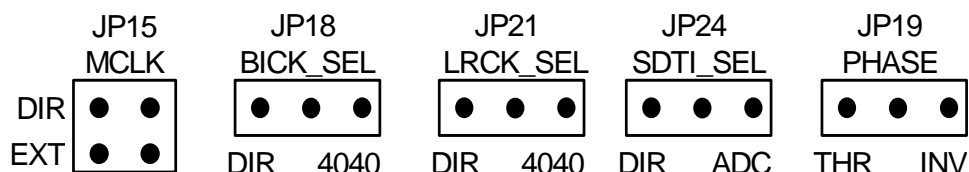
(3-1-2) Evaluation of Loop-back that master clock is fed externally, BICK and LRCK are divided with a board

J11 (EXT) is used. MCKI is supplied from J11 (EXT). BICK and LRCK are generated by 74HC4040 on AKD4671-A.Nothing should be connected to PORT1 (DIR), PORT2 (DIT) and PORT3 (DSP).
The jumper pins should be set as the following.

*When a termination (51Ω) is unnecessary, please set JP14 (EXT) open.
JP16 (MKFS) should be set to MCKO; JP17 (BCFS), and JP20 (LRCK) should be set according to the frequency of BICK and LRCK.
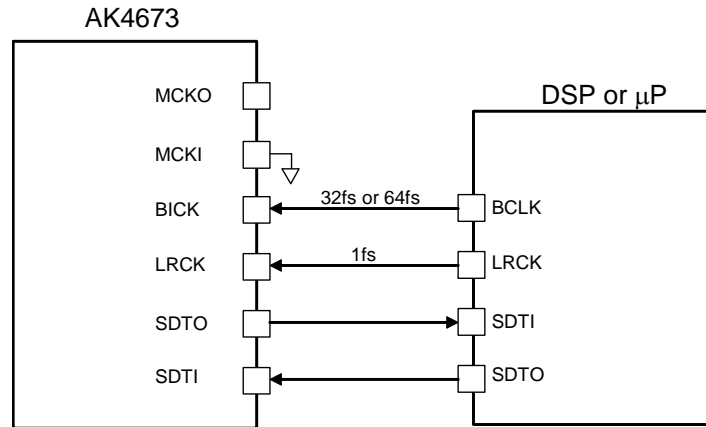
(3-2) PLL Reference Clock : BICK or LRCK pin

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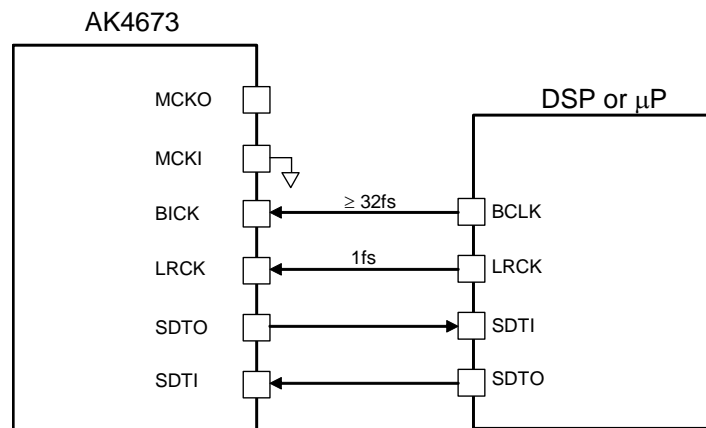Figure 5. PLL Slave Mode 2 (PLL Reference Clock: BICK pin)

AK4673

Figure 6. PLL Slave Mode 2 (PLL Reference Clock: LRCK pin)

(3-2-1) Evaluation of A/D using DIT of AK4114

X1 (X'tal) and PORT2 (DIT) are used. Nothing should be connected to PORT1 (DIR), PORT3 (DSP) and J11 (EXT).
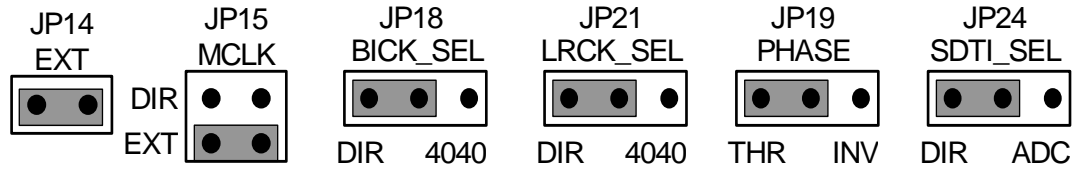The jumper pins should be set as the following.

* The AK4114 operates at fs of 32kHz or more. If the fs is slower than 32kHz, this evaluation mode can't be used.

(3-2-2) Evaluation of D/A using DIR of AK4114

PORT1 (DIR) is used. Nothing should be connected to PORT2 (DIT), PORT3 (DSP) and J11 (EXT).
The jumper pins should be set as the following.

JP14 EXT	JP15 MCLK	JP18 BICK_SEL	JP21 LRCK_SEL	JP19 PHASE	JP24 SDTI_SEL

* The AK4114 operates at fs of 32kHz or more. If the fs is slower than 32kHz, this evaluation mode can't be used.

(3-2-3) Evaluation of Loop-back using AK4114

X1 (X'tal) is used. Nothing should be connected to PORT1 (DIR), PORT2 (DIT), PORT3 (DSP) and J11 (EXT).
The jumper pins should be set as the following.

JP14 EXT	JP15 MCLK	JP18 BICK_SEL	JP21 LRCK_SEL	JP22 4114_MCKI	JP19 PHASE	JP24 SDTI_SEL

* The AK4114 operates at fs of 32kHz or more. If the fs is slower than 32kHz, this evaluation mode can't be used.

(4) PLL Master Mode

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz or 27MHz) is input to MCKI pin, the MCKO, BICK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits and the output is enabled by MCKO bit. The BICK output frequency is selected between 32fs or 64fs, by BCKO bit.
JP23 (M/S) should be set to "Master". In addition, the register of AK4673 should be set to "PLL Master Mode".
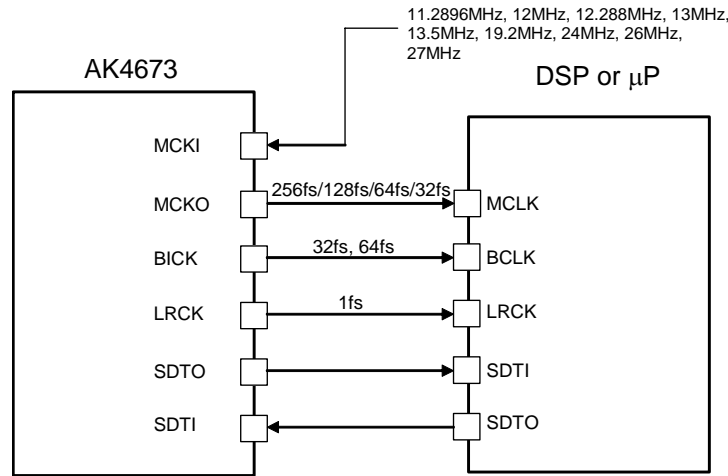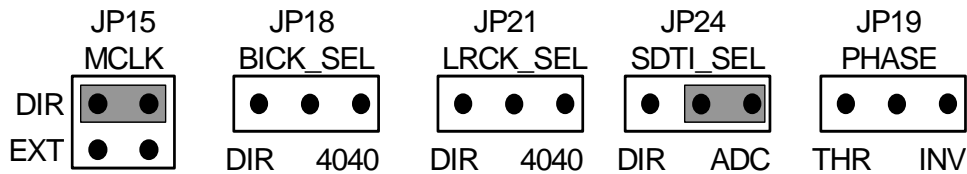

Figure 7. PLL Master Mode

(4-1) Evaluation of Loop-back using AK4114

X1 (X'tal) is used. Nothing should be connected to PORT1 (DIR), PORT3 (DSP) and J11 (EXT).
Using the AK4673's internal PLL it is possible to evaluate various sampling frequencies.
The jumper pins should be set to the following.

(4-2) Evaluation of Loop-back that master clock is fed externally

J11 (EXT) is used. Nothing should be connected to PORT1 (DIR) and PORT3 (DSP). Exclude X'tal oscillator from X1. Using the AK4673's internal PLL it is possible to evaluate various sampling frequencies.
The jumper pins should be set to the following.
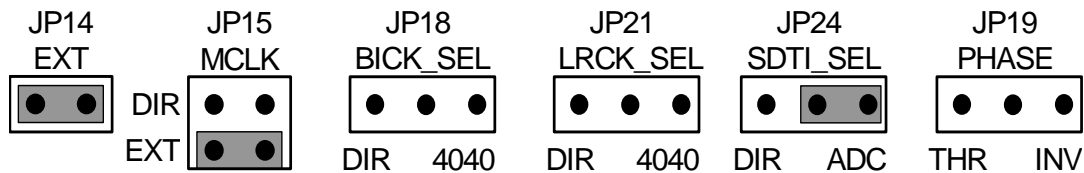
(4-3) Evaluation of Internal Loop-back using clock is fed externally

J11 (EXT) is used. Nothing should be connected to PORT1(DIR) and PORT3 (DSP).

It can be evaluated at internal loop-back mode (LOOP bit = "1").

Using the AK4673's internal PLL it is possible to evaluate various sampling frequencies.

The jumper pins should be set to the following.
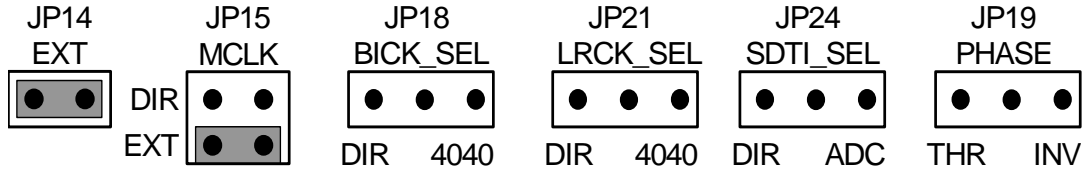
Evaluation of TSC

PORT4 (CTRL) should be directly connected to the parallel port. (Figure 9)
JP103, JP105 should be set to short. JP102, JP104 should be set to open.

(1) Position, Pen Pressure

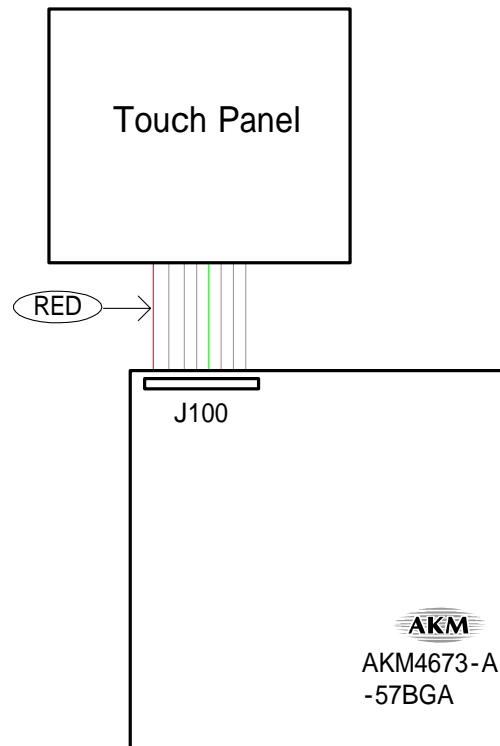4-wire touch-panel (X+, X-, Y+ and Y-) should be connected to J100 connector as the following figure.

Figure 8. Connect of Touch Panel

■ DIP Switch set up

[S1] : Mode Setting of AK4114 and AK4673
ON is "H", OFF is "L".

No.	Name	ON ("H")	OFF ("L")	Default
1	DIF2	AK4114 Audio Format Setting See Table 2		ON
2	DIF1			OFF
3	DIF0			OFF
4	OCKS1	AK4114 Master Clock Setting : See Table 3		OFF
5	CAD0	AK4673Control Mode Setting : See Table 4		OFF
6	I2C			OFF

Table 1. Mode Setting for AK4673 and AK4114

DIF2	DIF1	DIF0	AK4114DAUX	AK4114SDTO	LRCK	I/O	BICK	I/O	
0	0	0	24bit, Left justified	16bit, Right justified	H/L	O	64fs	O	
0	0	1	24bit, Left justified	18bit, Right justified	H/L	O	64fs	O	
0	1	0	24bit, Left justified	20bit, Right justified	H/L	O	64fs	O	
0	1	1	24bit, Left justified	24bit, Right justified	H/L	O	64fs	O	
1	0	0	24bit, Left justified	24bit, Left justified	H/L	O	64fs	O	default
1	0	1	24bit, I^2S	24bit, I^2S	L/H	O	64fs	O	
1	1	0	24bit, Left justified	24bit, Left justified	H/L	I	64-128fs	I	
1	1	1	24bit, I^2S	24bit, I^2S	L/H	I	64-128fs	I	

Table 2. Setting for AK4114 Audio Interface Format

OCKS1	MCKO1	X'tal	
0	256fs	256fs	default
1	512fs	512fs	

Table 3. AK4114 Master Clock Setting

■ **Other jumper pins set up**

Main Board

[JP1] (GND): Analog ground and Digital ground
      OPEN: Separated.
      SHORT: Common. (The connector "DGND" can be open.) <Default>

[JP3] (HVDD_SEL): HVDD of the AK4673
      OPEN: HVDD is supplied from "HVDD" jack.
      SHORT: Supplied from the regulator ("HVDD" jack should be open). <Default>

[JP4] (AVDD_SEL): AVDD of the AK4673
      OPEN: AVDD is supplied from "AVDD" jack.
      SHORT: Supplied from the regulator ("AVDD" jack should be open). <Default>

[JP5] (DVDD_SEL): DVDD of the AK4673
      OPEN: DVDD is supplied from "DVDD" jack.
      SHORT: DVDD is supplied from "AVDD" ("DVDD" jack should be open). <Default>

[JP6] (TVDD_SEL): TVDD of the AK4673
      OPEN: TVDD is supplied from "TVDD" jack.
      SHORT: TVDD is supplied from "DVDD" ("TVDD" jack should be open). <Default>

[JP7] (VCC_SEL): VCC of the AK4673
      OPEN: VCC is supplied from "VCC" jack.
      SHORT: VCC is supplied from "TVDD" ("VCC" jack should be open). <Default>

[JP16] (MKFS): MCLK Frequency
      256fs: 256fs. <Default>
      512fs: 512fs.
      1024fs: 1024fs.
      384/768fs: 384fs
      MCKO: MCKO is used.

[JP17] (BCFS): BICK Frequency
      32fs: 32fs (When MCLK is 256fs or 512fs or 768fs or 1024fs.)
      64fs: 64fs (When MCLK is 256fs or 512fs or 768fs or 1024fs.) <Default>
      32fs-384: 32fs (When MCLK is 384fs.)
      64fs-384: 64fs (When MCLK is 384fs.)

[JP22] (4114_MCKI): AK4114 Clock Source
      OPEN: X'tal of AK4114 is used. <Default>
      SHORT: X'tal of AK4114 is not used.

[JP25] (CTRL_SEL):Serial Control Interface (Must be set to I2C)
      3-WIRE: Invalid
      I2C: I^2C-bus Control Mode <Default>

Sub Board

[JP100] (I2CA_SEL): I2C (Must be set to H)
      H: Enable <Default>
      L: Unable

■ The function of the toggle SW

[SW1] (PDN): Power down of AK4673. Keep "H" during normal operation.

[SW2] (DIR): Power down of AK4114. Keep "H" during normal operation.
Keep "L" when AK4114 is not used.

■ Indication for LED

[LED1] (ERF): Monitor INT0 pin of the AK4114. LED turns on when some error has occurred to AK4114.

■ Serial Control

The AK4673 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT4 (CTRL) with PC by 10 wire flat cable packed with the AKD4673.Table 3 shows switch and jumper settings for serial control.
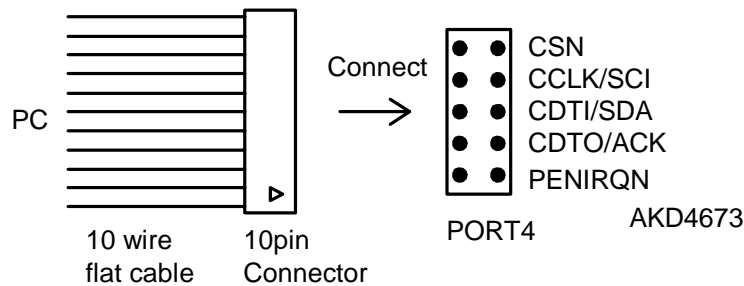

Figure 9. Connect of 10 wire flat cable

Mode		S1		JP25	JP100
		I2C	CAD0	CTRL_SEL	I2CA-SEL
I2C	CAD0=0	ON	OFF	I2C	H
	CAD0=1	ON	ON		

Table 4. Serial Control Setting

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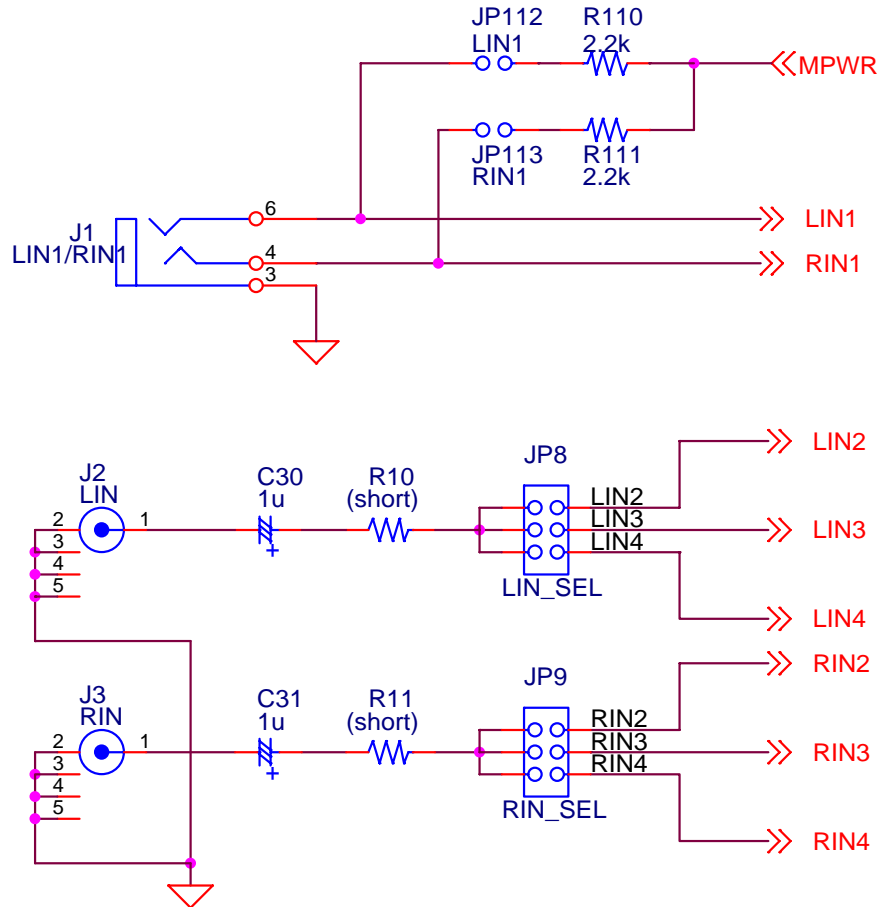
When MIN (shared with LIN3) Input path of AK4673 is used, JP108 should be set as below.
   AIN3bit ="0" (Register Address 21H)

```
┌───┐
│ ● │ MIN
│ ● │
└───┘
  ● LIN3
JP108
```
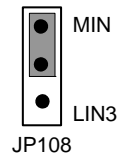
(2) Output Circuits

    (2-1)   HP Output Circuit

Figure 11. HP Output Circuit

(2-1-1) In case that signal is output from J7 and J8.

(2-1-2) In case that signal is output from J9.

(2-2)   LOUT/ROUT (LOP/LON) Output Circuit

Figure 12. LOUT/ROUT(LOP/LON) Output Circuit

(2-1-1) In case that signal is output from J5 and J6.

(2-1-1) In case that signal is output from J9.

∗ AKM assumes no responsibility for the trouble when using the above circuit examples.
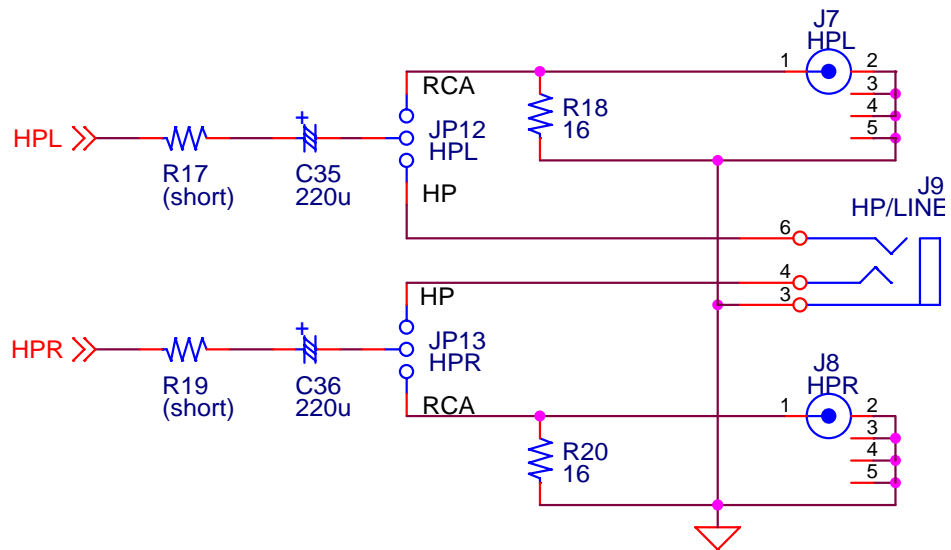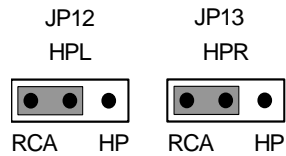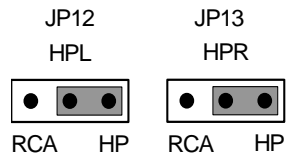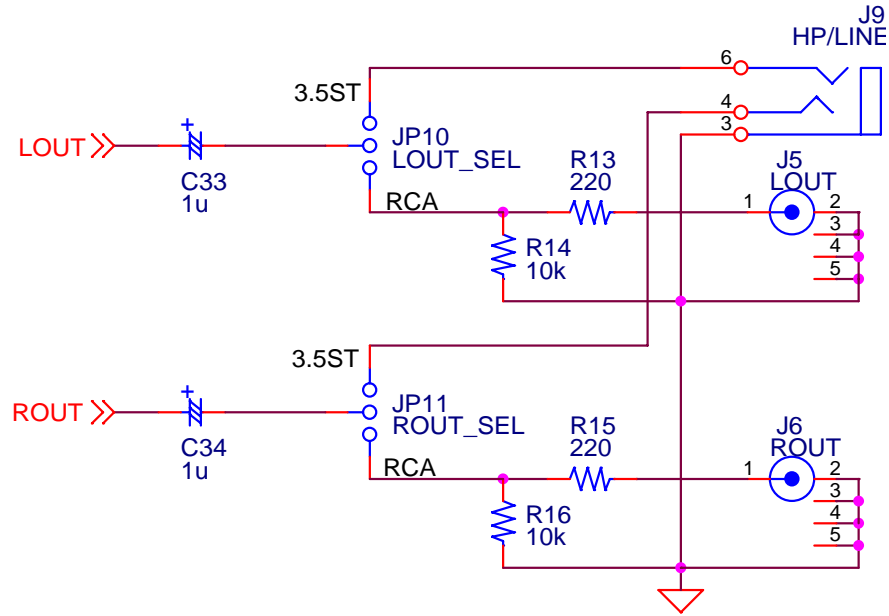
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Control Software Manual For the Evaluation of CODEC

■ **Set-up of evaluation board and control software**

1. Set up the AKD4673-A according to previous term.

2. Connect IBM-AT compatible PC with AKD4673-A by 10-line type flat cable (packed with AKD4673-A). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AK4673-A Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "AKD4673.exe" to set up the control program.

5. Then please evaluate according to the follows.

■ **Operation flow**

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.

■ **Explanation of each buttons**

[Port Reset] :	Set up the USB interface board (AKDUSBIF-A) .
[Write default] :	Initialize the register of AK4673.
[All Write] :	Write all registers that is currently displayed.
[Function1] :	Dialog to write data by keyboard operation.
[Function2] :	Dialog to write data by keyboard operation.
[Function3] :	The sequence of register setting can be set and executed.
[Function4] :	The sequence that is created on [Function3] can be assigned to buttons and executed.
[Function5]:	The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
[SAVE] :	Save the current register setting.
[OPEN] :	Write the saved values to all register.
[Write] :	Dialog to write data by mouse operation.
[Filter] :	Set Programmable Filter (FIL1, FIL3, EQ) of AK4673 easily.

■ **Indication of data**

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

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■ **Explanation of each dialog**

1. **[Write Dialog]**: Dialog to write data by mouse operation

   There are dialogs corresponding to each register.

   Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "1". If not, "L" or "0".

   If you want to write the input data to AK4673, click [OK] button. If not, click [Cancel] button.

2. **[Function1 Dialog]** : Dialog to write data by keyboard operation

   Address Box: Input registers address in 2 figures of hexadecimal.
   Data Box: Input registers data in 2 figures of hexadecimal.

   If you want to write the input data to AK4673, click [OK] button. If not, click [Cancel] button.

3. **[Function2 Dialog]** : Dialog to evaluate IVOL and DVOL

   Address Box: Input registers address in 2 figures of hexadecimal.
   Start Data Box: Input starts data in 2 figures of hexadecimal.
   End Data Box: Input end data in 2 figures of hexadecimal.
   Interval Box: Data is written to AK4673 by this interval.
   Step Box: Data changes by this step.
   Mode Select Box:
           If you check this check box, data reaches end data, and returns to start data.
           [Example]   Start Data = 00, End Data = 09
               Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

           If you do not check this check box, data reaches end data, but does not return to start data.
           [Example]   Start Data = 00, End Data = 09
               Data flow: 00 01 02 03 04 05 06 07 08 09

   If you want to write the input data to AK4673, click [OK] button. If not, click [Cancel] button.

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4. [Save] and [Open]

4-1. [Save]

Save the current register setting data. The extension of file name is "akr".

(Operation flow)
(1) Click [Save] Button.
(2) Set the file name and push [Save] Button. The extension of file name is "akr".

4-2. [Open]

   The register setting data saved by [Save] is written to AK4673. The file type is the same as [Save].

(Operation flow)
(1) Click [Open] Button.
(2) Select the file (*.akr) and Click [Open] Button.

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5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
 Set the address, Data and Interval time. Set "-1" to the address of the step where the sequence should be paused.

(3) Click [Start] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [Save] and [Open] button on the Function3 window. The extension of file name is "aks".

Figure 13. Window of [F3]

6. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in Figure 14 opens.
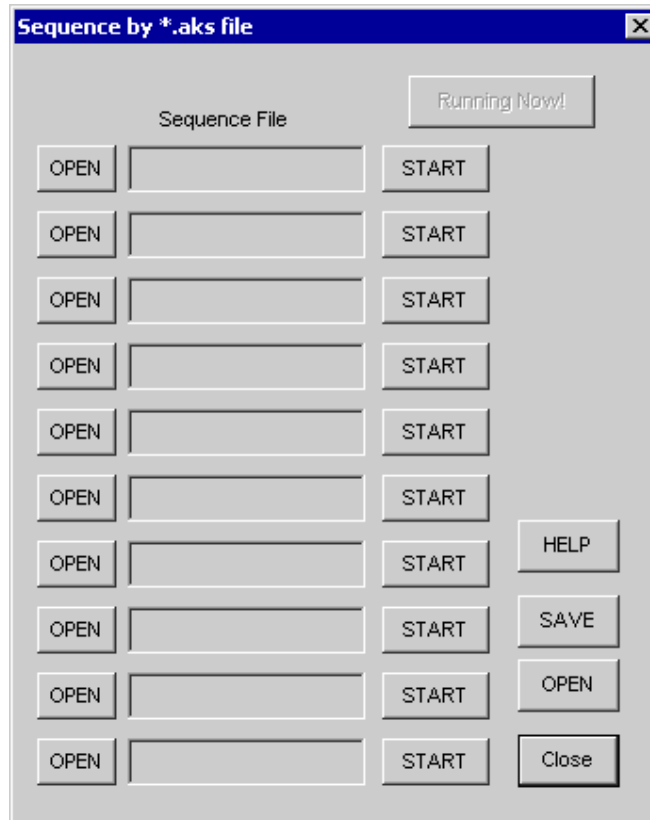
Figure 14. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 15.
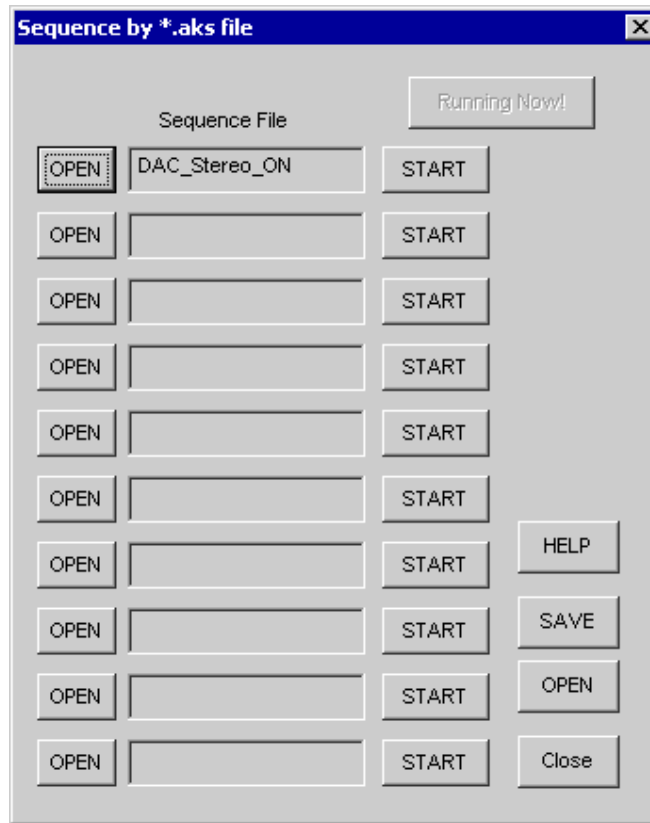
Figure 15. [F4] window(2)

(2) Click [START] button, then the sequence is executed.

3-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The sequence file names can assign be saved. The file name is *.ak4.

[OPEN] : The sequence file names assign that are saved in *.ak4 are loaded.

3-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. When [F5] button is clicked, the following window as shown in Figure 16 opens.
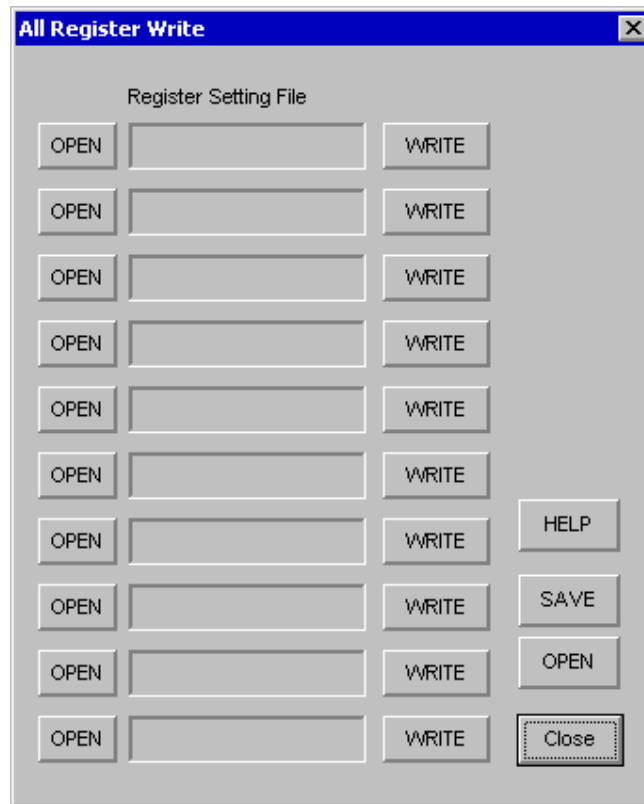

Figure 16. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

   The register setting file name is displayed as shown in Figure 17.

(2) Click [WRITE] button, then the register setting is executed.
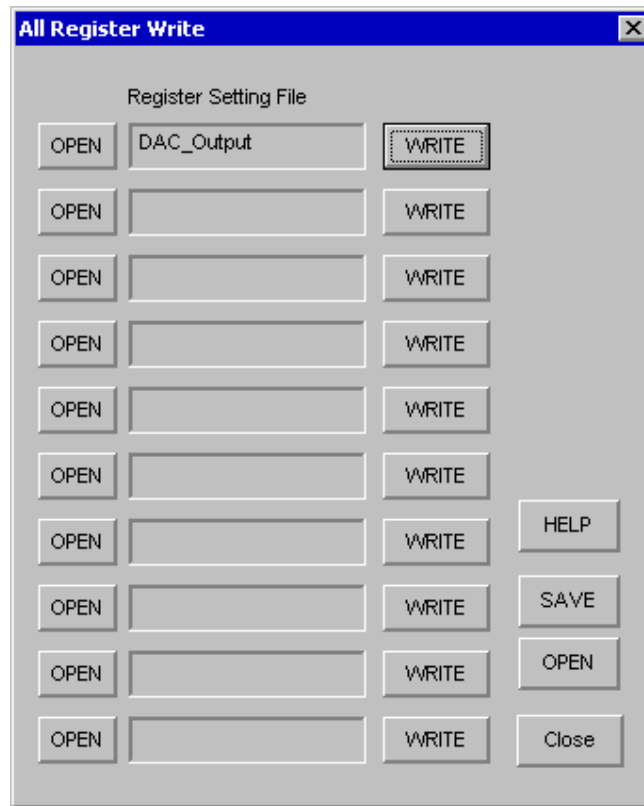
Figure 17. [F5] windows (2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The register setting file names assign can be saved. The file name is *.ak5.

[OPEN] : The register setting file names assign that are saved in *.ak5 are loaded.

7-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

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8. [Filter Dialog]

This dialog can easily set the AK4673's programmable filter.
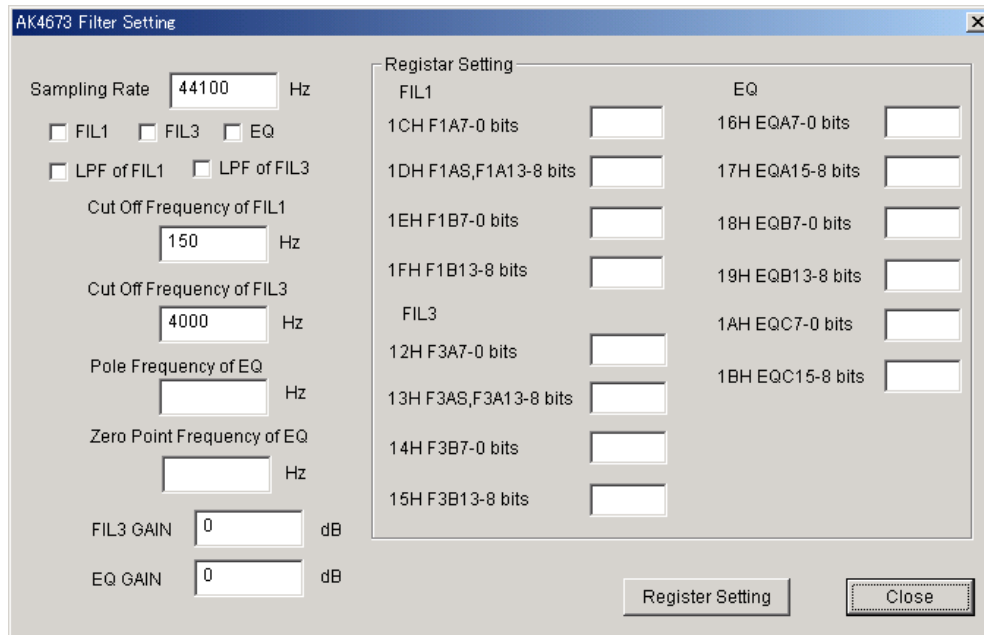
Figure 18. [Filter] window

8-1. Value input columns on left side

[Sampling Rate]	→ Input value of sampling frequency [unit : Hz] <default : 44100>
[Cut Off Frequency of FIL1]	→ Input value of cut off frequency of FIL1 [unit : Hz] <default : 150>
[Cut Off Frequency of FIL3]	→ Input value of cut off frequency of FIL3 [unit : Hz] <default : 4000>
[Pole Frequency of EQ]	→ Input value of pole frequency of EQ [unit : Hz]
[Zero Frequency of EQ]	→ Input value of zero frequency of EQ [unit : Hz]
[FIL3 GAIN]	→ Input value of gain of FIL3 (0~−10dB) [unit : dB]
[EQ GAIN]	→ Input value of gain of EQ (+12~0dB) [unit : dB]

8-2. Check box on left side

Check Box	Check	Check off
FIL1	FIL1 bit ="1"	FIL1 bit ="0"
FIL3	FIL3 bit ="1"	FIL3 bit ="0"
EQ	EQ bit ="1"	EQ bit ="0"
LPF of FIL1	F1AS bit ="1"(LPF)	F1AS bit ="0"(HPF)
LPF of FIL3	F3AS bit ="1"(LPF)	F3AS bit ="0"(HPF)

8-2. [Register Setting] panel and [Register Setting] button on right side

Click [Register setting] button, then filter coefficient set by 8-1 and 8-2 is written on [Register setting] panel. (It is also written to the actual control register of the AK4673.)

■ Parallel Port Driver install

Attached software is the application software, which checks the function of the AK4673. Windows(R) Win 98, Win 2K, and Win XP are supported. However, to make it operate on Win2K and XP, it is necessary to install driver in advance. Please follow a procedure with reference to DriverSetupe.pdf. Installation of a driver is unnecessary to use it by the Windows 98 system.

■ Run the software (AK4673_TSC.exe)

This software valuates the function of the AK4673 TSC block. First match Port Address of your PC environment. Measurements with pressed by pen or stylus on the touch panel are started when the start button is clicked after select Channel Selection, MODE, and Power Down 0. A result will be displayed on AD OUT Section. When carrying out position detection, the position where pen clicked on the touch panel is measured.

Operation can set up two control commands. Continuous operation can be performed. Each data (mean, max, and min) is also displayed at the same time. PENIRQN can be seen by the break of a command.

Figure 19. TSC control soft window

■ Trouble Shooting

1. Application error is occurred and doesn't start up
    If the operating system is Window2000/XP, Please install AKM port driver in advance of run the AK4673_TSC.exe.

2. MEAN value in AD OUT section does not change until click start button (cannot write control command to AK4673).
    Please set the port address correctly to your PC platform environment.

3. The mean, max, min value doesn't change wherever the pen is pressed down on the panel.
    There is a possibility of the trouble of the contact of the relay connector (plat 8pin-8-wire female dip converter) that connects the touch panel. Measure panel seat resistance (XP-XN, YP-YN), and check the resistance. Generally, the panel seat resistance is hundreds of Ω. There is a possibility that the touch panel is not correctly connected if the resistance is over thousands of kΩ. Please connect the connector and check the resistance value again.

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Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
07/05/30	KM086000	0	First edition	

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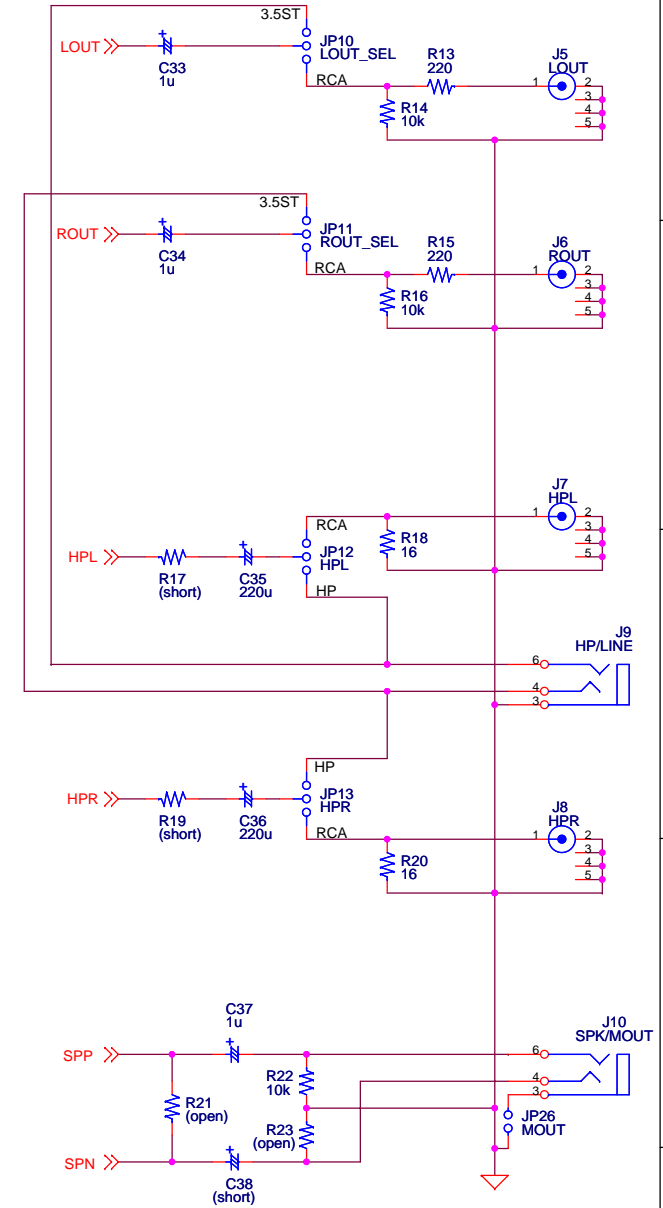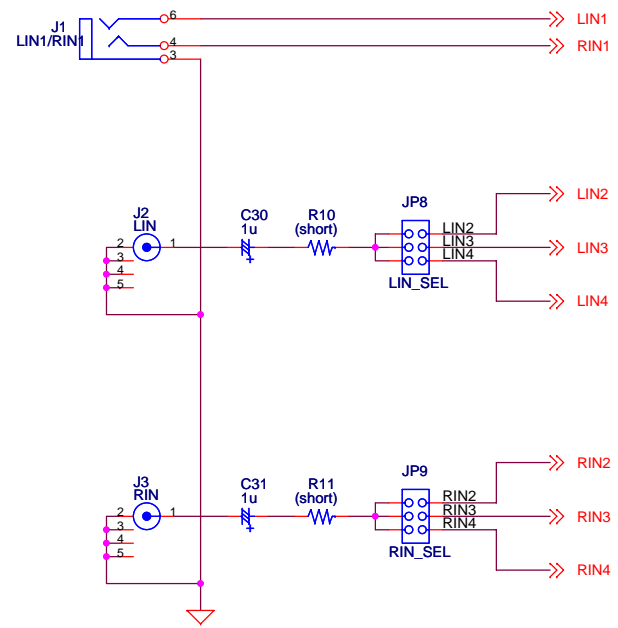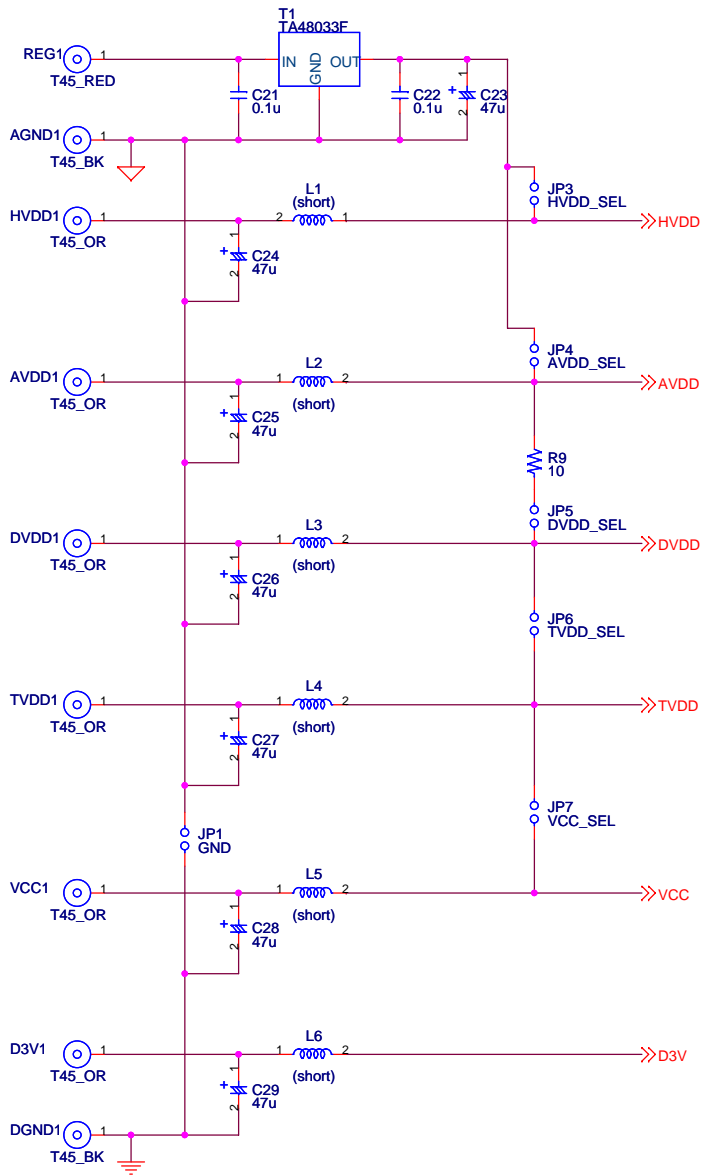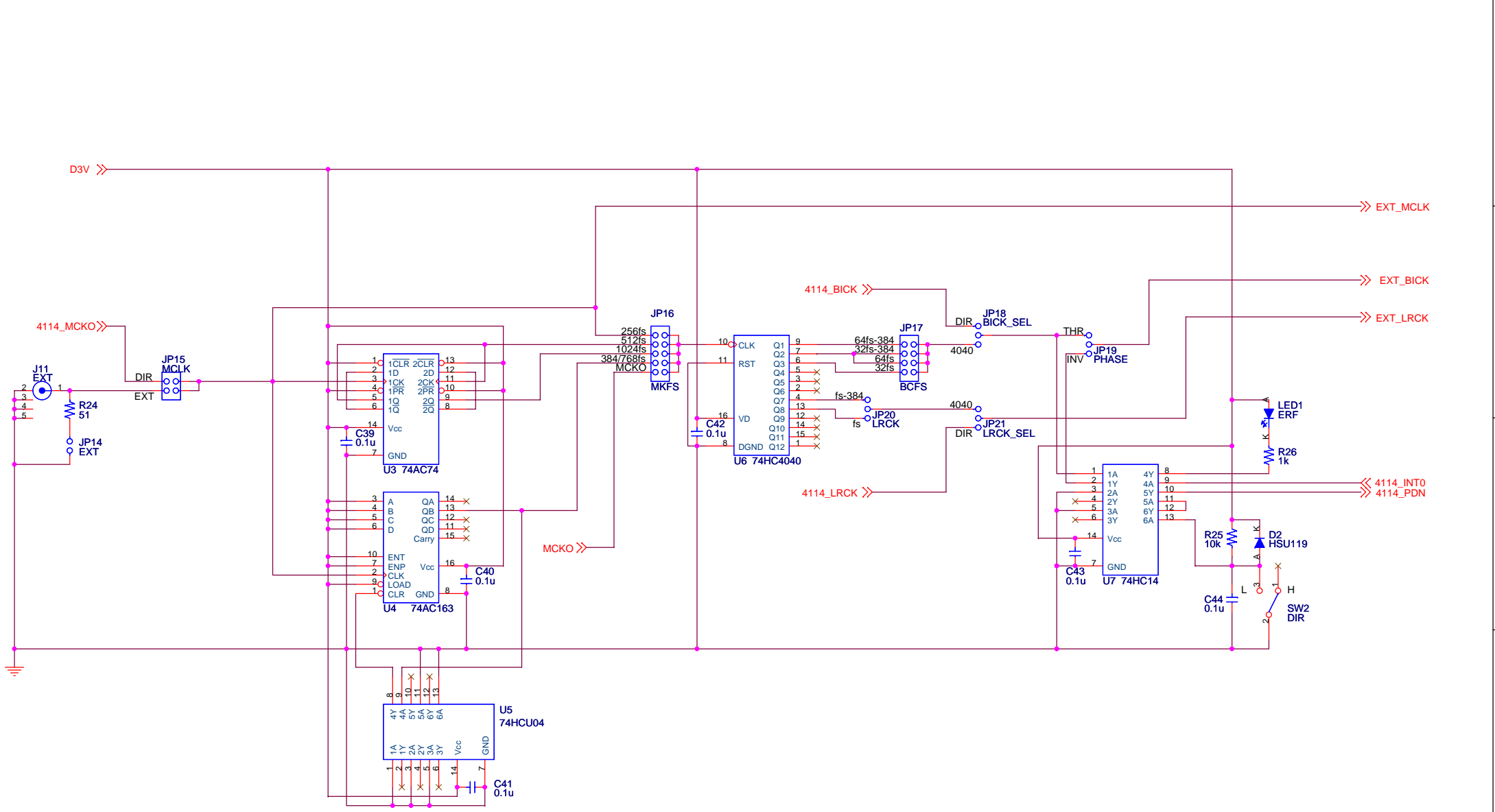● Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
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AK4673

VCC
U2
74HC14
1A 1Y 2A 2Y 3A 3Y
4Y 4A 5Y 5A 6Y 6A
Vcc GND
R8 10k
D1 HSU119
C20 0.1u
C19 0.1u
SW1 PDN
L H

端面 外 内
TouchScreen
J100
YN YP XN XP

CN2 12pin
CSN/CAD0 I2C AVDD
TP131 AVDD TP130 VSS1 MPWR TP129
TP137 PDN
R109 51
R106 2.2k JP110 RIN1
R107 2.2k JP111 LIN1

C117 4.7n
TP133 I2CA
R108 10k
TP138 YN
TP136 XN
JP101 VCOC-SEL VCOC
RIN3
TP134 YP
TP132 XP
AVDD-IN
JP100 H
AVDD-IN
I2CA-SEL
TP139 CADA
C121 0.01u
C120 0.01u TP135 VCOC/RIN3
C119 0.01u
C118 0.01u
C115 10u
C116 0.1u

U1
NC CADA YN PDN XN NC VCOC YP I2CA XP MPWR AVDD VSS1 NC
H1 G1 G2 E1 F2 E2 E1 D2 D1 C2 C1 B1 A1
J2 SDAA
H2 SCLA
H3 SDTI
J3 SDTO
H4 LRCK
J4 BICK
H5 NC
J5 VSS3
J6 DVDD
H6 TVDD2
H7 NC
J7 TVDD1
H8 MCKO
J9 NC

CN4 12pin
CCLK/SCL
CDTI/SDA
4371_SDTI
4371_SDTO
4371_LRCK
4371_BICK
DVDD
TVDD
PENIRQN-OUT

JP102 SDAA
JP103 SDAT
JP104
JP105 SCLA SCLT
TP100 SDAA
TP101 SCLA

R100 51
R101 51
R102 51
R103 51
R104 51
TP102 SDTI
TP103 SDTO
TP104 LRCK
TP105 BICK
TP106 DVDD

TP107 VSS3

TP108 TVDD2
JP106 TVDD2
C100 10u C101 0.1u
C102 10u C103 0.1u
TP109 TVDD1
JP107 TVDD1
C104 10u C105 0.1u

VCOM
RIN1/IN1+
LIN1/IN1-
NC
TSVDD
LIN2/IN2-
RIN2
NC
MIN/LIN3
LOUT/LOP
ROUT/LON
LIN4/IN4+
NC
RIN4/IN4-
B2 A3 B3 A4 B4 B5 A5 B6 A6 A7 B7 B8 A8

C113 0.1u C114 2.2u
TP128 VCOM
TP127 RIN1
C112 1u
C111 1u
TP126 LIN1
C109 0.1u C110 10u TP125 TSVDD JP109 TSVDD
TP124 LIN2
TP123 RIN2
JP108 MIN-SEL MIN
TP122 LIN3/MIN
LIN3
TP121 LOUT
TP120 ROUT
R105 open
R12 20k

CN1 12pin
RIN3
LIN3
RIN1
LIN1
LIN2
RIN2
LOUT
ROUT
LIN4
TP119 LIN4

NC NC MCKI NC PENIRQN CADT SDAT SCLT VSS2 HVDD HPR HPL MUTET NC
J8 G8 H9 G9 F8 F9 E8 E9 D8 D9 C8 C9 B9 A9

C106 0.1u
TP140 CADT TP141 SDAT TP142 SCLT
C107 10u
C108 1u
TP117 MUTET

TP116 PENIRQN

CN3 12pin
TP110 MCKI TP111 MCKO
TP112 VSS2 TP113 HVDD TP114 HPR TP115 HPL TP118 RIN4
4371_MCKI 4371_MCKO SPN SPP HVDD HPR HPL RIN4

This is a schematic diagram titled "AKD4673-A — Power Supply, I/O".

Title block:
- Title: AKD4673-A
- Document Number: Power Supply, I/O
- Size: A3
- Rev: 0
- Date: Monday, December 11, 2006
- Sheet: 2 of 5

Key components and labels:

Power supply (left section):
- T1 TA48033F (IN / GND / OUT)
- REG1 T45_RED (1)
- AGND1 T45_BK (1)
- C21 0.1u, C22 0.1u, C23 47u
- HVDD1 T45_OR (1) — L1 (short) — JP3 HVDD_SEL — HVDD; C24 47u
- AVDD1 T45_OR (1) — L2 (short) — JP4 AVDD_SEL — AVDD; C25 47u; R9 10
- DVDD1 T45_OR (1) — L3 (short) — JP5 DVDD_SEL — DVDD; C26 47u
- TVDD1 T45_OR (1) — L4 (short) — JP6 TVDD_SEL / JP7 VCC_SEL — TVDD; C27 47u
- JP1 GND
- VCC1 T45_OR (1) — L5 (short) — VCC; C28 47u
- D3V1 T45_OR (1) — L6 (short) — D3V; C29 47u
- DGND1 T45_BK (1)

Input section (center):
- J1 LIN1/RIN1 (6, 4, 3) — LIN1, RIN1
- J2 LIN (2,3,4,5 / 1) — C30 1u — R10 (short) — JP8 LIN_SEL — LIN2, LIN3, LIN4
- J3 RIN (2,3,4,5 / 1) — C31 1u — R11 (short) — JP9 RIN_SEL — RIN2, RIN3, RIN4

Output section (right):
- LOUT — C33 1u — 3.5ST — JP10 LOUT_SEL / RCA — R13 220 — J5 LOUT (1,2,3,4,5); R14 10k
- ROUT — C34 1u — 3.5ST — JP11 ROUT_SEL / RCA — R15 220 — J6 ROUT (1,2,3,4,5); R16 10k
- HPL — R17 (short) — C35 220u — JP12 HPL / RCA / HP — R18 16 — J7 HPL (1,2,3,4,5)
- J9 HP/LINE (6,4,3)
- HPR — R19 (short) — C36 220u — JP13 HPR / RCA / HP — R20 16 — J8 HPR (1,2,3,4,5)
- SPP — C37 1u — R22 10k — J10 SPK/MOUT (6,4,3); R21 (open); R23 (open); JP26 MOUT
- SPN — C38 (short)

D3V

EXT_MCLK

EXT_BICK

4114_BICK

EXT_LRCK

4114_MCKO

JP16
256fs
512fs
1024fs
384/768fs
MCKO
MKFS

JP15
MCLK
DIR
EXT

J11
EXT
R24
51
JP14
EXT

U3 74AC74
1CLR 2CLR
1D 2D
1CK 2CK
1PR 2PR
1Q 2Q
1Q 2Q
Vcc
GND
C39 0.1u

U6 74HC4040
CLK Q1
RST Q2
Q3
Q4
Q5
Q6
Q7
VD Q8
Q9
Q10
Q11
DGND Q12
C42 0.1u

JP17
64fs-384
32fs-384
64fs
32fs
BCFS

JP18
BICK_SEL
DIR
4040

JP19
THR
INV PHASE

JP20
fs-384
fs LRCK

JP21
4040
DIR LRCK_SEL

LED1
ERF
R26
1k

4114_INT0
4114_PDN

U4 74AC163
A QA
B QB
C QC
D QD
Carry
ENT
ENP Vcc
CLK
LOAD
CLR GND
C40 0.1u

MCKO

4114_LRCK

U7 74HC14
1A 4Y
1Y 4A
2A 5Y
2Y 5A
3A 6Y
3Y 6A
Vcc
GND
C43 0.1u

R25 10k
D2 HSU119

C44 0.1u

SW2 DIR
L H

U5 74HCU04
4Y
4A
5Y
5A
6Y
6A
1A
1Y
2A
2Y
3A
3Y
Vcc
GND
C41 0.1u

Title
AKD4673-A
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Document Number
CLOCK
Rev 0
Date: Monday, December 11, 2006
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AKD4673-A

DIR/DIT

U9 74AVC8T245

U10 74AVC8T245

U11 74AVC8T245

U12 74LVC07

VCC
D3V
EXT_BICK
EXT_LRCK

4371_BICK
4371_LRCK
4371_MCKO
PENIRQN-OUT
4371_SDTO

MCKO
PENIRQN
DAUX

4114_SDTO
EXT_MCLK

CAD0

4371_MCKI
4371_SDTI
CSN/CAD0
CCLK/SCL
CDTI/SDA

PENIRQN

R29 10k
R30 10k R31 10k R32 10k
R33 470 R34 470 R35 470
R36 1k

RP2 47k
RP3 47k

C57 0.1u
C58 0.1u
C59 0.1u
C60 0.1u
C61 0.1u
C62 0.1u
C63 0.1u

JP23 M/S Master / Slave
JP24 SDTI_SEL ADC / DIR
JP25 CTRL_SEL I2C / 3-WIRE

PORT3 DSP
MCLK 1 2 GND
BICK 3 4 GND
LRCK 5 6
SDTI 7 8
VCC 9 10 SDTO

PORT4 CTRL
10 9 CSN
8 7 CCLK/SCI
6 5 CDTO/SDA
4 3 CDTO/SDA(ACK)
2 1 PENIRQN
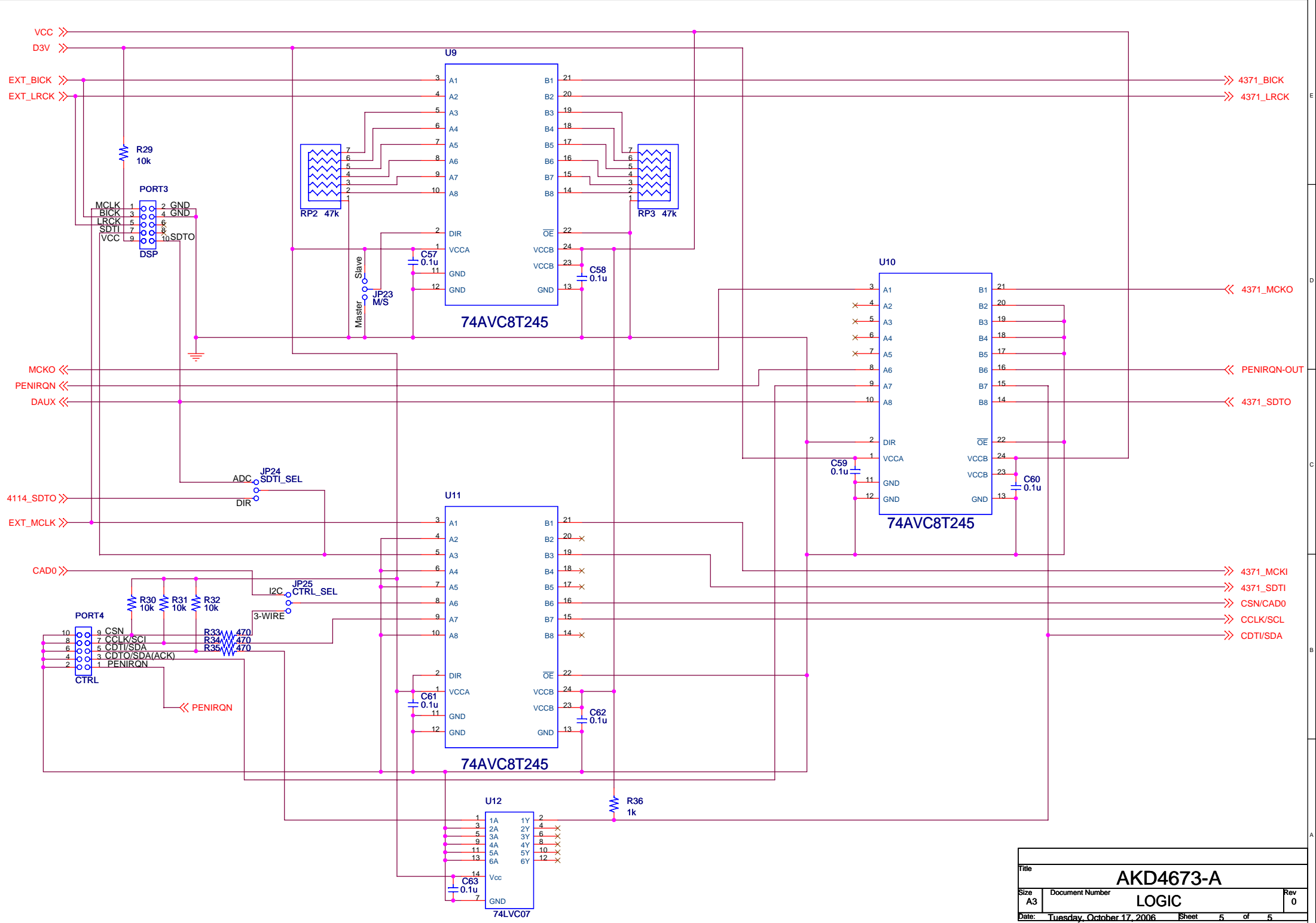
AKD4673-A-57BGA L1 PATTERN
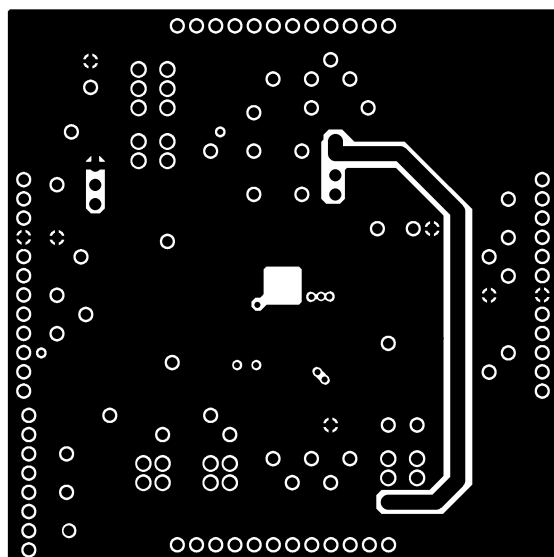
AKD4673-A-57BGA　L2　電源層
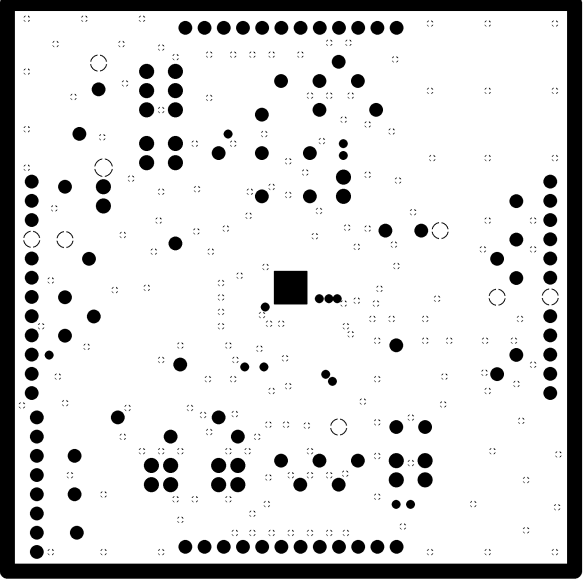
AKD4673-A-57BGA L3 GND
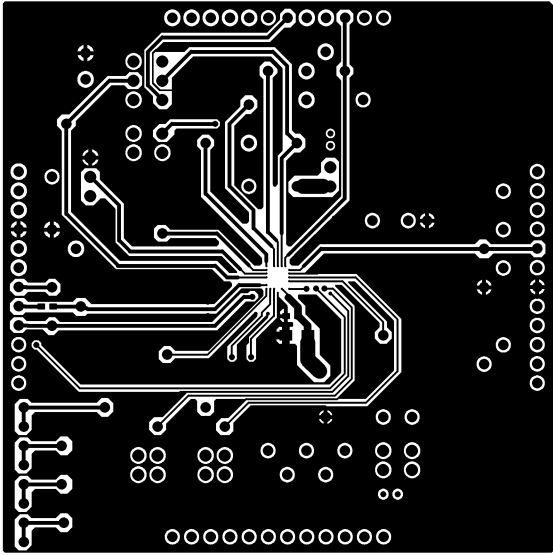
AKD4673-A-57BGA L4 PATTERN
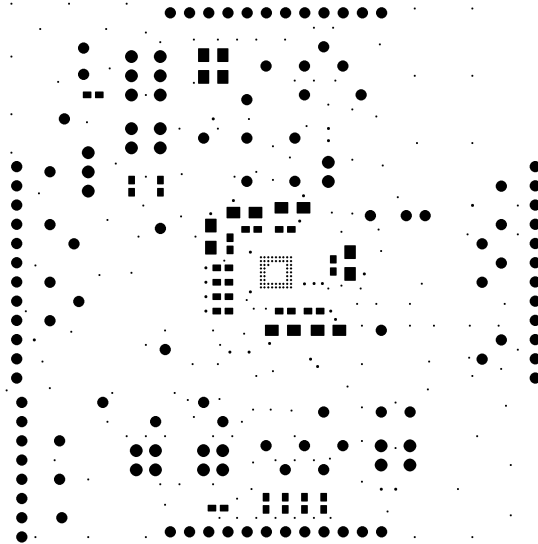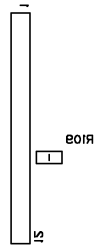
AKD4673-A-57BGA   L1 SR
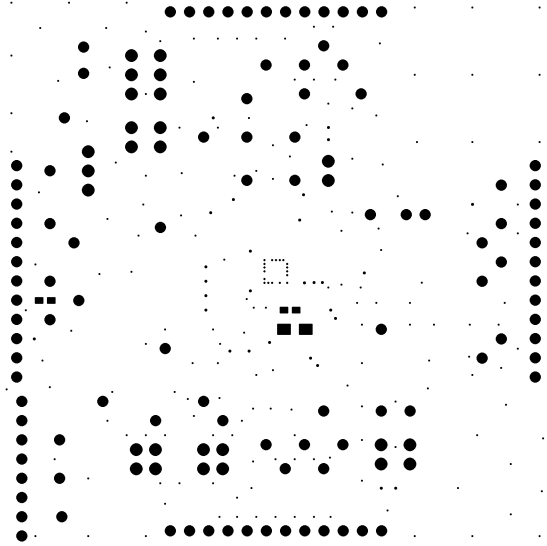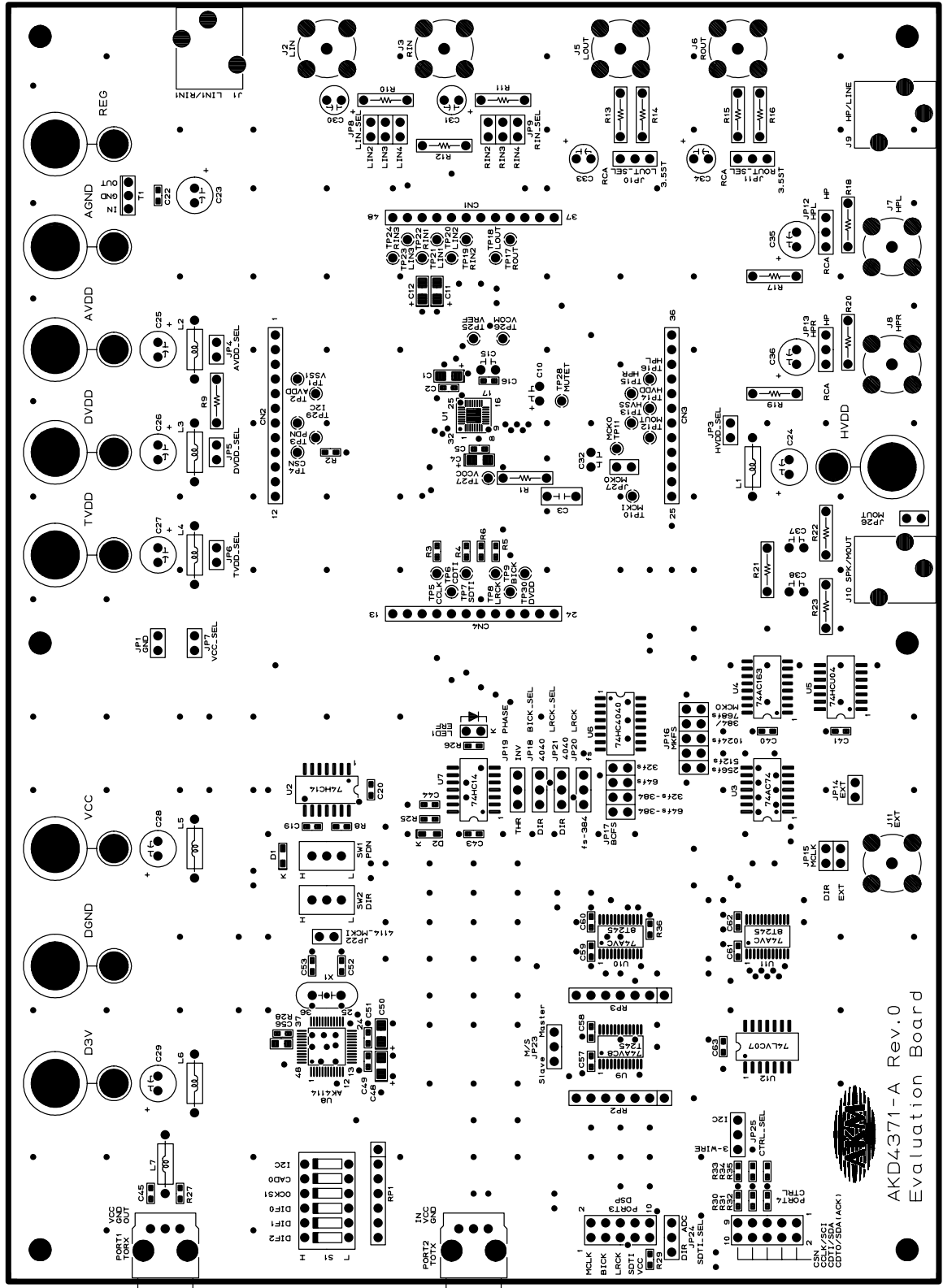
AKD4673-A-57BGA   L4 SR

AKD4673-A-57BGA   L1   SILK

48   37

1

25

38

25

R109

C103

C102

13   24
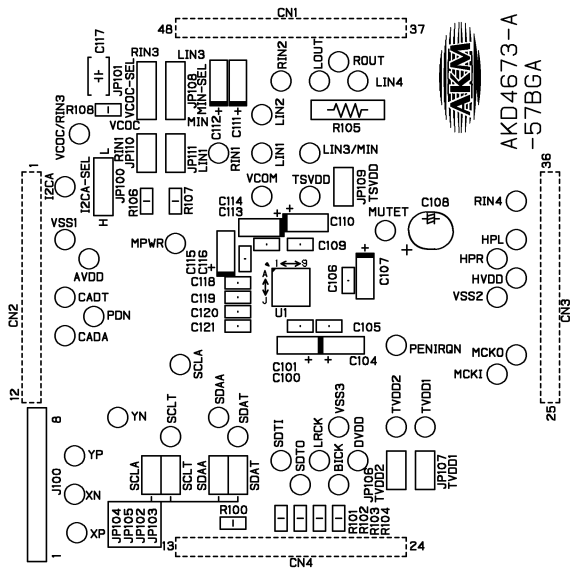
AKD4673-A-57BGA   L4   SILK
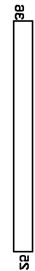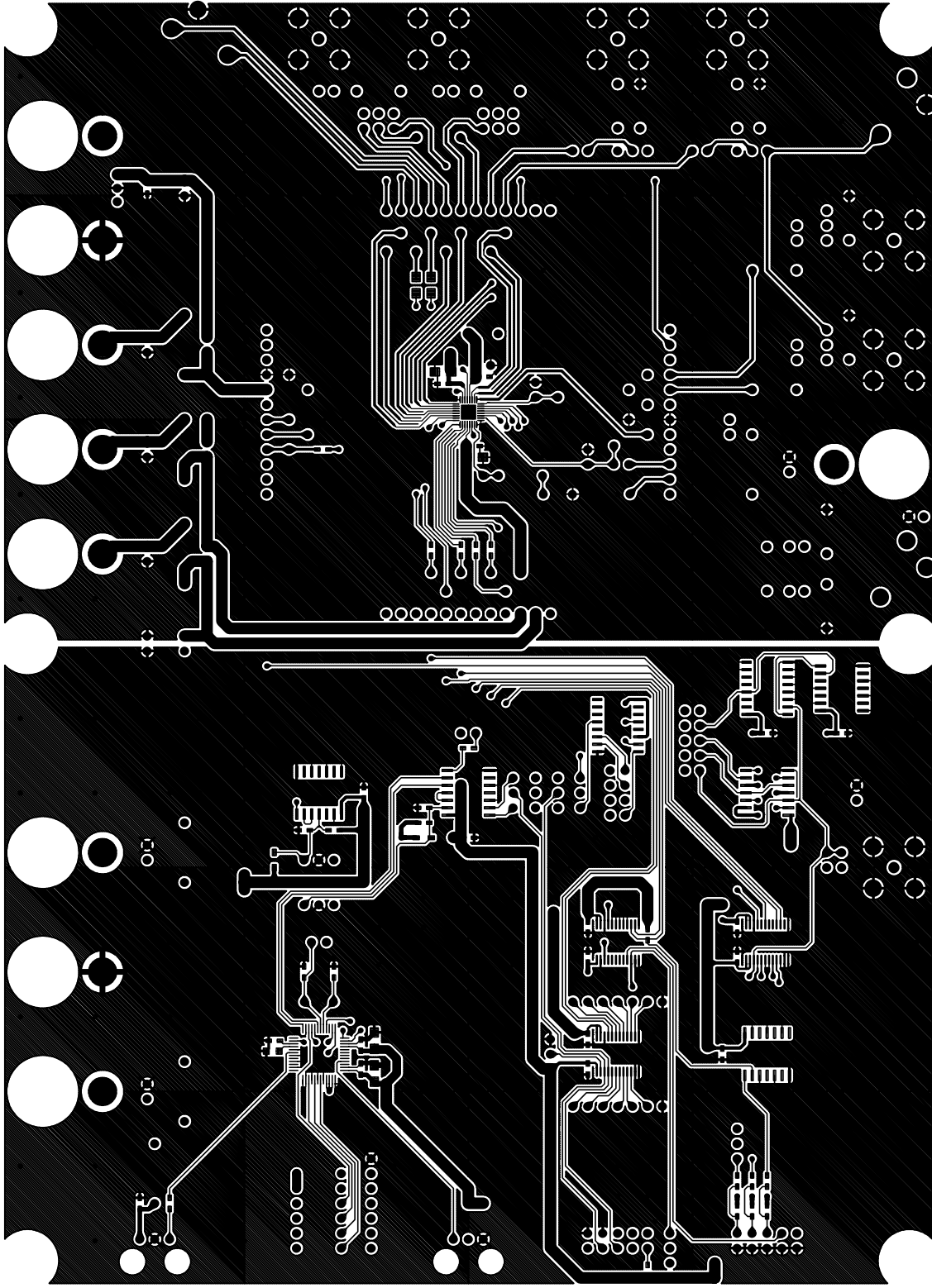
AKD4371-A Rev.0
Evaluation Board

AKD4370-A L1 SILK

AKDA370-A L2 SILK