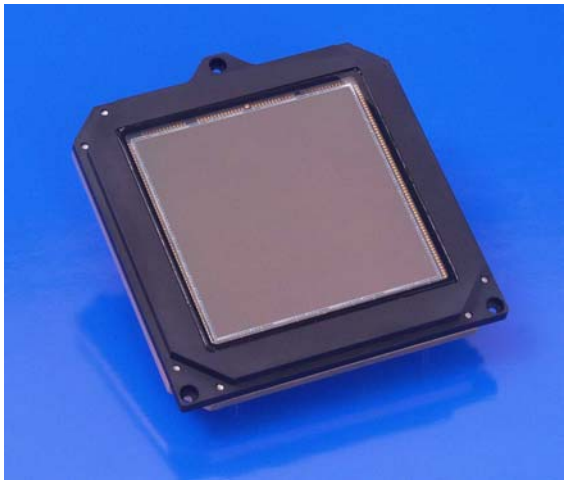
CCD595
9216 x 9216 Pixel Image Area
Full Frame CCD Image Sensor



FEATURES

- **9216 x 9216 Full Frame CCD Array**
- **8.75 μm x 8.75 μm Pixels**
- **80.64mm x 80.64mm Image Area**
- **100% Fill Factor**
- **Non Multi-Pinned Phase (MPP) Operation**
- **8 Outputs (4 on each side)**
- **Readout Noise Less Than 30 e^- at 100MHz (25MHz x 4)**

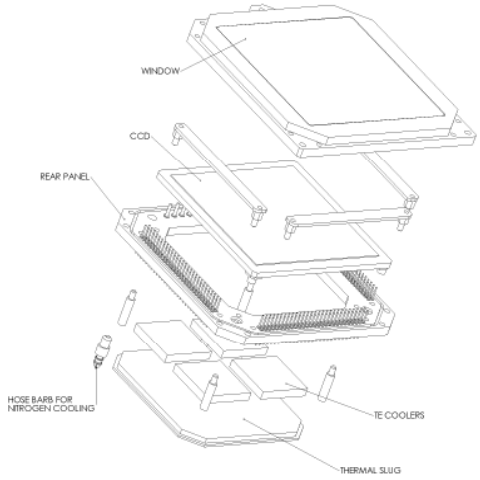
GENERAL DESCRIPTION

The CCD595 is a 9216 x 9216 active element solid state Charge Coupled Device (CCD) Full Frame sensor. The CCD is intended for advanced scientific, space, and aerial reconnaissance applications. The CCD595 is organized as an array of 9216 horizontal by 9216 vertical imaging elements. The pixel pitch is 8.75μm with a 100% fill factor. Three-phase clocking is employed in the imaging area with two-phase clocking in the serial readout registers. Image readout is performed via 4 serial registers containing 19 isolation rows between imaging and readout sections. The imaging array can be clocked unidirectional (4-output configuration) or bi-directional (8-output configuration). The imaging area segments are split in mid-array for the latter configuration. To maximize the exposure/readout cycle rate, concurrent array and serial register clocking is utilized. Fast transfer clocking between the array and serial registers is accomplished with strapped transfer gates that load each line in less than five microseconds.

DEVICE ARCHITECTURE

The output circuit architecture features eight (four active, eight optional) three-stage source follower readouts. The nominal read noise of the output amplifiers is less than 25 electrons at 25MHz. The combined data rates for 4 and 8 output configurations are 100MHz and 200MHz respectively. Internal temperature and humidity sensors are also located near the FPA for external monitoring.

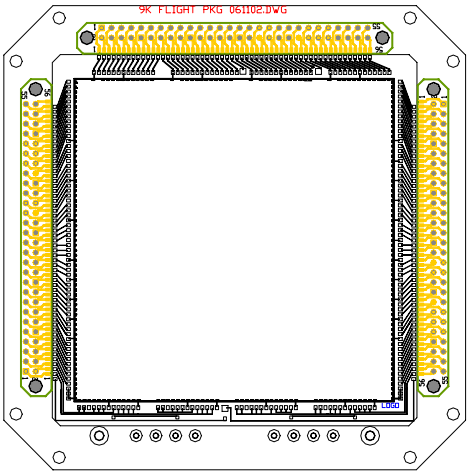
ROBUST FLIGHT PACKAGE



PACKAGE INFORMATION

The top of the package has an optical window over the CCD active area. The CCD595 is mounted in an environmentally sealed enclosure containing the CCD array with thermoelectric coolers for controlling the operating temperature of the array

Pinouts are provided on three sides for electrical connections (4-output configuration). The package base serves as the heat sink interface for thermal management. A mounting flange at the package rim is used as a Z-axis reference datum for the planarization of f the CCD focal plane with external optics.



PIN NUMBER AND PIN NAME

P1-xx	PIN NAME	P2-xx	PIN NAME	P3-xx	PIN NAME
P1-01	SUB	P2-01	TG3LB	P3-01	TEMP1P
P1-02	N.C.	P2-02	TG2LB	P3-02	BIAS2
P1-03	H2_4B	P2-03	TG1LB	P3-03	BIAS1
P1-04	H1_4B	P2-04	A1L16	P3-04	A1R1
P1-05	SW4	P2-05	A2L16	P3-05	A2R1
P1-06	RG4	P2-06	A3L16	P3-06	A3R1
P1-07	SUB	P2-07	A1L15	P3-07	A1R2
P1-08	OTG4	P2-08	A2L15	P3-08	A2R2
P1-09	RD4	P2-09	A3L15	P3-09	A3R2
P1-10	OD4	P2-10	A1L14	P3-10	A1R3
P1-11	OS4	P2-11	A2L14	P3-11	A2R3
P1-12	VSRC4	P2-12	A3L14	P3-12	A3R3
P1-13	VGT4	P2-13	A1L13	P3-13	A1R4
P1-14	SUB	P2-14	A2L13	P3-14	A2R4
P1-15	N.C.	P2-15	A3L13	P3-15	A3R4
P1-16	H2_3B	P2-16	A1L12	P3-16	A1R5
P1-17	H1_3B	P2-17	A2L12	P3-17	A2R5
P1-18	SW3	P2-18	A3L12	P3-18	A3R5
P1-19	RG3	P2-19	SUB	P3-19	SUB
P1-20	SUB	P2-20	A1L11	P3-20	A1R6
P1-21	OTG3	P2-21	A2L11	P3-21	A2R6
P1-22	RD3	P2-22	A3L11	P3-22	A3R6
P1-23	OD3	P2-23	A1L10	P3-23	A1R7
P1-24	OS3	P2-24	A2L10	P3-24	A2R7
P1-25	VSRC3	P2-25	A3L10	P3-25	A3R7
P1-26	VGT3	P2-26	A1L9	P3-26	A1R8
P1-27	TEMP2P	P2-27	A2L9	P3-27	A2R8
P1-28	TEMP2M	P2-28	A3L9	P3-28	A3R8
P1-29	SUB	P2-29	A3L8	P3-29	A3R9
P1-30	N.C.	P2-30	A2L8	P3-30	A2R9
P1-31	H2_2B	P2-31	A1L8	P3-31	A1R9
P1-32	H1_2B	P2-32	A3L7	P3-32	A3R10
P1-33	SW2	P2-33	A2L7	P3-33	A2R10
P1-34	RG2	P2-34	A1L7	P3-34	A1R10
P1-35	SUB	P2-35	A3L6	P3-35	A3R11
P1-36	OTG2	P2-36	A2L6	P3-36	A2R11
P1-37	RD2	P2-37	A1L6	P3-37	A1R11
P1-38	OD2	P2-38	SUB	P3-38	SUB
P1-39	OS2	P2-39	A3L5	P3-39	A3R12
P1-40	VSRC2	P2-40	A2L5	P3-40	A2R12
P1-41	VGT2	P2-41	A1L5	P3-41	A1R12
P1-42	HUM1	P2-42	A3L4	P3-42	A3R13
P1-43	HUM2	P2-43	A2L4	P3-43	A2R13
P1-44	SUB	P2-44	A1L4	P3-44	A1R13
P1-45	N.C.	P2-45	A3L3	P3-45	A3R14
P1-46	H2_1B	P2-46	A2L3	P3-46	A2R14
P1-47	H1_1B	P2-47	A1L3	P3-47	A1R14
P1-48	SW1	P2-48	A3L2	P3-48	A3R15
P1-49	RG1	P2-49	A2L2	P3-49	A2R15
P1-50	SUB	P2-50	A1L2	P3-50	A1R15
P1-51	OTG1	P2-51	A3L1	P3-51	A3R16
P1-52	RD1	P2-52	A2L1	P3-52	A2R16
P1-53	OD1	P2-53	A1L1	P3-53	A1R16
P1-54	OS1	P2-54	BIAS2	P3-54	TG1RB
P1-55	VSRC1	P2-55	BIAS1	P3-55	TG2RB
P1-56	VGT1	P2-56	TEMP1M	P3-56	TG3RB

DEVICE ARCHITECTURE

Array Size	9216 x 9216	Full Frame
Pixel Size	8.75-um x 8.75-um	
Image Format	80.64 x 80.64	Mm
Number of Outputs	8 (4 Upper, 4 Lower)	Current Configuration Wired for 4 outputs
Pixel Output Rate	100MHz (25MHz per output)	
Number of Phases	3 + 3 (TG clocks)	
Number of Prescan Pixels	3	Pixels/line
Number of Overscan Lines	19	Top and Bottom
Total Number of Lines	9216	
Number of Phases	2	Horizontal
Pixel Rate per Output	25MHz	Typical

DC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	RANGE MIN	RANGE NOM	RANGE MAX	UNIT	REMARKS
V_{DD}	DC Supply Voltage	18.0	20.0	23.0	V	
V_{RD}	Reset Drain Voltage	14.0	17.0	20.0	V	
V_{OG}	Output Gate Voltage		4.0			
V_{SS}	Substrate Ground		0.0		V	
V_{odc}	Output DC Level	VRD-5		VRD-4	V	
Z	Suggested Load Resistor	0.8	1.0	1.8	K ohms	

TYPICAL CLOCK VOLTAGES

SYMBOL	PARAMETER		HIGH	LOW	UNIT	REMARKS
$V\phi_{H(1,2),}$	Horizontal Transport Clock Voh Max-Min		+7.5	-7.5	V	+4.5, -0.5 Typical
ϕSG	Horizontal Transport Clock Voh Max-Min		+6	-2	V	
$V\phi V_{(1,2,3)}$	Vertical Transport Clocks		+8.0	-12.0	V	+5, -11 V Typical
$V\phi R$	Reset Gate Clock		+6.0	+1.0	V	+2.0 +8.0 V Typical
$V\phi_{VTG\ (2,3)}$	Array Transfer Gate Clock		+8.0	-12.0	V	+5, -11 Typical
$C\phi V_{(1,2,3)}$	Vertical Array Gates Cap. (per ϕV)	A_1 A_2 A_3	47 86 109	30 38 31	nF	Min @ +10V Max @ -10V
$C\phi VTG_{2,3}$	Array Transfer Gate Cap. (per pin)	TG_2 TG_3	200 200	150 150	pF	Min @ +10V Max @ -10V
$C\phi H_{(1,2)}$	Horizontal Transfer Gate Cap. (per ϕ H)	S_1 S_2	65 76		PF	Min @ +10V (per output) Max @ -10V (per output)

Note 1: ϕH = 400 pF, ϕV = 60,000 pF. All ϕH clock rise and fall times should be > 10 ns.

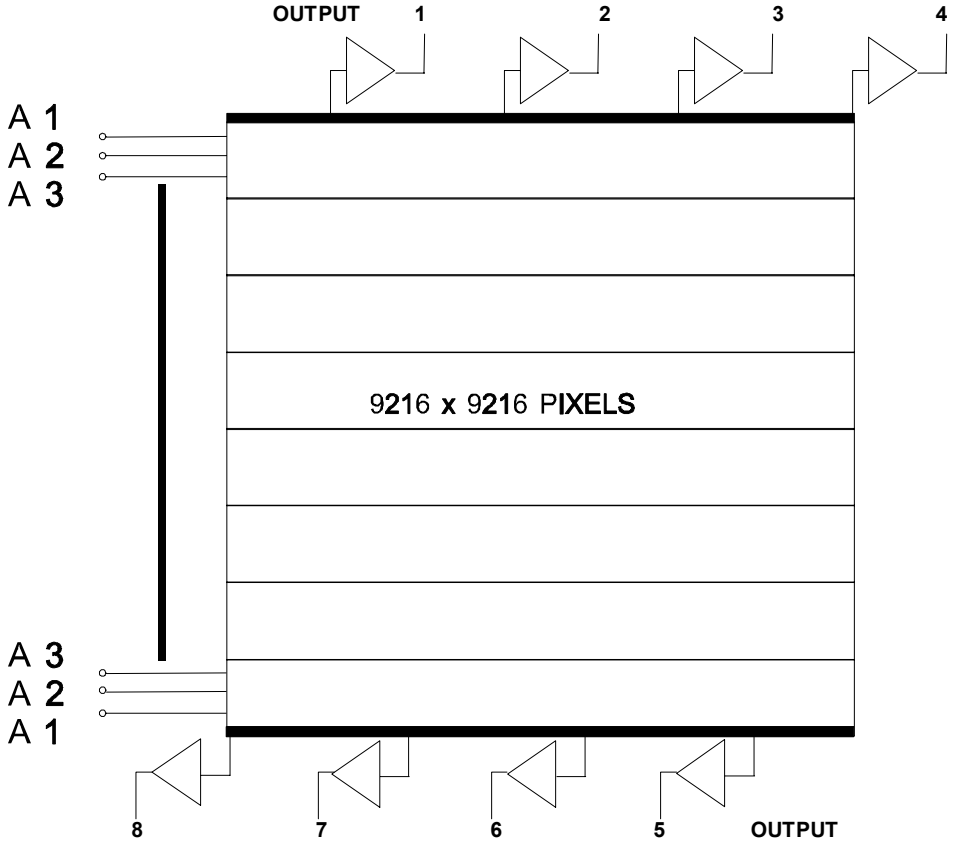
PERFORMANCE SPECIFICATIONS

SYMBOL	PARAMETER	RANGE MIN	RANGE NOM	RANGE MAX	UNIT	REMARKS
V_{sat}	Saturation Output Voltage	350	600	750	mV	Note 1
Q_{sat}	Full Well Capacity (98% of Pixels)	70,000			e-	Note 1
S_V	Output Amp Sensitivity	5	9	11	μV/e-	
H_{sat}	Horizontal Register Capacity		100,000		e-	
PRNU	Photo Response Non-Uniformity, Peak-to-Peak		$\pm$10		$\%V_{SAT}$	Note 2
DSNU	Dark Signal Non-Uniformity (RMS)			5.0	mV	Note 3
DC	Average Dark Current			0.5	nA/cm^2	Note 3
QE_A	Average Quantum Efficiency (550 – 800μm)		0.35		%	
MTF	MTF at Nyquist		0.50		%	Note 4
V_{cte}	Vertical Transfer Efficiency	0.999995				Per Transfer (each phase) Note 2
H_{cte}	Horizontal Charge Transfer Efficiency	0.99995				Per Transfer (each phase) Note 2
NE	Total Read Noise Electrons		20	30	e-rms	Less Shot Noise Note 6
$fMAX_H$	H Clock Frequency		25		MHz	
PD	Power Dissipation On Chip		2.9		W	At 25MHz each register

Note 1: Minimum output voltage and/or well capacity is achieved operating in standard test condition mode and is the level above which saturation non-linearity of 50% from best straight line fit occurs.
Note 2: Measured at approximately 50% V_{sat}.
Note 3: Value shown is for 15°C.
Note 4: Measured at the format center with 2854K tungsten source and Schott OG550 filter, 3mm thick.
Note 5: Standard test conditions are non-MPP clocks and DC operating voltages with 25MHz serial output rate/port.
Note 6: Measured in dark with correlated double sampling of amplifier output signal.

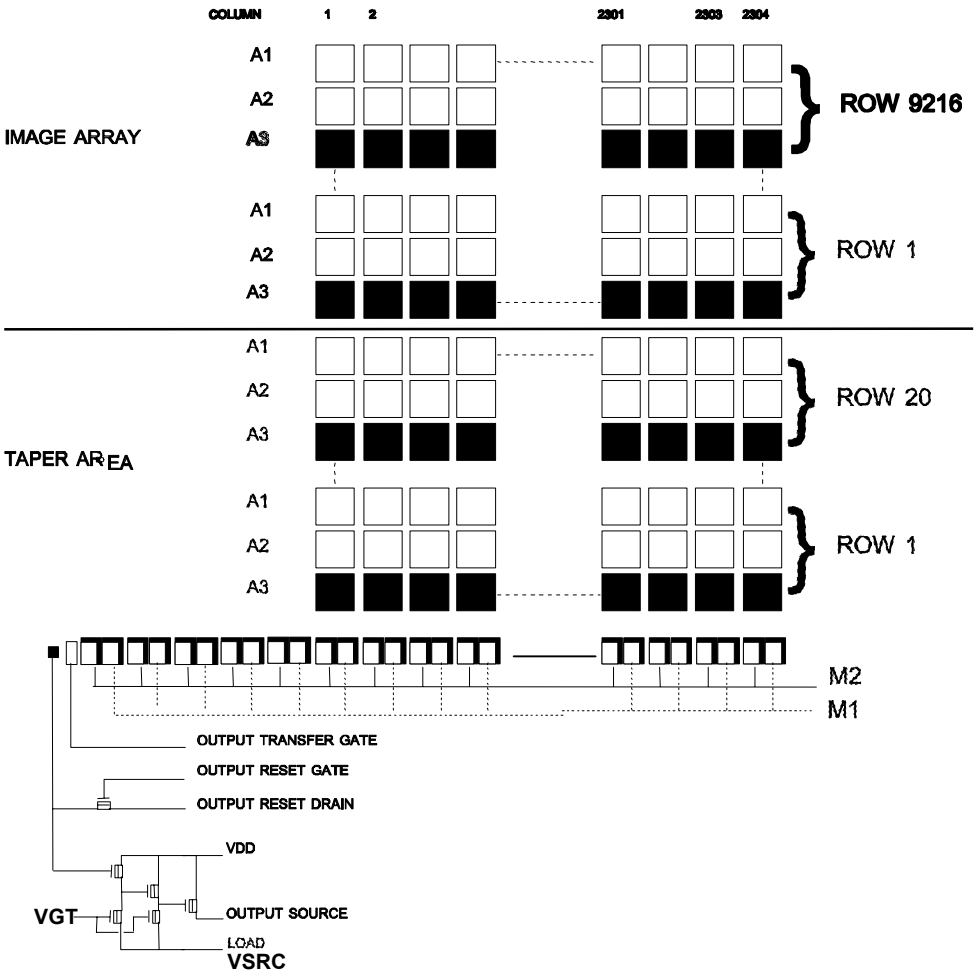
READOUT AMPLIFIER CONFIGURATION

The CCD595 readout structure is shown in the diagram below. Array to serial register transfer gates are not shown.

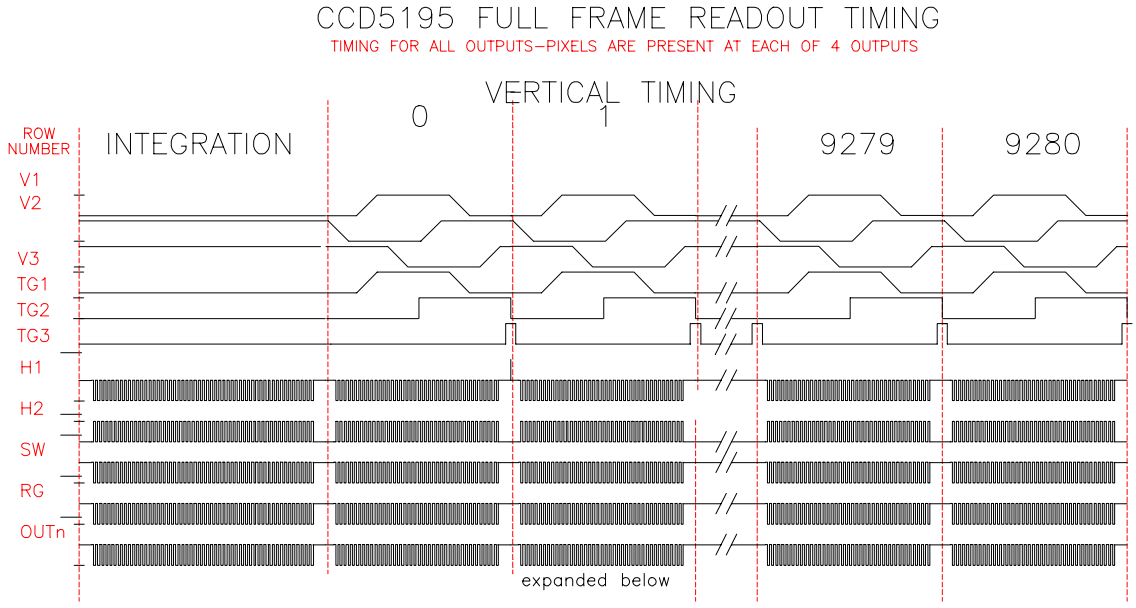


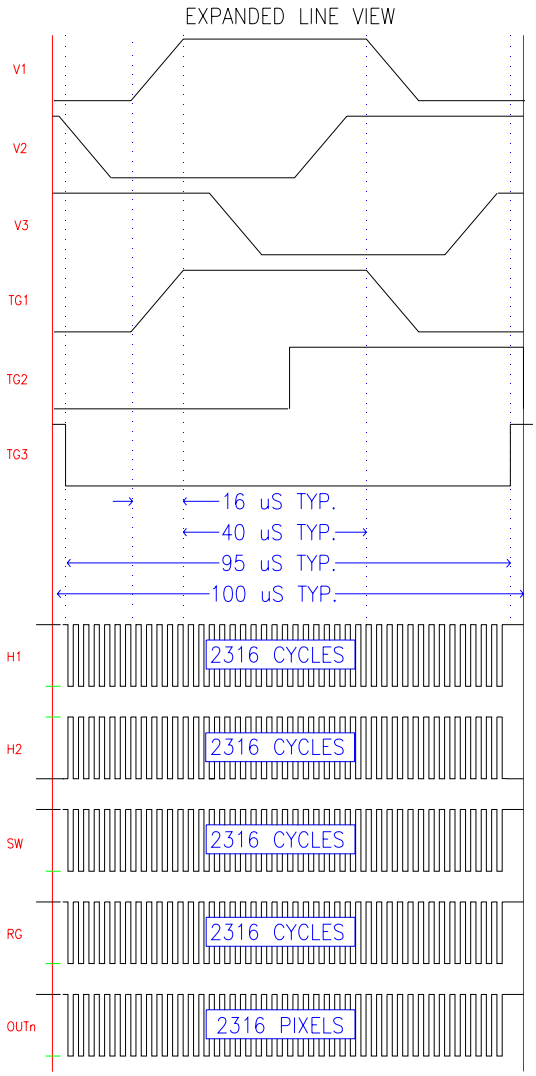
SINGLE OUTPUT SECTION DIAGRAM

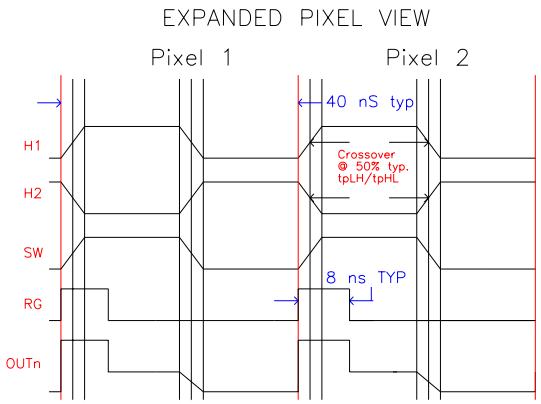
A single section of the CCD595 is shown below. The 20 taper rows include a single row of transfer gates nearest the serial readout register.



TIMING




EXPANDED LINE VIEW
V1
V2
V3
TG1
TG2
TG3
16 uS TYP.
40 uS TYP.
95 uS TYP.
100 uS TYP.
H1
2316 CYCLES
H2
2316 CYCLES
SW
2316 CYCLES
RG
2316 CYCLES
OUTn
2316 PIXELS


EXPANDED PIXEL VIEW
Pixel 1
Pixel 2
40 nS typ
Crossover
@ 50% typ.
tpLH/tpHL
8 ns TYP
H1
H2
SW
RG
OUTn

COSMETIC SPECIFICATIONS

Parameters	Grade 1	Grade 2	Grade 3	Units	Notes
Number of Outputs	4	4	≥ 2	Output	
Column Defects	≤ 10	≤ 50	≤ 250	Column	
Maximum Defective Column Width	≤ 2	≤ 10	≤ 50	Column	
Defective Column Separation	≥ 2	≥ 2	≥ 2	Column	
Single Pixels	100,000	200,000	400,000	Pixel	Excluding defective columns & clusters
Cluster Defects					
Small	≤ 400	≤ 900	≥ 900	Cluster	Excluding defective columns & single pixels
Medium	≤ 10	≤ 50	≤ 250	Cluster	Excluding defective columns & single pixels
Large	0	≤ 2	≤ 10	Cluster	Excluding defective columns & single pixels
Cluster Defect Separation	≥ 2	≥ 2	≥ 2	Rows/Columns	

Test Conditions:
Device temperature 25°C
Readout mode 1 x 1
Data Rate 25Mhz per output

Definitions:

Single Pixels	Pixels which photoresponse deviates more than ± 10% of the minimum vertical pixel well at 50% of V_{sat}
Column Defects	More than 25 contiguous blemished pixels in a column
Defective Column Width	Number of adjacent defective columns
Cluster Defects	
Small	A grouping of 2 to 11 adjacent point defects
Medium	A grouping of 12 to 25 adjacent point defects
Large	A grouping of 26 to 1000 adjacent point defetcs
Excluded Regions	The outer 5 rows and columns are excluded

WARRANTY
Within twelve months of delivery to the end customer, Fairchild Imaging will repair or replace, at our option, any Fairchild Imaging camera product if any part is found to be defective in materials or workmanship. Contact Customer Service for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

This product is designed, manufactured and distributed utilizing the ISO 9000:2000 Business Management System.

CERTIFICATION
Fairchild Imaging certifies that all products are carefully inspected and tested at the factory prior to shipment and will meet all requirements of the specifications under which it is furnished.

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