KING BILLION ELECTRONICS CO., LTD
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HF88S05
SRAM Series

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1. General Description

The HF88S05 is a command mode SRAM device. It features dual (parallel and serial) command access modes. Multiple device arrays can be accessed with only minimal additional device select pin. Simple Exclusive OR checksum provides error detection during data transfer between MCU and the device. The interface logic and protocol include setting up the starting address for data transfer, writing data into RAM, as well as read it back for verification, and error checking by Exclusive OR checksum. It can be used for Read/Write memory extension for all KB's MCUs.

Chip Select pins allows array of HF88S05 devices are used simultaneously for both parallel and serial transfer mode. In the serial mode, the HF88S05 is connected in daisy chain configuration to minimize the I/O pins required to use multi-chip array, while in parallel mode, the devices share most of the control pins and data bus except the chip select pins.

2. Features

✓ Dual (parallel and serial) command access modes.

✓ Address automatically increment with each Read/Write data access.

✓ Exclusive or checksum error detection

✓ Multiple chip array is allowed with easy addressing logic

✓ Read access voltage range 2.7V ~ 3.6V

✓ Organization -- Memory Cell Array: 64K × 8

✓ Package – Dice form

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3. Pin Description

```
        1   ┌─────────────┐   18
     ──────┤ P_SN    VDD ├──────
        2   │             │   17
     ──────┤ VSS     CS1 ├──────
        3   │             │   16
     ──────┤ CS0N    SDO ├──────
        4   │             │   15
     ──────┤ D_CN    SDI ├──────
        5   │             │   14
     ──────┤ R_WN   SCLK ├──────
        6   │             │   13
     ──────┤ D0       D7 ├──────
        7   │             │   12
     ──────┤ D1       D6 ├──────
        8   │             │   11
     ──────┤ D2       D5 ├──────
        9   │             │   10
     ──────┤ D3       D4 ├──────
            └─────────────┘
              HF88S05
```
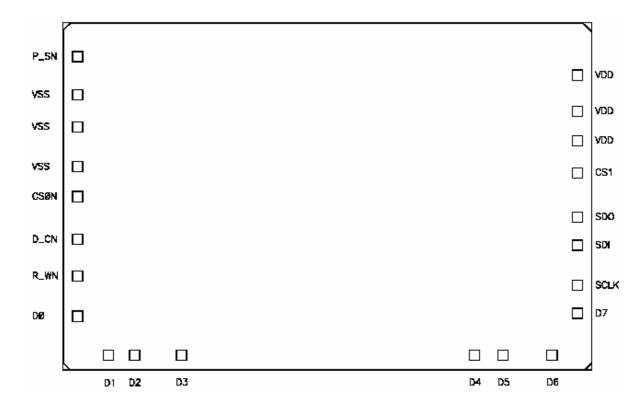
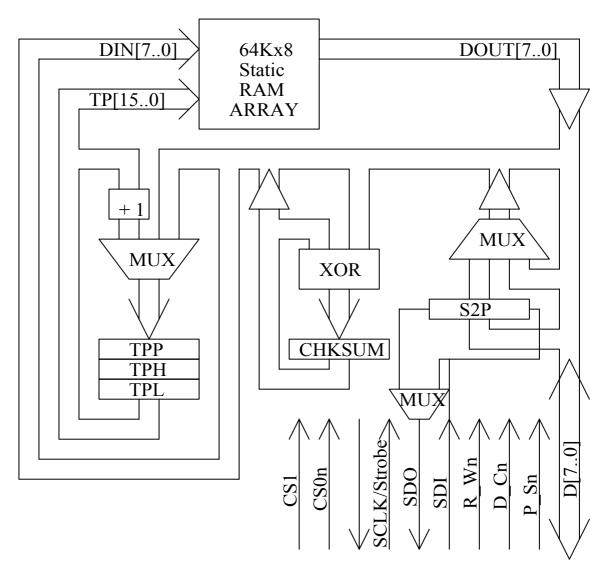| Symbol	I/O	Description
P_Sn	I	Input to select either parallel (when '1') or serial (when '0') interface is used for transferring data.
VSS	I	Negative power supply of the device
CS0n	I	CS0n is active low chip select input pin. The device is selected when CS1 is high and CS0n is low simultaneously. Otherwise, it is deselected.
D_Cn	I	Input to select either the SRAM or Registers (TPP, TPH, TPL, Mode or Checksum) operations.
R_Wn	I	Input to select either a Read operation (when '1') or a write operation (when '0') is to be performed.
D0 ~ D7	I/O	Bi-directional data bus for parallel transfer mode.
SCLK/ Strobe	I	This pin is shared between parallel and serial modes. In serial mode, this pin is Serial Clock SCLK for transferring the data from/to SDI/SDO. In parallel mode, it is the strobe signal used to write the registers and SRAM as well as read the checksum and contents of SRAM. This pin is equipped with Schmidt type input structure to prevent the input from chattering due to slow rising clock source transition.
SDI	I	Serial Data Input for writing to either Registers or SRAM.
SDO	O	Serial Data Output for reading data from either Checksum Register or SRAM.
CS1	I	CS1 is active high chip select input. The device is selected when CS1 is high and CS0n is low simultaneously. Otherwise, it is deselected.
VDD	I	Positive power supply of the device

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4. Pad Diagram & Coordinates

Pin Number	Pin Name	X Coordinate	Y Coordinate	Pin Number	Pin Name	X Coordinate	Y Coordinate
1	P_SN	-1970.5	1260.4	12	D4	1150.32	-1088.97
2	VSS	-1970.5	960.41	13	D5	1375.93	-1088.97
3	VSS	-1970.5	707.54	14	D6	1762.16	-1088.97
4	VSS	-1970.5	394.22	15	D7	1964.53	-759.28
5	CS0N	-1970.5	159.23	16	SCLK	1964.53	-538.44
6	D_CN	-1970.5	-177.15	17	SDI	1964.53	-221.71
7	R_WN	-1970.5	-465.52	18	SDO	1964.53	-0.91
8	D0	-1970.5	-780.53	19	CS1	1964.53	347.7
9	D1	-1725.02	-1088.97	20	VDD	1964.53	600.92
10	D2	-1521.22	-1088.97	21	VDD	1964.53	831.74
11	D3	-1152.68	-1088.97	22	VDD	1964.53	1114.36

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5. Function Block Diagram

Several registers are used in the interface logic. The functions of the registers are described below and their initial values are as indicated in the following table.

Register	Type	Description	Initial Value
TPL	W	Address register 0 for A7 ~ A0	"--------"
TPH	W	Address register 1 for A15 ~ A8	"--------"
TPP	W	Address register 2 for A23 ~ A16	"--------"
Checksum	R	XOR checksum of data	"--------"

The Table Pointer register keeps the address of SRAM being written to or read from. It will automatically increment by one with each read/write access, but remains unchanged when writing command or reading checksum.

The Checksum Register keeps the Exclusive OR checksum of the data bytes as they are written to/read from SRAM. The Checksum register cannot be written but it is cleared by any access to the TPL, TPH

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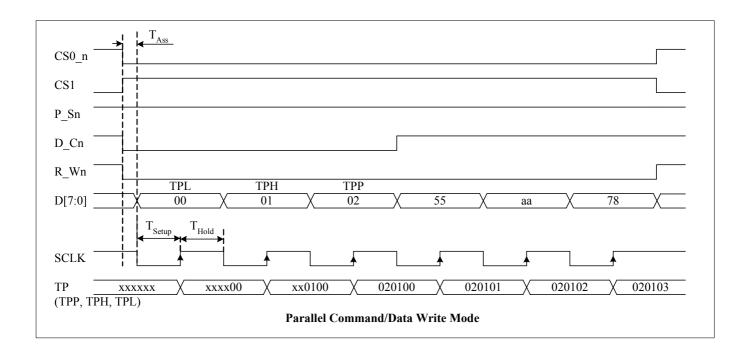
and TPP registers.

6. Parallel Mode

When in parallel mode, an 8-bit data bus D[7..0] are used to transfer information between MCU and SRAM. The advantage of parallel transfer mode is that higher speed can be achieved. To operate in parallel mode, the P_Sn pin should be driven with high level voltage.

6.1. Parallel Write Command Mode

Loading of Addresses and Mode Register in parallel mode are by asserting the Strobe (going low and then high) in write command mode (both R_Wn and D_Cn are low), which will also clear the CHKSUM register at the same time. After the previous data transfer or when the device is just selected (CS1 is high and CS0n is low), the command data will be written to registers in the order of TPL, TPH, TPP, then Mode, TPL… So when unsure, a dummy data read or deselect and select the device again will reset the register select.

The timing chart below exemplifies when original TP is unknown, then 0x00, 0x01, 0x02 addresses were written sequentially to TPL, TPH, and then TPP, the TP becomes 0x020100h.

Parallel Command/Data Write Mode
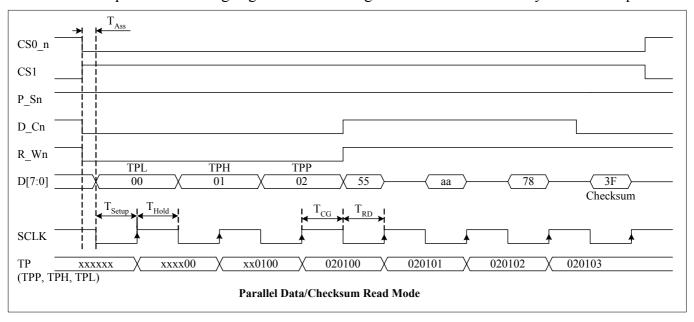
6.2. Parallel Write Data Mode

To write data to SRAM in parallel mode, assert Strobe in Data Write Mode (D_Cn @ Vih and R_Wn at Vil). The checksum register will be updated, and the TP register will be incremented at the rising edge of Strobe signal.

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6.3. Parallel Read Data Mode

To Read from SRAM in parallel mode, assert the Strobe in Read Data mode (R_Wn at high and D_Cn low).   The data will appear on the Data bus after proper access time.   The TP will increment and Checksum will update at the rising edge of Strobe.   Register select will be reset by Read Data operation.

Parallel Data/Checksum Read Mode

6.4. Parallel Checksum Read Mode

To read the checksum result from previous data transfer (either from SRAM or to SRAM), assert the Strobe signal in Read Command mode (R_Wn is high and D_Cn low).

7. Serial Mode

The serial interface is preferable to parallel interface in applications where I/O pins are limited.   The interface logic circuit is basically the same as the parallel mode except that an internal shift register and bit counter are used to facilitate transferring serial data from/to external MCU.

Multiple devices array can also be used in serial mode.   The chip array is connected in daisy chain manner.   The MCU's serial data output pin drives the SDI pin of the first device.   The SDO pin of the device then, in turn, drives the SDI pin of the next device in the chain. The SDO pin of the last device then connects back to the MCU's SDI pin to complete the loop.

There could be only one active device in the array at one time, while the other device must be deselected.

7.1. Bi-directional Synchronous Serial Data Interface

The Serial interface is a Bi-directional Synchronous Serial Interface.   The Serial Data can be written to Registers (such as TPL, TPH, TPP registers) as well as SRAM through the serial interface.   The

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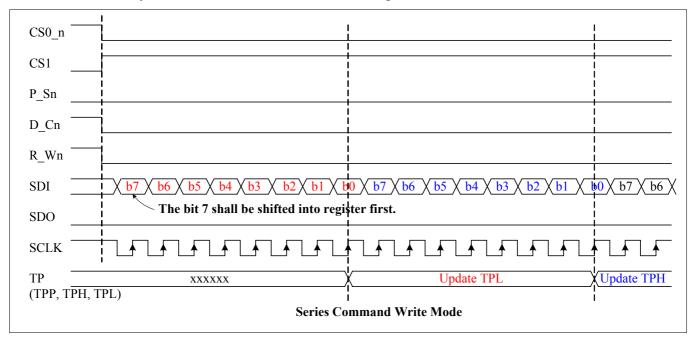Checksum and SRAM contents can also be read through Serial Interface, too.

The Serial Data Input SDI pin is connected to LSB of internal shift register.   With each rising edge of SCLK pin, the SDI input is shifted into the shift register.   At the eighth rising edge of SCLK, the content of shift Register is transferred from/to registers or SRAM depending on the status of D_Cn and R_Wn.

If R_Wn is at "high" state at the eighth rising edge of SCLK then either the contents of Checksum Register (if D_Cn is "low") or SRAM been addressed (if D_Cn is "high") will be latched into the internal shift register.   Then the contents of Shift Register can be shifted out with the next eight rising edges of SCLK.

So one thing important should be noted here when using the Serial Data Interface to read checksum register or SRAM data is that one dummy read should be performed before the real data can be shifted out from SDO pin.

7.2. Serial Command Write Mode

The sequence of setting up addresses for data transfer is similar to the parallel mode.   The register pointer will be reset by accesses to SRAM data in the same way as the parallel mode does.   So immediately after completion of previous data transfers or when the device is just selected, the command writes will be made to TPL, TPH then TPP registers and then wrap around.   If unsure any time during the transfer, a dummy data read can be made to reset the register select.

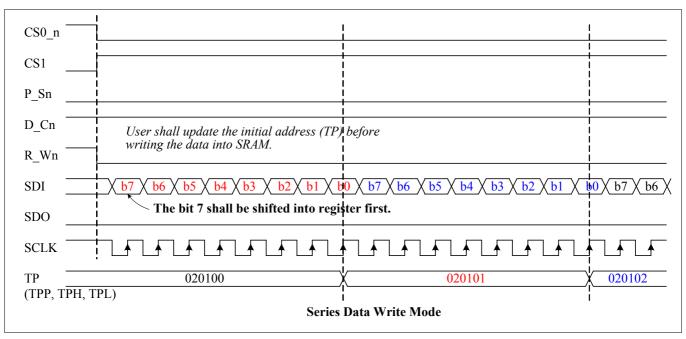**Series Command Write Mode**

7.3. Serial Data Write Mode

With each rising edge of SCLK signal in the serial data write mode (P_Sn @ logic '0', R_Wn @ logic '0', and D_Cn @ logic '1'), the Data on the SDI pin will be shifted into the internal shift register. The content

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of less significant 7 Bits of the internal shift register along with SDI pin will be transfer to SRAM at the eighth rising edge of SCLK. The checksum register will be updated, and the TP register will be incremented. The status of R_Wn, D_Cn and SDI must be held steady in the mean time.

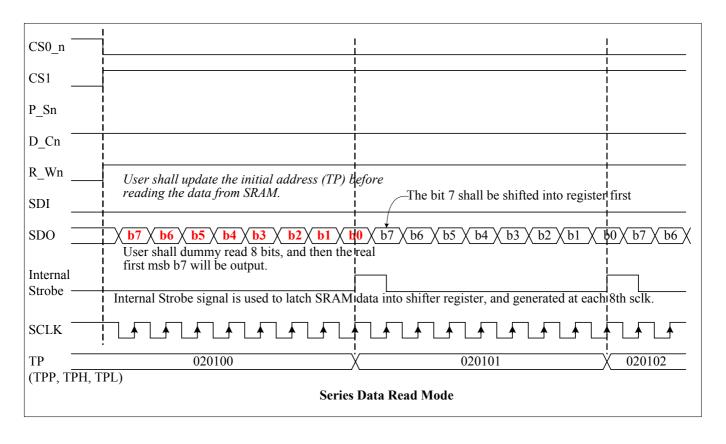**Series Data Write Mode**

7.4. Serial Data Read Mode

If both R_Wn, and D_Cn are at high level at the eighth rising edge of SCLK then the contents of SRAM been addressed will be latched into the internal shift register. Then the contents of shift register can be shifted out with the next eight rising edges of SCLK.

So one thing important should be noted here when using the Serial Data Interface to read SRAM data is that one dummy read should be performed before the real data can be shifted out from SDO pin.

User shall update the initial address (TP) before reading the data from SRAM.

The bit 7 shall be shifted into register first

User shall dummy read 8 bits, and then the real first msb b7 will be output.

Internal Strobe signal is used to latch SRAM data into shifter register, and generated at each 8th sclk.

Series Data Read Mode

7.5. Serial Command Read Mode

Reading checksum in serial mode is similar to Read data mode except that the D_Cn is at low level instead of high.

8. Power consideration

In order to conserve power consumed by the device, the static power consumption by SRAM sense amplifier need to be minimized. Since the sense amplifier is on whenever the device is selected and Strobe/SCLK is asserted low in Data Read Mode. Therefore the way to save power is to minimize the duty of the overall Strobe/SCLK signal to an extent that it is just long enough to satisfy the access time so that the static power consumption can be lower.

9. Absolute Maximum Rating

Items	Symbol	Rating	Condition
Supply Voltage	V_{DD}	-0.3 to 4.0 V	
Input Voltage	V_{IN}	-0.3 to Vdd+0.3 V	
Operating Temperature	T_{OPR}	-0 to 70 °C	
Storage Temperature	T_{STR}	-55 to 125 °C	

10. AC Electrical Characteristics

Item	Symbol	VCC=3.0V		Unit
		Min	**Max**	
Chip Asserted Time	T_{Ass}	100	-	ns
Data Setup Time	T_{Setup}	200	-	ns
Data Hold Time	T_{Hold}	150	-	ns
Pre-charge Time	T_{CG}	120	-	ns
Data Ready Time	T_{RD}	250	-	ns

11. Electrical Characteristics

(V_{DD} = 3.0 V, T_{OPR} = 25°C unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max	Unit	Condition
Supply Voltage	V_{DD}	2.7	-	3.6	V	
Operating Current	I_{DD}	-	TBD	-	mA	No load
Standby Current	I_{DD}	-	10	-	μA	No load
Input voltage	V_{IH}	0.7	-	1	V_{DD}	VDD = 4V ~ 6V
	V_{IL}	0	-	0.3		
Input current leakage	I_{IL}	-	-	+/- 10	μA	

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12. Application Circuit

The application circuit diagram shows one of the KB's MCU uses two HF88S05 as expansion RAMs. Please note that the SDO pin of the first device drive SDI pin of the second device and only one device select pin DEV1 is used to select between one of the two devices. The P_Sn pins are tied to ground operate at serial mode.

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13. Update History

Version	Date	Revision Description
V1.0	12/17/03	Modify the SRAM access timing diagram.