

HYS72T128001HR-5-A HYS72T256000HR-[3S/3.7/5]-A

*240-Pin Registered DDR SDRAM Modules
RDIMM
DDR2 SDRAM
RoHS Compliant*



Internet Data Sheet

Rev. 1.4

HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

| | |
|--|---|
| HYS72T128001HR-5-A, HYS72T256000HR-[3S/3.7/5]-A | |
| Revision History: 2007-02, Rev. 1.4 | |
| Page | Subjects (major changes since last revision) |
| All | Adapted internet edition |
| All | Added HYS72T256000HR-3S-A: Updated Ordering Information, Block Diagrams, I_{DD} Currents, SPD Codes |
| Previous Revision: Rev. 1.31, 2006-09 | |
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| Previous Revision: Rev. 1.3, 2006-01 | |
| | Added HYS72T128001HR-5-A: Updated Ordering Information, Block Diagrams, I_{DD} Currents, SPD Codes and Package Outlines accordingly |
| 5 | Added High Temperature Self refresh to Feature List, Operating Temperature and to SPD Codes |
| 20 | Changed footnote 1 (Table 9) into "Attention" |
| 29 | Added footnote 2 to I_{DD} Currents (Table 18) |
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| 28, 32 | SPD Codes updated |
| 35 | Package Outline figure updated |

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1 Overview

This chapter gives an overview of the 240-Pin Registered DDR SDRAM Modules product family and describes its main characteristics.

1.1 Features

- 240-Pin PC2-4200 and PC2-3200 DDR2 SDRAM memory modules for PC, Workstation and Server main memory applications.
- One rank 128M x72, 256M x72 module organization and 128M x 8, 256M x4 chip organization
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- 1 and 2 GByte module built with 1 Gbit DDR2 SDRAMs in P-TFBGA-68 chipsize packages.
- All speed grades faster than DDR2-400 comply with DDR2-400 timing specifications as well.
- Programmable CAS Latencies (3, 4 & 5), Burst Length (4 & 8) and Burst Type
- Auto Refresh (CBR) and Self Refresh
- Average Refresh Period 7.8 μ s at a T_{CASE} lower than 85 °C, 3.9 μ s between 85 °C and 95 °C
- Programmable self refresh rate via EMRS2 setting
- All inputs and outputs SSTL_18 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E²PROM
- RDIMM Dimensions (nominal): 30,00 mm high, 133.35 mm wide
- Based on JEDEC standard reference card layouts Raw Card "A-F" and "C-H"
- RoHS compliant products¹⁾

TABLE 1
Performance Table

| Product Type Speed Code | | | -3S | -3.7 | -5 | Unit |
|-------------------------|------|-----------|-------------------|-------------------|-------------------|------|
| Speed Grade | | | PC2-5300 5-5-5 | PC2-4200 4-4-4 | PC2-3200 4-4-4 | — |
| Max. Clock Frequency | @CL5 | f_{CK5} | 333 | 266 | 200 | MHz |
| | @CL4 | f_{CK4} | 266 | 266 | 200 | MHz |
| | @CL3 | f_{CK3} | 200 | 200 | 200 | MHz |
| Min. RAS-CAS-Delay | | t_{RCD} | 15 | 15 | 15 | ns |
| Min. Row Precharge Time | | t_{RP} | 15 | 15 | 15 | ns |
| Min. Row Active Time | | t_{RAS} | 45 | 45 | 40 | ns |
| Min. Row Cycle Time | | t_{RC} | 60 | 60 | 55 | ns |

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

1.2 Description

The Qimonda HYS72T[128/256]00xHR-[3S/3.7/5]-A module family are Registered DIMM modules with 30,0 mm height based on DDR2 technology. DIMMs are available as ECC modules in 128M ×72 (1 GByte) and 256M ×72 (2 GByte) organization and density, intended for mounting into 240-Pin connector sockets.

The memory array is designed with 1-Gbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. All control and address

signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E²PROM device using the 2-pin I²C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.



TABLE 2
Ordering Information for RoHS Compliant Products

| Product Type ¹⁾ | Compliance Code ²⁾ | Description | SDRAM Technology |
|----------------------------|-------------------------------|-------------|------------------|
| PC2-5300 | | | |
| HYS72T256000HR-3S-A | 2GB 1Rx4 PC2-5300R-444-11-H0 | 1 Rank, ECC | 1 Gbit (×4) |
| PC2-4200 | | | |
| HYS72T256000HR-3.7-A | 2GB 1Rx4 PC2-4200R-444-11-H0 | 1 Rank, ECC | 1 Gbit (×4) |
| PC2-3200 | | | |
| HYS72T128001HR-5-A | 1GB 1Rx8 PC2-3200R-333-12-F0 | 1 Rank, ECC | 1 Gbit (×8) |
| HYS72T256000HR-5-A | 2GB 1Rx4 PC2-3200R-333-11-H0 | 1 Rank, ECC | 1 Gbit (×4) |

- 1) All Product Types end with a place code, designating the silicon die revision. Example: HYS72T256000HR-3.7-A, indicating Rev. "A" dies are used for DDR2 SDRAM components. For all Qimonda DDR2 module and component nomenclature see **Chapter 6** of this data sheet.
- 2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC2-4200R-444-11-H0", where 4200R means Registered DIMM modules with 4.26 GB/sec Module Bandwidth and "444-11" means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.1 and produced on the Raw Card "F"

TABLE 3
Address Format

| DIMM Density | Module Organization | Memory Ranks | ECC/ Non-ECC | # of SDRAMs | # of row/bank/column bits | Raw Card |
|--------------|---------------------|--------------|--------------|-------------|---------------------------|----------|
| 1 GB | 128M ×72 | 1 | ECC | 9 | 14/3/11 | A-F |
| 2 GB | 256M ×72 | 1 | ECC | 18 | 14/3/11 | C-H |

HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules**TABLE 4**
Components on Modules

| Product Type ¹⁾ | DRAM Components ¹⁾ | DRAM Density | DRAM Organisation | Note |
|----------------------------|-------------------------------|--------------|-------------------|------|
| HYS72T128001HR | HYB18T1G800AF | 1 Gbit | 128M ×8 | 2) |
| HYS72T256000HR | HYB18T1G400AF | 1 Gbit | 256M ×4 | 2) |

1) Green Product

2) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.



2 Pin Configuration

2.1 Pin Configuration

The pin configuration of the Registered DDR2 SDRAM DIMM is listed by function in **Table 5** (240 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 6** and **Table 7** respectively. The pin numbering is depicted in **Figure 1**.

TABLE 5
Pin Configuration of RDIMM

| Ball No. | Name | Pin Type | Buffer Type | Function |
|------------------------|---------------------------|----------|-------------|---|
| Clock Signals | | | | |
| 185 | CK0 | I | SSTL | Clock Signal CK0, Complementary Clock Signal CK0 |
| 186 | $\overline{\text{CK0}}$ | I | SSTL | |
| 52 | CKE0 | I | SSTL | Clock Enables 1:0 |
| 171 | CKE1 | I | SSTL | <i>Note: 2-Ranks module</i> |
| | NC | NC | — | Not Connected <i>Note: 1-Rank module</i> |
| Control Signals | | | | |
| 193 | $\overline{\text{S0}}$ | I | SSTL | Chip Select Rank 1:0 <i>Note: 2-Ranks module</i> |
| 76 | $\overline{\text{S1}}$ | I | SSTL | |
| | NC | NC | — | Not Connected <i>Note: 1-Rank module</i> |
| 192 | $\overline{\text{RAS}}$ | I | SSTL | Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE) |
| 74 | $\overline{\text{CAS}}$ | I | SSTL | |
| 73 | $\overline{\text{WE}}$ | I | SSTL | |
| 18 | $\overline{\text{RESET}}$ | I | CMOS | Register Reset |
| Address Signals | | | | |
| 71 | BA0 | I | SSTL | Bank Address Bus 1:0 |
| 190 | BA1 | I | SSTL | |
| 54 | BA2 | I | SSTL | Bank Address Bus 2 Greater than 512Mb DDR2 SDRAMS |
| | NC | I | SSTL | Not Connected Less than 1Gb DDR2 SDRAMS |



HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

| Ball No. | Name | Pin Type | Buffer Type | Function |
|----------|------|----------|-------------|---|
| 188 | A0 | I | SSTL | Address Bus 12:0, Address Signal 10/AutoPrecharge |
| 183 | A1 | I | SSTL | |
| 63 | A2 | I | SSTL | |
| 182 | A3 | I | SSTL | |
| 61 | A4 | I | SSTL | |
| 60 | A5 | I | SSTL | |
| 180 | A6 | I | SSTL | |
| 58 | A7 | I | SSTL | |
| 179 | A8 | I | SSTL | |
| 177 | A9 | I | SSTL | |
| 70 | A10 | I | SSTL | |
| | AP | I | SSTL | |
| 57 | A11 | I | SSTL | |
| 176 | A12 | I | SSTL | |
| 196 | A13 | I | SSTL | Address Signal 13 |
| | NC | NC | — | Not Connected <i>Note: Non CA parity modules based on 256 Mbit component</i> |
| 174 | A14 | I | SSTL | Address Signal 14 <i>Note: CA Parity module</i> |
| | NC | NC | — | Not Connected <i>Note: Non CA parity module. Less than 1 GBit per DRAM die.</i> |
| 173 | A15 | I | SSTL | Address Signal 14 <i>Note: CA Parity module</i> |
| | NC | NC | — | Not Connected <i>Note: Non CA parity module. Less than 1 GBit per DRAM die.</i> |



HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---------------------|------|----------|-------------|----------------------|
| Data Signals | | | | |
| 3 | DQ0 | I/O | SSTL | Data Bus 63:0 |
| 4 | DQ1 | I/O | SSTL | |
| 9 | DQ2 | I/O | SSTL | |
| 10 | DQ3 | I/O | SSTL | |
| 122 | DQ4 | I/O | SSTL | |
| 123 | DQ5 | I/O | SSTL | |
| 128 | DQ6 | I/O | SSTL | |
| 129 | DQ7 | I/O | SSTL | |
| 12 | DQ8 | I/O | SSTL | |
| 13 | DQ9 | I/O | SSTL | |
| 21 | DQ10 | I/O | SSTL | |
| 22 | DQ11 | I/O | SSTL | |
| 131 | DQ12 | I/O | SSTL | |
| 132 | DQ13 | I/O | SSTL | |
| 140 | DQ14 | I/O | SSTL | |
| 141 | DQ15 | I/O | SSTL | |
| 24 | DQ16 | I/O | SSTL | |
| 25 | DQ17 | I/O | SSTL | |
| 30 | DQ18 | I/O | SSTL | |
| 31 | DQ19 | I/O | SSTL | |
| 143 | DQ20 | I/O | SSTL | |
| 144 | DQ21 | I/O | SSTL | |
| 149 | DQ22 | I/O | SSTL | |
| 150 | DQ23 | I/O | SSTL | |
| 33 | DQ24 | I/O | SSTL | |
| 34 | DQ25 | I/O | SSTL | |
| 39 | DQ26 | I/O | SSTL | |
| 40 | DQ27 | I/O | SSTL | |
| 152 | DQ28 | I/O | SSTL | |
| 153 | DQ29 | I/O | SSTL | |
| 158 | DQ30 | I/O | SSTL | |
| 159 | DQ31 | I/O | SSTL | |
| 80 | DQ32 | I/O | SSTL | |
| 81 | DQ33 | I/O | SSTL | |
| 86 | DQ34 | I/O | SSTL | |
| 87 | DQ35 | I/O | SSTL | |
| 199 | DQ36 | I/O | SSTL | |
| 200 | DQ37 | I/O | SSTL | |
| 205 | DQ38 | I/O | SSTL | |



HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

| Ball No. | Name | Pin Type | Buffer Type | Function |
|-------------------|------|----------|-------------|--|
| 206 | DQ39 | I/O | SSTL | Data Bus 63:0 |
| 89 | DQ40 | I/O | SSTL | |
| 90 | DQ41 | I/O | SSTL | |
| 95 | DQ42 | I/O | SSTL | |
| 96 | DQ43 | I/O | SSTL | |
| 208 | DQ44 | I/O | SSTL | |
| 209 | DQ45 | I/O | SSTL | |
| 214 | DQ46 | I/O | SSTL | |
| 215 | DQ47 | I/O | SSTL | |
| 98 | DQ48 | I/O | SSTL | |
| 99 | DQ49 | I/O | SSTL | |
| 107 | DQ50 | I/O | SSTL | |
| 108 | DQ51 | I/O | SSTL | |
| 217 | DQ52 | I/O | SSTL | |
| 218 | DQ53 | I/O | SSTL | |
| 226 | DQ54 | I/O | SSTL | |
| 227 | DQ55 | I/O | SSTL | |
| 110 | DQ56 | I/O | SSTL | |
| 111 | DQ57 | I/O | SSTL | |
| 116 | DQ58 | I/O | SSTL | |
| 117 | DQ59 | I/O | SSTL | |
| 229 | DQ60 | I/O | SSTL | |
| 230 | DQ61 | I/O | SSTL | |
| 235 | DQ62 | I/O | SSTL | |
| 236 | DQ63 | I/O | SSTL | |
| Check Bits | | | | |
| 42 | CB0 | I/O | SSTL | Check Bits 7:0 <i>Note: NC on Non-ECC module</i> |
| 43 | CB1 | I/O | SSTL | |
| 48 | CB2 | I/O | SSTL | |
| 49 | CB3 | I/O | SSTL | |
| 161 | CB4 | I/O | SSTL | |
| 162 | CB5 | I/O | SSTL | |
| 167 | CB6 | I/O | SSTL | |
| 168 | CB7 | I/O | SSTL | |



HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

| Ball No. | Name | Pin Type | Buffer Type | Function |
|------------------------|---------------------------|----------|-------------|--------------------------|
| Data Strobe Bus | | | | |
| 7 | DQS0 | I/O | SSTL | Data Strobes 17:0 |
| 6 | $\overline{\text{DQS0}}$ | I/O | SSTL | |
| 16 | DQS1 | I/O | SSTL | |
| 15 | $\overline{\text{DQS1}}$ | I/O | SSTL | |
| 28 | DQS2 | I/O | SSTL | |
| 27 | $\overline{\text{DQS2}}$ | I/O | SSTL | |
| 37 | DQS3 | I/O | SSTL | |
| 36 | $\overline{\text{DQS3}}$ | I/O | SSTL | |
| 84 | DQS4 | I/O | SSTL | |
| 83 | $\overline{\text{DQS4}}$ | I/O | SSTL | |
| 93 | DQS5 | I/O | SSTL | |
| 92 | $\overline{\text{DQS5}}$ | I/O | SSTL | |
| 105 | DQS6 | I/O | SSTL | |
| 104 | $\overline{\text{DQS6}}$ | I/O | SSTL | |
| 114 | DQS7 | I/O | SSTL | |
| 113 | $\overline{\text{DQS7}}$ | I/O | SSTL | |
| 46 | DQS8 | I/O | SSTL | |
| 45 | $\overline{\text{DQS8}}$ | I/O | SSTL | |
| 125 | DQS9 | I/O | SSTL | |
| 126 | $\overline{\text{DQS9}}$ | I/O | SSTL | |
| 134 | DQS10 | I/O | SSTL | |
| 135 | $\overline{\text{DQS10}}$ | I/O | SSTL | |
| 146 | DQS11 | I/O | SSTL | |
| 147 | $\overline{\text{DQS11}}$ | I/O | SSTL | |
| 155 | DQS12 | I/O | SSTL | |
| 156 | $\overline{\text{DQS12}}$ | I/O | SSTL | |
| 202 | DQS13 | I/O | SSTL | |
| 203 | $\overline{\text{DQS13}}$ | I/O | SSTL | |
| 211 | DQS14 | I/O | SSTL | |
| 212 | $\overline{\text{DQS14}}$ | I/O | SSTL | |
| 223 | DQS15 | I/O | SSTL | |
| 224 | $\overline{\text{DQS15}}$ | I/O | SSTL | |
| 232 | DQS16 | I/O | SSTL | |
| 233 | $\overline{\text{DQS16}}$ | I/O | SSTL | |
| 164 | DQS17 | I/O | SSTL | |
| 165 | $\overline{\text{DQS17}}$ | I/O | SSTL | |



HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

| Ball No. | Name | Pin Type | Buffer Type | Function |
|---|-------------|----------|-------------|---|
| Data Mask | | | | |
| 125 | DM0 | I | SSTL | Data Masks 8:0 <i>Note: x8 based module</i> |
| 134 | DM1 | I | SSTL | |
| 146 | DM2 | I | SSTL | |
| 155 | DM3 | I | SSTL | |
| 202 | DM4 | I | SSTL | |
| 211 | DM5 | I | SSTL | |
| 223 | DM6 | I | SSTL | |
| 232 | DM7 | I | SSTL | |
| 164 | DM8 | I | SSTL | |
| EEPROM | | | | |
| 120 | SCL | I | CMOS | Serial Bus Clock |
| 119 | SDA | I/O | OD | Serial Bus Data |
| 239 | SA0 | I | CMOS | Serial Address Select Bus 2:0 |
| 240 | SA1 | I | CMOS | |
| 101 | SA2 | I | CMOS | |
| Parity | | | | |
| 55 | ERR_OUT | O | CMOS | Parity bits |
| | PAR_IN | I | CMOS | |
| Power Supplies | | | | |
| 1 | V_{REF} | AI | — | I/O Reference Voltage |
| 238 | V_{DDSPD} | PWR | — | EEPROM Power Supply |
| 51, 56, 62, 72, 75, 78, 170, 175, 181, 191, 194 | V_{DDQ} | PWR | — | I/O Driver Power Supply |
| 53, 59, 64, 67, 69, 172, 178, 184, 187, 189, 197 | V_{DD} | PWR | — | Power Supply |
| 2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 65, 66, 79, 82, 85, 88, 91, 94, 97, 100, 103, 106, 109, 112, 115, 118, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 169, 198, 201, 204, 207, 210, 213, 216, 219, 222, 225, 228, 231, 234, 237 | V_{SS} | GND | — | Ground Plane |



HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

| Ball No. | Name | Pin Type | Buffer Type | Function |
|--|------|----------|-------------|---------------------------------------|
| Other Pins | | | | |
| 19, 55, 68, 102, 137, 138, 173, 220, 221 | NC | NC | — | Not connected |
| 195 | ODT0 | I | SSTL | On-Die Termination Control 1:0 |
| 77 | ODT1 | I | SSTL | <i>Note: 2-Ranks module</i> |
| | NC | NC | — | <i>Note: 1-Rank modules</i> |

TABLE 6
Abbreviations for Buffer Type

| Abbreviation | Description |
|--------------|---|
| SSTL | Serial Stub Terminated Logic (SSTL_18) |
| CMOS | CMOS Levels |
| OD | Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. |

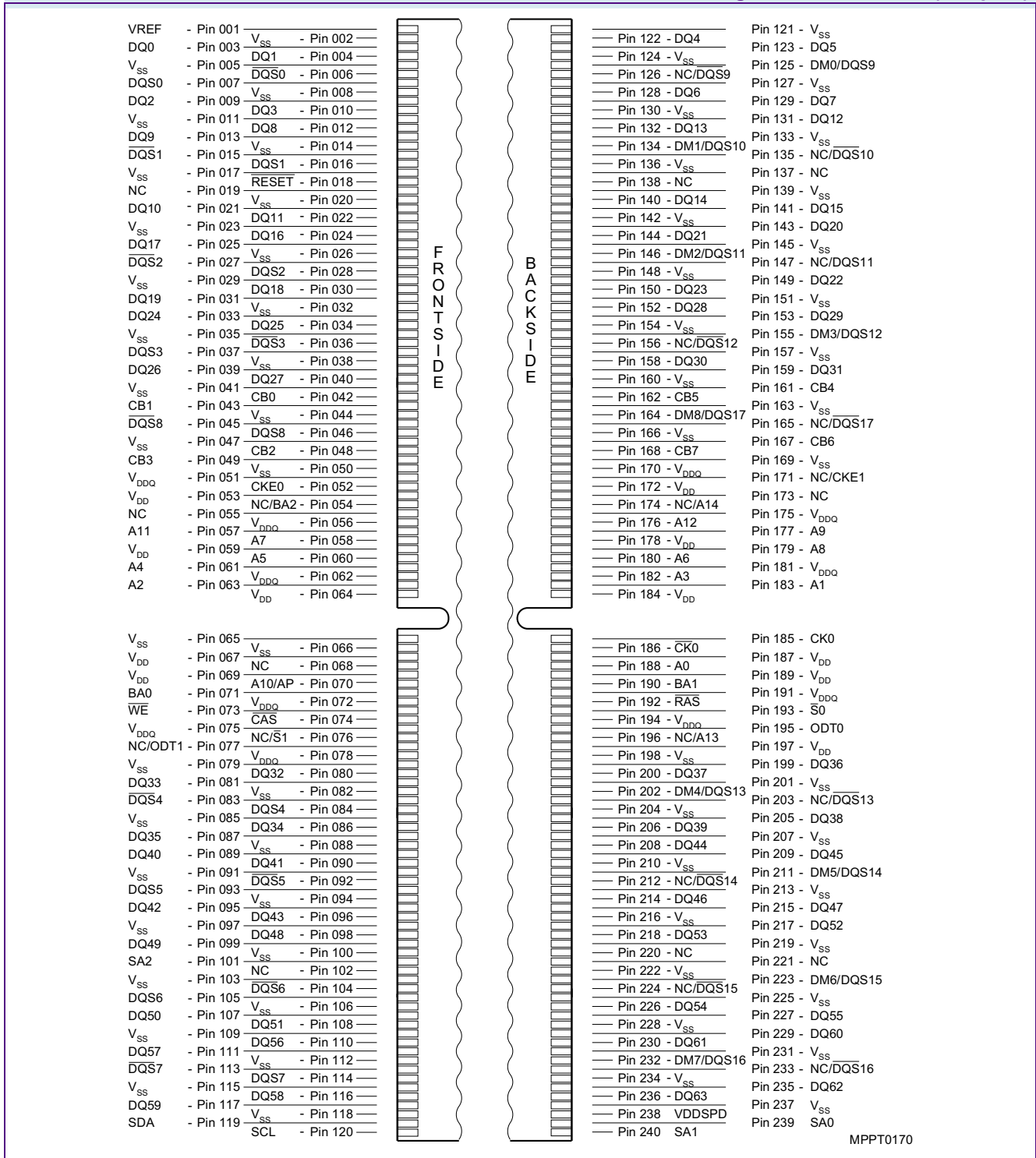
TABLE 7
Abbreviations for Pin Type

| Abbreviation | Description |
|--------------|---|
| I | Standard input-only pin. Digital levels. |
| O | Output. Digital levels. |
| I/O | I/O is a bidirectional input/output signal. |
| AI | Input. Analog levels. |
| PWR | Power |
| GND | Ground |
| NU | Not Usable |
| NC | Not Connected |



HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

FIGURE 1
Pin Configuration for RDIMM (240 pins)



MPPT0170



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

TABLE 8
Absolute Maximum Ratings

| Parameter | Symbol | Values | | Unit | Note/Test Condition |
|---|-------------------|--------|------|------|---------------------|
| | | Min. | Max. | | |
| Voltage on any pins relative to V_{SS} | V_{IN}, V_{OUT} | -0.5 | 2.3 | V | |
| Voltage on V_{DD} relative to V_{SS} | V_{DD} | -1.0 | 2.3 | V | |
| Voltage on V_{DDQ} relative to V_{SS} | V_{DDQ} | -0.5 | 2.3 | V | |
| Storage Humidity (without condensation) | H_{STG} | 5 | 95 | % | |

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.



3.2 DC Operating Conditions

TABLE 9
Operating Conditions

| Parameter | Symbol | Values | | Unit | Note |
|---|------------|--------|------|------|----------|
| | | Min. | Max. | | |
| DIMM Module Operating Temperature Range (ambient) | T_{OPR} | 0 | +55 | °C | 1) |
| DRAM Component Case Temperature Range | T_{CASE} | 0 | +95 | °C | 2)3)4)5) |
| Storage Temperature | T_{STG} | -55 | +100 | °C | |
| Barometric Pressure (operating & storage) | P_{Bar} | +69 | +105 | kPa | 6) |
| Operating Humidity (relative) | H_{OPR} | 10 | 90 | % | |

- 1) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to "1". When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50 %
- 2) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.
- 3) Within the DRAM Component Case Temperature range all DRAM specification will be supported.
- 4) Above 85 °C DRAM case temperature the Auto-Refresh command interval has to be reduced to $t_{REF1} = 3.9 \mu s$.
- 5) Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 °C case temperature before initiating self-refresh operation.
- 6) Up to 3000 m

TABLE 10
Supply Voltage Levels and DC Operating Conditions

| Parameter | Symbol | Values | | | Unit | Note |
|-----------------------------|--------------|-----------------------|----------------------|-----------------------|------|------|
| | | Min. | Typ. | Max. | | |
| Device Supply Voltage | V_{DD} | 1.7 | 1.8 | 1.9 | V | |
| Output Supply Voltage | V_{DDQ} | 1.7 | 1.8 | 1.9 | V | 1) |
| Input Reference Voltage | V_{REF} | $0.49 \times V_{DDQ}$ | $0.5 \times V_{DDQ}$ | $0.51 \times V_{DDQ}$ | V | 2) |
| SPD Supply Voltage | V_{DDSPD} | 1.7 | — | 3.6 | V | |
| DC Input Logic High | $V_{IH(DC)}$ | $V_{REF} + 0.125$ | — | $V_{DDQ} + 0.3$ | V | |
| DC Input Logic Low | $V_{IL(DC)}$ | -0.30 | — | $V_{REF} - 0.125$ | V | |
| In / Output Leakage Current | I_L | -5 | — | 5 | μA | 3) |

- 1) Under all conditions, V_{DDQ} must be less than or equal to V_{DD}
- 2) Peak to peak AC noise on V_{REF} may not exceed $\pm 2\% V_{REF(DC)}$. V_{REF} is also expected to track noise in V_{DDQ} .
- 3) Input voltage for any connector pin under test of $0 V \leq V_{IN} \leq V_{DDQ} + 0.3 V$; all other pins at 0 V. Current is per pin



3.3 AC Characteristics

3.3.1 Speed Grades Definitions

TABLE 11
Speed Grade Definition

| Speed Grade | | DDR2-667 | | DDR2-533C | | DDR2-400B | | Unit | Note | |
|----------------------|-----------|----------|-------|-----------|-------|-----------|-------|----------|------------|----------|
| QAG Sort Name | | -3S | | -3.7 | | -5 | | | | |
| CAS-RCD-RP latencies | | 5-5-5 | | 4-4-4 | | 3-3-3 | | t_{CK} | | |
| Parameter | Symbol | Min. | Max. | Min. | Max. | Min. | Max. | — | | |
| Clock Frequency | @ CL = 3 | t_{CK} | 5 | 8 | 5 | 8 | 5 | 8 | ns | 1)2)3)4) |
| | @ CL = 4 | t_{CK} | 3.75 | 8 | 3.75 | 8 | 5 | 8 | ns | 1)2)3)4) |
| | @ CL = 5 | t_{CK} | 3 | 8 | 3.75 | 8 | 5 | 8 | ns | 1)2)3)4) |
| Row Active Time | t_{RAS} | 45 | 70000 | 45 | 70000 | 40 | 70000 | ns | 1)2)3)4)5) | |
| Row Cycle Time | t_{RC} | 60 | — | 60 | — | 55 | — | ns | 1)2)3)4) | |
| RAS-CAS-Delay | t_{RCD} | 15 | — | 15 | — | 15 | — | ns | 1)2)3)4) | |
| Row Precharge Time | t_{RP} | 15 | — | 15 | — | 15 | — | ns | 1)2)3)4) | |

- 1) Timings are guaranteed with CK/CK differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the "Reference Load for Timing Measurements"
- 2) The CK/CK input reference level (for timing reference to CK/CK) is the point at which CK and CK cross. The DQS / DQS, RDQS / RDQS, input reference level is the crosspoint when in differential strobe mode.
- 3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 4) The output timing reference voltage level is V_{TT} .
- 5) $t_{RAS,MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to $9 \times t_{REFI}$.

3.3.2 AC Timing Parameters

TABLE 12
DRAM Component Timing Parameter by Speed Grade - DDR2-667

| Parameter | Symbol | DDR2-667 | | Unit | Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾⁷⁾⁸⁾ |
|------------------------------------|--------------|----------|------|--------------|----------------------------------|
| | | Min. | Max. | | |
| DQ output access time from CK / CK | t_{AC} | -450 | +450 | ps | 9) |
| CAS to CAS command delay | t_{CCD} | 2 | — | nCK | |
| Average clock high pulse width | $t_{CH,AVG}$ | 0.48 | 0.52 | $t_{CK,AVG}$ | 10)11) |
| Average clock period | $t_{CK,AVG}$ | 3000 | 8000 | ps | |



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| Parameter | Symbol | DDR2-667 | | Unit | Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾⁷⁾⁸⁾ |
|--|---------------|------------------------------------|--------------|--------------|----------------------------------|
| | | Min. | Max. | | |
| CKE minimum pulse width (high and low pulse width) | t_{CKE} | 3 | — | nCK | 12) |
| Average clock low pulse width | $t_{CL.AVG}$ | 0.48 | 0.52 | $t_{CK.AVG}$ | 1)1) |
| Auto-Precharge write recovery + precharge time | t_{DAL} | WR + t_{nRP} | — | nCK | 13)14) |
| Minimum time clocks remain ON after CKE asynchronously drops LOW | t_{DELAY} | $t_{IS} + t_{CK.AVG} + t_{IH}$ | — | ns | |
| DQ and DM input hold time | $t_{DH.BASE}$ | 175 | — | ps | 19)20)15) |
| DQ and DM input pulse width for each input | t_{DIPW} | 0.35 | — | $t_{CK.AVG}$ | |
| DQS output access time from CK / \overline{CK} | t_{DQSCK} | -400 | +400 | ps | 9) |
| DQS input high pulse width | t_{DQSH} | 0.35 | — | $t_{CK.AVG}$ | |
| DQS input low pulse width | t_{DQSL} | 0.35 | — | $t_{CK.AVG}$ | |
| DQS-DQ skew for DQS & associated DQ signals | t_{DQSQ} | — | 240 | ps | 16) |
| DQS latching rising transition to associated clock edges | t_{DQSS} | -0.25 | +0.25 | $t_{CK.AVG}$ | 17) |
| DQ and DM input setup time | $t_{DS.BASE}$ | 100 | — | ps | 18)19)20) |
| DQS falling edge hold time from CK | t_{DSH} | 0.2 | — | $t_{CK.AVG}$ | 17) |
| DQS falling edge to CK setup time | t_{DSS} | 0.2 | — | $t_{CK.AVG}$ | 17) |
| CK half pulse width | t_{HP} | Min($t_{CH.ABS}$, $t_{CL.ABS}$) | — | ps | 21) |
| Data-out high-impedance time from CK / \overline{CK} | t_{HZ} | — | $t_{AC.MAX}$ | ps | 9)22) |
| Address and control input hold time | $t_{IH.BASE}$ | 275 | — | ps | 25)23) |
| Control & address input pulse width for each input | t_{IPW} | 0.6 | — | $t_{CK.AVG}$ | |
| Address and control input setup time | $t_{IS.BASE}$ | 200 | — | ps | 24)25) |
| DQ low impedance time from CK/ \overline{CK} | $t_{LZ.DQ}$ | $2 \times t_{AC.MIN}$ | $t_{AC.MAX}$ | ps | 9)22) |
| DQS/DQS low-impedance time from CK / \overline{CK} | $t_{LZ.DQS}$ | $t_{AC.MIN}$ | $t_{AC.MAX}$ | ps | 9)22) |
| MRS command to ODT update delay | t_{MOD} | 0 | 12 | ns | 1) |
| Mode register set command cycle time | t_{MRD} | 2 | — | nCK | |
| OCD drive mode output delay | t_{OIT} | 0 | 12 | ns | 1) |
| DQ/DQS output hold time from DQS | t_{QH} | $t_{HP} - t_{QHS}$ | — | ps | 26) |
| DQ hold skew factor | t_{QHS} | — | 340 | ps | 27) |
| Read preamble | t_{RPRE} | 0.9 | 1.1 | $t_{CK.AVG}$ | 28)29) |
| Read postamble | t_{RPST} | 0.4 | 0.6 | $t_{CK.AVG}$ | 28)30) |
| Internal Read to Precharge command delay | t_{RTP} | 7.5 | — | ns | 31) |
| Write preamble | t_{WPRE} | 0.35 | — | $t_{CK.AVG}$ | |
| Write postamble | t_{WPST} | 0.4 | 0.6 | $t_{CK.AVG}$ | |
| Write recovery time | t_{WR} | 15 | — | ns | 31) |
| Internal write to read command delay | t_{WTR} | 7.5 | — | ns | 31)32) |
| Exit power down to read command | t_{XARD} | 2 | — | nCK | |
| Exit active power-down mode to read command (slow exit, lower power) | t_{XARDS} | 7 – AL | — | nCK | |



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| Parameter | Symbol | DDR2-667 | | Unit | Note 1)2)3)4)5)6)7)8) |
|---|------------|----------------|------|------|-----------------------|
| | | Min. | Max. | | |
| Exit precharge power-down to any valid command (other than NOP or Deselect) | t_{XP} | 2 | — | nCK | |
| Exit self-refresh to a non-read command | t_{XSNR} | $t_{RFC} + 10$ | — | ns | 31) |
| Exit self-refresh to read command | t_{XSRD} | 200 | — | nCK | |
| Write command to DQS associated clock edges | WL | RL-1 | | nCK | |

- 1) For details and notes see the relevant Qimonda component data sheet
- 2) $V_{DDQ} = 1.8\text{ V} \pm 0.1\text{ V}$; $V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$. See notes 1)6)1)8)
- 3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) Timings are guaranteed with CK/CK differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 5) The CK / $\overline{\text{CK}}$ input reference level (for timing reference to CK / $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross. The DQS / $\overline{\text{DQS}}$, RDQS / $\overline{\text{RDQS}}$, input reference level is the crosspoint when in differential strobe mode.
- 6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $\text{CKE} = 0.2 \times V_{DDQ}$ is recognized as low.
- 7) The output timing reference voltage level is V_{TT} .
- 8) New units, ' $t_{\text{CK,AVG}}$ ' and 'nCK', are introduced in DDR2-667 and DDR2-800. Unit ' $t_{\text{CK,AVG}}$ ' represents the actual $t_{\text{CK,AVG}}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, ' t_{CK} ' is used for both concepts. Example: $t_{XP} = 2$ [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is $2 \times t_{\text{CK,AVG}} + t_{\text{ERR,2PER(Min)}}$.
- 9) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{\text{ERR(6-10per)}}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has $t_{\text{ERR(6-10PER),MIN}} = -272$ ps and $t_{\text{ERR(6-10PER),MAX}} = +293$ ps, then $t_{\text{DQSCK,MIN(DERATED)}} = t_{\text{DQSCK,MIN}} - t_{\text{ERR(6-10PER),MAX}} = -400\text{ ps} - 293\text{ ps} = -693\text{ ps}$ and $t_{\text{DQSCK,MAX(DERATED)}} = t_{\text{DQSCK,MAX}} - t_{\text{ERR(6-10PER),MIN}} = 400\text{ ps} + 272\text{ ps} = +672\text{ ps}$. Similarly, $t_{\text{LZ,DQ}}$ for DDR2-667 derates to $t_{\text{LZ,DQ,MIN(DERATED)}} = -900\text{ ps} - 293\text{ ps} = -1193\text{ ps}$ and $t_{\text{LZ,DQ,MAX(DERATED)}} = 450\text{ ps} + 272\text{ ps} = +722\text{ ps}$. (Caution on the MIN/MAX usage!)
- 10) Input clock jitter spec parameter. These parameters are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2-667 and DDR2-800 only. The jitter specified is a random jitter meeting a Gaussian distribution.
- 11) These parameters are specified per their average values, however it is understood that the relationship between the average timing and the absolute instantaneous timing holds all the times (min. and max of SPEC values are to be used for calculations).
- 12) $t_{\text{CKE,MIN}}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $t_{\text{IS}} + 2 \times t_{\text{CK}} + t_{\text{IH}}$.
- 13) $\text{DAL} = \text{WR} + \text{RU}\{t_{\text{RP}}(\text{ns}) / t_{\text{CK}}(\text{ns})\}$, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For t_{RP} , if the result of the division is not already an integer, round up to the next highest integer. t_{CK} refers to the application clock period. Example: For DDR2-533 at $t_{\text{CK}} = 3.75$ ns with t_{WR} programmed to 4 clocks. $t_{\text{DAL}} = 4 + (15\text{ ns} / 3.75\text{ ns})$ clocks = 4 + (4) clocks = 8 clocks.
- 14) $t_{\text{DAL,nCK}} = \text{WR} [\text{nCK}] + t_{\text{nRP,nCK}} = \text{WR} + \text{RU}\{t_{\text{RP}} [\text{ps}] / t_{\text{CK,AVG}} [\text{ps}]\}$, where WR is the value programmed in the EMR.
- 15) Input waveform timing t_{DH} with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{\text{IH,DC}}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{\text{IL,DC}}$ level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{\text{IL,DC,MAX}}$ and $V_{\text{IH,DC,MIN}}$. See Figure 3.
- 16) t_{DQSQ} : Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{\text{DQS}}$ and associated DQ in any given cycle.
- 17) These parameters are measured from a data strobe signal ((L/U/R)DQS / $\overline{\text{DQS}}$) crossing to its respective clock signal (CK / $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{\text{JIT,PER}}$, $t_{\text{JIT,CC}}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
- 18) Input waveform timing t_{DS} with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the $V_{\text{IH,AC}}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{\text{IL,AC}}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{\text{il(DC)MAX}}$ and $V_{\text{ih(DC)MIN}}$. See Figure 3.
- 19) If t_{DS} or t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
- 20) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS / $\overline{\text{DQS}}$) crossing.



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- 21) t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH} . The value to be used for t_{QH} calculation is determined by the following equation; $t_{HP} = \text{MIN}(t_{CH,ABS}, t_{CL,ABS})$, where, $t_{CH,ABS}$ is the minimum of the actual instantaneous clock high time; $t_{CL,ABS}$ is the minimum of the actual instantaneous clock low time.
- 22) t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}).
- 23) Input waveform timing is referenced from the input signal crossing at the $V_{IL,DC}$ level for a rising signal and $V_{IH,DC}$ for a falling signal applied to the device under test. See **Figure 4**.
- 24) Input waveform timing is referenced from the input signal crossing at the $V_{IH,AC}$ level for a rising signal and $V_{IL,AC}$ for a falling signal applied to the device under test. See **Figure 4**.
- 25) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK / \overline{CK}) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT,PER}$, $t_{JIT,CC}$, etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
- 26) $t_{QH} = t_{HP} - t_{QHS}$, where: t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.}
Examples: 1) If the system provides t_{HP} of 1315 ps into a DDR2-667 SDRAM, the DRAM provides t_{QH} of 975 ps minimum. 2) If the system provides t_{HP} of 1420 ps into a DDR2-667 SDRAM, the DRAM provides t_{QH} of 1080 ps minimum.
- 27) t_{QHS} accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.
- 28) t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}). **Figure 2** shows a method to calculate these points when the device is no longer driving (t_{RPST}), or begins driving (t_{RPRE}) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
- 29) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT,PER}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has $t_{JIT,PER,MIN} = -72$ ps and $t_{JIT,PER,MAX} = +93$ ps, then $t_{RPRE,MIN(DERATED)} = t_{RPRE,MIN} + t_{JIT,PER,MIN} = 0.9 \times t_{CK,AVG} - 72$ ps = + 2178 ps and $t_{RPRE,MAX(DERATED)} = t_{RPRE,MAX} + t_{JIT,PER,MAX} = 1.1 \times t_{CK,AVG} + 93$ ps = + 2843 ps. (Caution on the MIN/MAX usage!).
- 30) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT,DUTY}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has $t_{JIT,DUTY,MIN} = -72$ ps and $t_{JIT,DUTY,MAX} = +93$ ps, then $t_{RPST,MIN(DERATED)} = t_{RPST,MIN} + t_{JIT,DUTY,MIN} = 0.4 \times t_{CK,AVG} - 72$ ps = + 928 ps and $t_{RPST,MAX(DERATED)} = t_{RPST,MAX} + t_{JIT,DUTY,MAX} = 0.6 \times t_{CK,AVG} + 93$ ps = + 1592 ps. (Caution on the MIN/MAX usage!).
- 31) For these parameters, the DDR2 SDRAM device is characterized and verified to support $t_{nPARAM} = \text{RU}\{t_{PARAM} / t_{CK,AVG}\}$, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support $t_{nRP} = \text{RU}\{t_{RP} / t_{CK,AVG}\}$, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2-667 5-5-5, of which $t_{RP} = 15$ ns, the device will support $t_{nRP} = \text{RU}\{t_{RP} / t_{CK,AVG}\} = 5$, i.e. as long as the input clock jitter specifications are met, Precharge command at T_m and Active command at $T_m + 5$ is valid even if $(T_m + 5 - T_m)$ is less than 15 ns due to input clock jitter.
- 32) t_{WTR} is at least two clocks ($2 \times t_{CK}$) independent of operation frequency.

FIGURE 2

Method for calculating transitions and endpoint

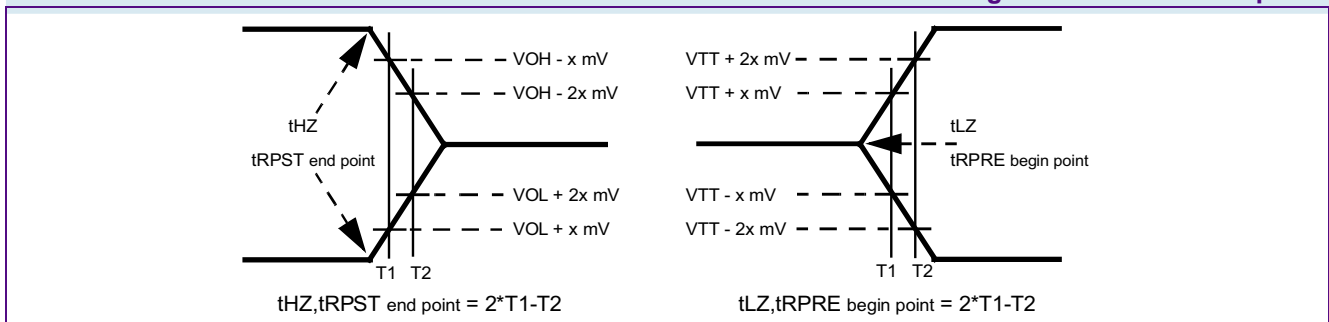




FIGURE 3

Differential input waveform timing - t_{DS} and t_{DH}

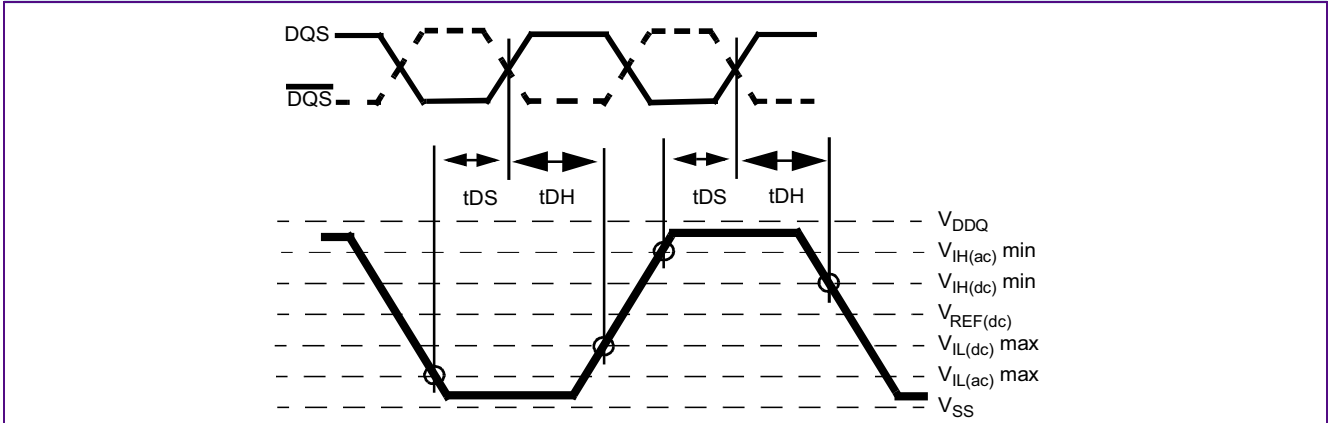


FIGURE 4

Differential input waveform timing - t_{IS} and t_{IH}

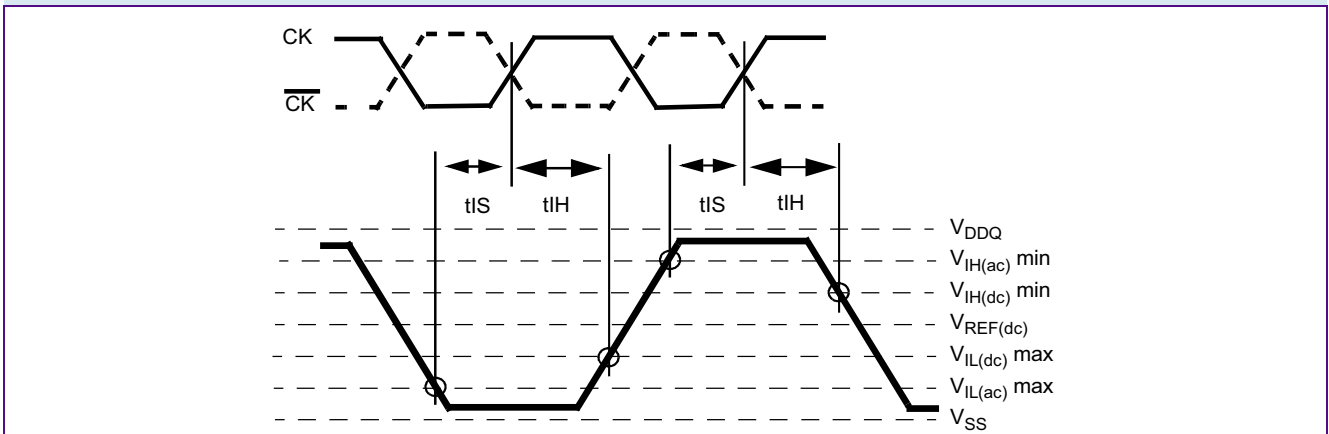




TABLE 13
DRAM Component Timing Parameter by Speed Grade - DDR2-533

| Parameter | Symbol | DDR2-533 | | Unit | Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾⁷⁾ |
|--|------------------------|----------------------------|--------------|---------------|--------------------------------|
| | | Min. | Max. | | |
| DQ output access time from CK / $\overline{\text{CK}}$ | t_{AC} | -500 | +500 | ps | |
| CAS A to $\overline{\text{CAS}}$ B command period | t_{CCD} | 2 | — | t_{CK} | |
| CK, $\overline{\text{CK}}$ high-level width | t_{CH} | 0.45 | 0.55 | t_{CK} | |
| CKE minimum high and low pulse width | t_{CKE} | 3 | — | t_{CK} | |
| CK, $\overline{\text{CK}}$ low-level width | t_{CL} | 0.45 | 0.55 | t_{CK} | |
| Auto-Precharge write recovery + precharge time | t_{DAL} | WR + t_{RP} | — | t_{CK} | 8)18) |
| Minimum time clocks remain ON after CKE asynchronously drops LOW | t_{DELAY} | $t_{IS} + t_{CK} + t_{IH}$ | — | ns | 9) |
| DQ and DM input hold time (differential data strobe) | $t_{DH}(\text{base})$ | 225 | — | ps | 10) |
| DQ and DM input hold time (single ended data strobe) | $t_{DH1}(\text{base})$ | -25 | — | ps | 11) |
| DQ and DM input pulse width (each input) | t_{DIPW} | 0.35 | — | t_{CK} | |
| DQS output access time from CK / $\overline{\text{CK}}$ | t_{DQSCK} | -450 | +450 | ps | |
| DQS input low (high) pulse width (write cycle) | $t_{DQSL,H}$ | 0.35 | — | t_{CK} | |
| DQS-DQ skew (for DQS & associated DQ signals) | t_{DQSQ} | — | 300 | ps | 11) |
| Write command to 1st DQS latching transition | t_{DQSS} | - 0.25 | + 0.25 | t_{CK} | |
| DQ and DM input setup time (differential data strobe) | $t_{DS}(\text{base})$ | 100 | — | ps | 11) |
| DQ and DM input setup time (single ended data strobe) | $t_{DS1}(\text{base})$ | -25 | — | ps | 11) |
| DQS falling edge hold time from CK (write cycle) | t_{DSH} | 0.2 | — | t_{CK} | |
| DQS falling edge to CK setup time (write cycle) | t_{DSS} | 0.2 | — | t_{CK} | |
| Clock half period | t_{HP} | MIN. (t_{CL}, t_{CH}) | | | 12) |
| Data-out high-impedance time from CK / $\overline{\text{CK}}$ | t_{HZ} | — | $t_{AC,MAX}$ | ps | 13) |
| Address and control input hold time | $t_{IH}(\text{base})$ | 375 | — | ps | 11) |
| Address and control input pulse width (each input) | t_{IPW} | 0.6 | — | t_{CK} | |
| Address and control input setup time | $t_{IS}(\text{base})$ | 250 | — | ps | 11) |
| DQ low-impedance time from CK / $\overline{\text{CK}}$ | $t_{LZ(DQ)}$ | $2 \times t_{AC,MIN}$ | $t_{AC,MAX}$ | ps | 14) |
| DQS low-impedance from CK / $\overline{\text{CK}}$ | $t_{LZ(DQS)}$ | $t_{AC,MIN}$ | $t_{AC,MAX}$ | ps | 14) |
| Mode register set command cycle time | t_{MRD} | 2 | — | t_{CK} | |
| OCD drive mode output delay | t_{OIT} | 0 | 12 | ns | |
| Data output hold time from DQS | t_{QH} | $t_{HP} - t_{QHS}$ | — | — | |
| Data hold skew factor | t_{QHS} | — | 400 | ps | |
| Average periodic refresh Interval | t_{REFI} | — | 7.8 | μs | 14)15) |



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| Parameter | Symbol | DDR2-533 | | Unit | Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾⁷⁾ |
|---|-------------|--------------------|------|---------------|--------------------------------|
| | | Min. | Max. | | |
| Average periodic refresh Interval | t_{REFI} | — | 3.9 | μs | 16)18) |
| Auto-Refresh to Active/Auto-Refresh command period | t_{RFC} | — | — | ns | 17) |
| Precharge-All (4 banks) command period | t_{RP} | $t_{RP} + 1t_{CK}$ | — | ns | |
| Precharge-All (8 banks) command period | t_{RP} | $15 + 1t_{CK}$ | — | ns | |
| Read preamble | t_{RPRE} | 0.9 | 1.1 | t_{CK} | 14) |
| Read postamble | t_{RPST} | 0.40 | 0.60 | t_{CK} | 14) |
| Active bank A to Active bank B command period | t_{RRD} | 7.5 | — | ns | 14)18) |
| Active bank A to Active bank B command period | t_{RRD} | 10 | — | ns | 16)22) |
| Internal Read to Precharge command delay | t_{RTP} | 7.5 | — | ns | |
| Write preamble | t_{WPRE} | 0.25 | — | t_{CK} | |
| Write postamble | t_{WPST} | 0.40 | 0.60 | t_{CK} | 19) |
| Write recovery time for write without Auto-Precharge | t_{WR} | 15 | — | ns | |
| Internal Write to Read command delay | t_{WTR} | 7.5 | — | ns | 20) |
| Exit power down to any valid command (other than NOP or Deselect) | t_{XARD} | 2 | — | t_{CK} | 21) |
| Exit active power-down mode to Read command (slow exit, lower power) | t_{XARDS} | 6 – AL | — | t_{CK} | 21) |
| Exit precharge power-down to any valid command (other than NOP or Deselect) | t_{XP} | 2 | — | t_{CK} | |
| Exit Self-Refresh to non-Read command | t_{XSNR} | $t_{RFC} + 10$ | — | ns | |
| Exit Self-Refresh to Read command | t_{XSRD} | 200 | — | t_{CK} | |
| Write recovery time for write with Auto-Precharge | WR | t_{WR}/t_{CK} | — | t_{CK} | 22) |

- 1) For details and notes see the relevant Qimonda component data sheet.
- 2) $V_{DDQ} = 1.8 \text{ V} \pm 0.1 \text{ V}$; $V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$. See notes ¹⁾⁶⁾¹⁾⁸⁾
- 3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) Timings are guaranteed with CK/ $\overline{\text{CK}}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 5) The CK / $\overline{\text{CK}}$ input reference level (for timing reference to CK / $\overline{\text{CK}}$) is the point at which CK and $\overline{\text{CK}}$ cross. The DQS / $\overline{\text{DQS}}$, RDQS / $\overline{\text{RDQS}}$, input reference level is the crosspoint when in differential strobe mode.
- 6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $\text{CKE} = 0.2 \times V_{DDQ}$ is recognized as low.
- 7) The output timing reference voltage level is V_{TT} .
- 8) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
- 9) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
- 10) For timing definition, refer to the Component data sheet.
- 11) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / $\overline{\text{DQS}}$ and associated DQ in any given cycle.
- 12) MIN (t_{CL} , t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).



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- 13) The t_{HZ} , t_{RPST} and t_{LZ} , t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ} , t_{RPST}), or begins driving (t_{LZ} , t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are verified by design and characterization, but not subject to production test.
- 14) The Auto-Refresh command interval has been reduced to 3.9 μ s when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
- 15) $0\text{ }^{\circ}\text{C} \leq T_{CASE} \leq 85\text{ }^{\circ}\text{C}$
- 16) $85\text{ }^{\circ}\text{C} < T_{CASE} \leq 95\text{ }^{\circ}\text{C}$
- 17) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
- 18) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See Table 2 "Ordering Information for RoHS Compliant Products" on Page 4.
- 19) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 20) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
- 21) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In "standard active power-down mode" (MR, A12 = "0") a fast power-down exit timing t_{XARD} can be used. In "low active power-down mode" (MR, A12 = "1") a slow power-down exit timing t_{XARDS} has to be satisfied.
- 22) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where $WR_{MIN}[\text{cycles}] = t_{WR}(\text{ns})/t_{CK}(\text{ns})$ rounded up to the next integer value. $t_{DAL} = WR + (t_{RP}/t_{CK})$. For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.

TABLE 14
DRAM Component Timing Parameter by Speed Grade - DDR2 - 400

| Parameter | Symbol | DDR2-400 | | Unit | Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾⁷⁾ |
|--|------------------------|----------------------------|--------|----------|--------------------------------|
| | | Min. | Max. | | |
| DQ output access time from CK / $\overline{\text{CK}}$ | t_{AC} | -600 | +600 | ps | |
| CAS A to $\overline{\text{CAS}}$ B command period | t_{CCD} | 2 | — | t_{CK} | |
| CK, $\overline{\text{CK}}$ high-level width | t_{CH} | 0.45 | 0.55 | t_{CK} | |
| CKE minimum high and low pulse width | t_{CKE} | 3 | — | t_{CK} | |
| CK, $\overline{\text{CK}}$ low-level width | t_{CL} | 0.45 | 0.55 | t_{CK} | |
| Auto-Precharge write recovery + precharge time | t_{DAL} | $WR + t_{RP}$ | — | t_{CK} | 8)21) |
| Minimum time clocks remain ON after CKE asynchronously drops LOW | t_{DELAY} | $t_{IS} + t_{CK} + t_{IH}$ | — | ns | 9) |
| DQ and DM input hold time (differential data strobe) | $t_{DH}(\text{base})$ | 275 | — | ps | 10) |
| DQ and DM input hold time (single ended data strobe) | $t_{DH1}(\text{base})$ | -25 | — | ps | 11) |
| DQ and DM input pulse width (each input) | t_{DIPW} | 0.35 | — | t_{CK} | |
| DQS output access time from CK / $\overline{\text{CK}}$ | t_{DQSCK} | -500 | +500 | ps | |
| DQS input low (high) pulse width (write cycle) | $t_{DQSL,H}$ | 0.35 | — | t_{CK} | |
| DQS-DQ skew (for DQS & associated DQ signals) | t_{DQSQ} | — | 350 | ps | 11) |
| Write command to 1st DQS latching transition | t_{DQSS} | - 0.25 | + 0.25 | t_{CK} | |
| DQ and DM input setup time (differential data strobe) | $t_{DS}(\text{base})$ | 150 | — | ps | 11) |
| DQ and DM input setup time (single ended data strobe) | $t_{DS1}(\text{base})$ | -25 | — | ps | 11) |



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| Parameter | Symbol | DDR2-400 | | Unit | Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾⁷⁾ |
|---|----------------|------------------------------|--------------|----------|--------------------------------|
| | | Min. | Max. | | |
| DQS falling edge hold time from CK (write cycle) | t_{DSH} | 0.2 | — | t_{CK} | |
| DQS falling edge to CK setup time (write cycle) | t_{DSS} | 0.2 | — | t_{CK} | |
| Clock half period | t_{HP} | MIN. (t_{CL} , t_{CH}) | | — | 12) |
| Data-out high-impedance time from CK / \overline{CK} | t_{HZ} | — | $t_{AC.MAX}$ | ps | 13) |
| Address and control input hold time | $t_{IH}(base)$ | 475 | — | ps | 11) |
| Address and control input pulse width (each input) | t_{IPW} | 0.6 | — | t_{CK} | |
| Address and control input setup time | $t_{IS}(base)$ | 350 | — | ps | 11) |
| DQ low-impedance time from CK / \overline{CK} | $t_{LZ}(DQ)$ | $2 \times t_{AC.MIN}$ | $t_{AC.MAX}$ | ps | 14) |
| DQS low-impedance from CK / \overline{CK} | $t_{LZ}(DQS)$ | $t_{AC.MIN}$ | $t_{AC.MAX}$ | ps | 14) |
| Mode register set command cycle time | t_{MRD} | 2 | — | t_{CK} | |
| OCD drive mode output delay | t_{OIT} | 0 | 12 | ns | |
| Data output hold time from DQS | t_{QH} | $t_{HP} - t_{QHS}$ | — | — | |
| Data hold skew factor | t_{QHS} | — | 450 | ps | |
| Average periodic refresh Interval | t_{REFI} | — | 7.8 | μs | 14)15) |
| Average periodic refresh Interval | t_{REFI} | — | 3.9 | μs | 16)18) |
| Auto-Refresh to Active/Auto-Refresh command period | — | — | — | ns | 17) |
| Precharge-All (4 banks) command period | t_{RP} | $t_{RP} + 1t_{CK}$ | — | ns | |
| Precharge-All (8 banks) command period | t_{RP} | $15 + 1t_{CK}$ | — | ns | |
| Read preamble | t_{RPRE} | 0.9 | 1.1 | t_{CK} | 14) |
| Read postamble | t_{RPST} | 0.40 | 0.60 | t_{CK} | 14) |
| Active bank A to Active bank B command period | t_{RRD} | 7.5 | — | ns | 14)18) |
| Active bank A to Active bank B command period | t_{RRD} | 10 | — | ns | 16)22) |
| Internal Read to Precharge command delay | t_{RTP} | 7.5 | — | ns | |
| Write preamble | t_{WPRE} | 0.25 | — | t_{CK} | |
| Write postamble | t_{WPST} | 0.40 | 0.60 | t_{CK} | 19) |
| Write recovery time for write without Auto-Precharge | t_{WR} | 15 | — | ns | |
| Internal Write to Read command delay | t_{WTR} | 10 | — | ns | 20) |
| Exit power down to any valid command (other than NOP or Deselect) | t_{XARD} | 2 | — | t_{CK} | 21) |
| Exit active power-down mode to Read command (slow exit, lower power) | t_{XARDS} | 6 – AL | — | t_{CK} | 21) |
| Exit precharge power-down to any valid command (other than NOP or Deselect) | t_{XP} | 2 | — | t_{CK} | |
| Exit Self-Refresh to non-Read command | t_{XSNR} | $t_{RFC} + 10$ | — | ns | |



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Registered DDR2 SDRAM Modules

| Parameter | Symbol | DDR2-400 | | Unit | Note ¹⁾²⁾³⁾⁴⁾⁵⁾⁶⁾⁷⁾ |
|---|------------|-----------------|------|----------|--------------------------------|
| | | Min. | Max. | | |
| Exit Self-Refresh to Read command | t_{XSRD} | 200 | — | t_{CK} | |
| Write recovery time for write with Auto-Precharge | WR | t_{WR}/t_{CK} | — | t_{CK} | ²²⁾ |

- 1) For details and notes see the relevant Qimonda component data sheet.
- 2) $V_{DDQ} = 1.8 V \pm 0.1 V$; $V_{DD} = 1.8 V \pm 0.1 V$. See notes ¹⁾⁶⁾¹⁾⁸⁾
- 3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) Timings are guaranteed with CK/ \overline{CK} differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 5) The CK / \overline{CK} input reference level (for timing reference to CK / \overline{CK}) is the point at which CK and \overline{CK} cross. The DQS / \overline{DQS} , RDQS / \overline{RDQS} , input reference level is the crosspoint when in differential strobe mode.
- 6) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, $CKE = 0.2 \times V_{DDQ}$ is recognized as low.
- 7) The output timing reference voltage level is V_{TT} .
- 8) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
- 9) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
- 10) For timing definition, refer to the Component data sheet.
- 11) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / \overline{DQS} and associated DQ in any given cycle.
- 12) MIN (t_{CL} , t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
- 13) The t_{HZ} , t_{RPST} and t_{LZ} , t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ} , t_{RPST}), or begins driving (t_{LZ} , t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are verified by design and characterization, but not subject to production test.
- 14) The Auto-Refresh command interval has been reduced to 3.9 μs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
- 15) $0 \text{ }^\circ\text{C} \leq T_{CASE} \leq 85 \text{ }^\circ\text{C}$
- 16) $85 \text{ }^\circ\text{C} < T_{CASE} \leq 95 \text{ }^\circ\text{C}$
- 17) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
- 18) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See **Table 2 “Ordering Information for RoHS Compliant Products” on Page 4.**
- 19) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 20) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
- 21) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MR, A12 = “0”) a fast power-down exit timing t_{XARD} can be used. In “low active power-down mode” (MR, A12 = “1”) a slow power-down exit timing t_{XARDS} has to be satisfied.
- 22) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where $WR_{MIN}[\text{cycles}] = t_{WR}(\text{ns})/t_{CK}(\text{ns})$ rounded up to the next integer value. $t_{DAL} = WR + (t_{RP}/t_{CK})$. For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.



3.3.3 ODT AC Electrical Characteristics

TABLE 15
ODT AC Characteristics and Operating Conditions for DDR2-667

| Symbol | Parameter / Condition | Values | | Unit | Note |
|-------------|--------------------------------------|-----------------------------|--|----------|------|
| | | Min. | Max. | | |
| t_{AOND} | ODT turn-on delay | 2 | 2 | n_{CK} | 1) |
| t_{AON} | ODT turn-on | $t_{AC.MIN}$ | $t_{AC.MAX} + 0.7 \text{ ns}$ | ns | 1)2) |
| t_{AONPD} | ODT turn-on (Power-Down Modes) | $t_{AC.MIN} + 2 \text{ ns}$ | $2 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$ | ns | 1) |
| t_{AOFD} | ODT turn-off delay | 2.5 | 2.5 | n_{CK} | 1) |
| t_{AOF} | ODT turn-off | $t_{AC.MIN}$ | $t_{AC.MAX} + 0.6 \text{ ns}$ | ns | 1)3) |
| t_{AOFPD} | ODT turn-off (Power-Down Modes) | $t_{AC.MIN} + 2 \text{ ns}$ | $2.5 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$ | ns | 1) |
| t_{ANPD} | ODT to Power Down Mode Entry Latency | 3 | — | n_{CK} | 1) |
| t_{AXPD} | ODT Power Down Exit Latency | 8 | — | n_{CK} | 1) |

- 1) New units, " $t_{CK.AVG}$ " and " n_{CK} ", are introduced in DDR2-667 and DDR2-800. Unit " $t_{CK.AVG}$ " represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit " n_{CK} " represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, " t_{CK} " is used for both concepts. Example: $t_{XP} = 2 [n_{CK}]$ means; if Power Down exit is registered at T_m , an Active command may be registered at $T_m + 2$, even if $(T_m + 2 - T_m)$ is $2 \times t_{CK.AVG} + t_{ERR.2PER(Min)}$.
- 2) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND} , which is interpreted differently per speed bin. For DDR2-667/800, t_{AOND} is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.
- 3) ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD} , which is interpreted differently per speed bin. For DDR2-667/800, if $t_{CK(avg)} = 3 \text{ ns}$ is assumed, t_{AOFD} is 1.5 ns (= $0.5 \times 3 \text{ ns}$) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.



TABLE 16
ODT AC Characteristics and Operating Conditions for DDR2-533 & DDR2-400

| Symbol | Parameter / Condition | Values | | Unit | Note |
|-------------|--------------------------------------|-----------------------------|--|----------|------|
| | | Min. | Max. | | |
| t_{AOND} | ODT turn-on delay | 2 | 2 | t_{CK} | |
| t_{AON} | ODT turn-on | $t_{AC.MIN}$ | $t_{AC.MAX} + 1 \text{ ns}$ | ns | 1) |
| t_{AONPD} | ODT turn-on (Power-Down Modes) | $t_{AC.MIN} + 2 \text{ ns}$ | $2 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$ | ns | |
| t_{AOFD} | ODT turn-off delay | 2.5 | 2.5 | t_{CK} | |
| t_{AOF} | ODT turn-off | $t_{AC.MIN}$ | $t_{AC.MAX} + 0.6 \text{ ns}$ | ns | 2) |
| t_{AOFPD} | ODT turn-off (Power-Down Modes) | $t_{AC.MIN} + 2 \text{ ns}$ | $2.5 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$ | ns | |
| t_{ANPD} | ODT to Power Down Mode Entry Latency | 3 | — | t_{CK} | |
| t_{AXPD} | ODT Power Down Exit Latency | 8 | — | t_{CK} | |

- 1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND} , which is interpreted differently per speed bin. For DDR2-400/533, t_{AOND} is 10 ns (= 2 x 5 ns) after the clock edge that registered a first ODT HIGH if $t_{CK} = 5 \text{ ns}$.
- 2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD} . Both are measured from t_{AOF} , which is interpreted differently per speed bin. For DDR2-400/533, t_{AOFD} is 12.5 ns (= 2.5 x 5 ns) after the clock edge that registered a first ODT HIGH if $t_{CK} = 5 \text{ ns}$.

3.4 Currents Specifications and Conditions

TABLE 17
 I_{DD} Measurement Conditions

| Parameter | Symbol | Note 1)2)3)4)5)6) |
|---|------------|----------------------|
| Operating Current 0 One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, CKE is HIGH, \overline{CS} is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING. | I_{DD0} | |
| Operating Current 1 One bank Active - Read - Precharge; $I_{OUT} = 0 \text{ mA}$, $BL = 4$, $t_{CK} = t_{CK.MIN}$, $t_{RC} = t_{RC.MIN}$, $t_{RAS} = t_{RAS.MIN}$, $t_{RCD} = t_{RCD.MIN}$, $AL = 0$, $CL = CL_{MIN}$; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING. | I_{DD1} | |
| Precharge Standby Current All banks idle; \overline{CS} is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING. | I_{DD2N} | |
| Precharge Power-Down Current Other control and address inputs are STABLE, Data bus inputs are FLOATING. | I_{DD2P} | |
| Precharge Quiet Standby Current All banks idle; \overline{CS} is HIGH; CKE is HIGH; $t_{CK} = t_{CK.MIN}$; Other control and address inputs are STABLE, Data bus inputs are FLOATING. | I_{DD2Q} | |



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| Parameter | Symbol | Note 1)2)3)4)5)6) |
|--|---------------|----------------------|
| Active Standby Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CL _{MIN} ; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MIN}$; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; $I_{OUT} = 0$ mA. | I_{DD3N} | |
| Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit); | $I_{DD3P(0)}$ | |
| Active Power-Down Current All banks open; $t_{CK} = t_{CK.MIN}$, CKE is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit); | $I_{DD3P(1)}$ | |
| Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CL _{MIN} ; $t_{CK} = t_{CK.MIN}$; $t_{RAS} = t_{RAS.MAX}$, $t_{RP} = t_{RP.MAX}$; CKE is HIGH, \overline{CS} is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; | I_{DD4W} | |
| Burst Refresh Current $t_{CK} = t_{CK.MIN}$, Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, CKE is HIGH, \overline{CS} is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING. | I_{DD5B} | |
| Distributed Refresh Current $t_{CK} = t_{CK.MIN}$, Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and \overline{CS} is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING. | I_{DD5D} | |
| Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and \overline{CK} at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. I_{DD6} current values are guaranteed up to T_{CASE} of 85 °C max. | I_{DD6} | |
| All Bank Interleave Read Current All banks are being interleaved at minimum t_{RC} without violating t_{RRD} using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. $I_{out} = 0$ mA. | I_{DD7} | |

- 1) $V_{DDQ} = 1.8\text{ V} \pm 0.1\text{ V}$; $V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$
- 2) I_{DD} specifications are tested after the device is properly initialized and I_{DD} parameter are specified with ODT disabled.
- 3) Definitions for I_{DD} see **Table 18**
- 4) I_{DD1} , I_{DD4R} and I_{DD7} current measurements are defined with the outputs disabled ($I_{OUT} = 0$ mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.
- 5) For two rank modules: for all active current measurements the other rank is in Precharge Power-Down Mode I_{DD2P}
- 6) For details and notes see the relevant Qimonda component data sheet

TABLE 18
Definitions for I_{DD}

| Parameter | Description |
|-----------|--|
| LOW | $V_{IN} \leq V_{IL(ac).MAX}$, HIGH is defined as $V_{IN} \geq V_{IH(ac).MIN}$ |
| STABLE | inputs are stable at a HIGH or LOW level |
| FLOATING | inputs are $V_{REF} = V_{DDQ}/2$ |
| SWITCHING | inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes |



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TABLE 19
I_{DD} Specification for HYS72T[128/256]00xHR-[3S/3.7/5]-A

| Product Type | HYS72T256000HR-3S-A | HYS72T256000HR-3.7-A | HYS72T128001HR-5-A | HYS72T256000HR-5-A | Unit | Note ¹⁾ |
|--------------------------------|---------------------|----------------------|--------------------|--------------------|------|--------------------|
| Organization | 2 GByte | 2 GByte | 1 GByte | 2 GByte | | |
| | 1 Rank | 1 Rank | 1 Rank | 1 Rank | | |
| | ×72 | ×72 | ×72 | ×72 | | |
| | -3S | -3.7 | -5 | -5 | | |
| Symbol | Max. | Max. | Max. | Max. | | |
| <i>I</i> _{DD0} | 2130 | 1850 | 910 | 1670 | mA | 2) |
| <i>I</i> _{DD1} | 2490 | 2030 | 1000 | 1850 | mA | 2) |
| <i>I</i> _{DD2N} | 1680 | 1330 | 590 | 1040 | mA | 3) |
| <i>I</i> _{DD2P} | 720 | 630 | 340 | 530 | mA | 3) |
| <i>I</i> _{DD2Q} | 1320 | 910 | 530 | 910 | mA | 3) |
| <i>I</i> _{DD3N} | 1770 | 1400 | 640 | 1130 | mA | 3) |
| <i>I</i> _{DD3P.MRS=0} | 470 | 860 | 440 | 910 | mA | 3)4) |
| <i>I</i> _{DD3P.MRS=1} | 720 | 660 | 360 | 730 | mA | 3)5) |
| <i>I</i> _{DD4R} | 4200 | 3100 | 1310 | 2480 | mA | 2) |
| <i>I</i> _{DD4W} | 4200 | 3020 | 1270 | 2390 | mA | 2) |
| <i>I</i> _{DD5B} | 4200 | 3830 | 1900 | 3650 | mA | 2) |
| <i>I</i> _{DD5D} | 720 | 680 | 370 | 590 | mA | 3)6) |
| <i>I</i> _{DD6} | 108 | 144 | 72 | 144 | mA | 3)6) |
| <i>I</i> _{DD7} | 5190 | 4640 | 2120 | 4100 | mA | 3) |

- 1) Module *I*_{DD} is calculated on the basis of component *I*_{DD} and includes currents of Registers and PLL. ODT disabled. *I*_{DD1}, *I*_{DD4R} and *I*_{DD7} are defined with the outputs disabled.
- 2) The other rank is in IDD2P Percharge Power-Down mode
- 3) Both ranks are in the same IDD current mode
- 4) Fast: MRS(12)=0
- 5) Slow: MRS(12)=1
- 6) Values for 0 °C ≤ *T*_{CASE} ≤ 85 °C



4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

List of SPD Code Tables

- Table 20 “HYS72T[128/256]00xHR-[3S/3.7/5]-A” on Page 30

TABLE 20

HYS72T[128/256]00xHR-[3S/3.7/5]-A

| Product Type | | HYS72T256000HR-3S-A | HYS72T256000HR-3.7-A | HYS72T128001HR-5-A | HYS72T256000HR-5-A |
|--------------------|--|---------------------|----------------------|--------------------|--------------------|
| Organization | | 2 GByte | 2 GByte | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×4) | 1 Rank (×4) | 1 Rank (×8) | 1 Rank (×4) |
| Label Code | | PC2-5300R-555 | PC2-4200R-444 | PC2-3200R-333 | PC2-3200R-333 |
| JEDEC SPD Revision | | Rev. 1.2 | Rev. 1.1 | Rev. 1.2 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 0 | Programmed SPD Bytes in EEPROM | 80 | 80 | 80 | 80 |
| 1 | Total number of Bytes in EEPROM | 08 | 08 | 08 | 08 |
| 2 | Memory Type (DDR2) | 08 | 08 | 08 | 08 |
| 3 | Number of Row Addresses | 0E | 0E | 0E | 0E |
| 4 | Number of Column Addresses | 0B | 0B | 0A | 0B |
| 5 | DIMM Rank and Stacking Information | 60 | 60 | 60 | 60 |
| 6 | Data Width | 48 | 48 | 48 | 48 |
| 7 | Not used | 00 | 00 | 00 | 00 |
| 8 | Interface Voltage Level | 05 | 05 | 05 | 05 |
| 9 | $t_{CK} @ CL_{MAX}$ (Byte 18) [ns] | 30 | 3D | 50 | 50 |
| 10 | t_{AC} SDRAM @ CL_{MAX} (Byte 18) [ns] | 45 | 50 | 60 | 60 |
| 11 | Error Correction Support (non-ECC, ECC) | 02 | 02 | 02 | 02 |
| 12 | Refresh Rate and Type | 82 | 82 | 82 | 82 |
| 13 | Primary SDRAM Width | 04 | 04 | 08 | 04 |



HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

| Product Type | | HYS72T256000HR-3S-A | HYS72T256000HR-3.7-A | HYS72T128001HR-5-A | HYS72T256000HR-5-A |
|--------------------|---------------------------------------|---------------------|----------------------|--------------------|--------------------|
| Organization | | 2 GByte | 2 GByte | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×4) | 1 Rank (×4) | 1 Rank (×8) | 1 Rank (×4) |
| Label Code | | PC2-5300R-555 | PC2-4200R-444 | PC2-3200R-333 | PC2-3200R-333 |
| JEDEC SPD Revision | | Rev. 1.2 | Rev. 1.1 | Rev. 1.2 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 14 | Error Checking SDRAM Width | 04 | 04 | 08 | 04 |
| 15 | Not used | 00 | 00 | 00 | 00 |
| 16 | Burst Length Supported | 0C | 0C | 0C | 0C |
| 17 | Number of Banks on SDRAM Device | 08 | 08 | 08 | 08 |
| 18 | Supported CAS Latencies | 38 | 38 | 38 | 38 |
| 19 | DIMM Mechanical Characteristics | 01 | 00 | 00 | 00 |
| 20 | DIMM Type Information | 01 | 01 | 01 | 01 |
| 21 | DIMM Attributes | 05 | 05 | 04 | 05 |
| 22 | Component Attributes | 03 | 01 | 01 | 01 |
| 23 | $t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns] | 3D | 3D | 50 | 50 |
| 24 | t_{AC} SDRAM @ $CL_{MAX} -1$ [ns] | 50 | 50 | 60 | 60 |
| 25 | $t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns] | 50 | 50 | 50 | 50 |
| 26 | t_{AC} SDRAM @ $CL_{MAX} -2$ [ns] | 60 | 60 | 60 | 60 |
| 27 | $t_{RP.MIN}$ [ns] | 3C | 3C | 3C | 3C |
| 28 | $t_{RRD.MIN}$ [ns] | 1E | 1E | 1E | 1E |
| 29 | $t_{RCD.MIN}$ [ns] | 3C | 3C | 3C | 3C |
| 30 | $t_{RAS.MIN}$ [ns] | 2D | 2D | 28 | 28 |
| 31 | Module Density per Rank | 02 | 02 | 01 | 02 |
| 32 | $t_{AS.MIN}$ and $t_{CS.MIN}$ [ns] | 20 | 25 | 35 | 35 |
| 33 | $t_{AH.MIN}$ and $t_{CH.MIN}$ [ns] | 27 | 37 | 47 | 47 |
| 34 | $t_{DS.MIN}$ [ns] | 10 | 10 | 15 | 15 |
| 35 | $t_{DH.MIN}$ [ns] | 17 | 22 | 27 | 27 |
| 36 | $t_{WR.MIN}$ [ns] | 3C | 3C | 3C | 3C |
| 37 | $t_{WTR.MIN}$ [ns] | 1E | 1E | 28 | 28 |
| 38 | $t_{RTP.MIN}$ [ns] | 1E | 1E | 1E | 1E |
| 39 | Analysis Characteristics | 00 | 00 | 00 | 00 |



HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

| Product Type | | HYS72T256000HR-3S-A | HYS72T256000HR-3.7-A | HYS72T128001HR-5-A | HYS72T256000HR-5-A |
|--------------------|--|---------------------|----------------------|--------------------|--------------------|
| Organization | | 2 GByte | 2 GByte | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×4) | 1 Rank (×4) | 1 Rank (×8) | 1 Rank (×4) |
| Label Code | | PC2-5300R-555 | PC2-4200R-444 | PC2-3200R-333 | PC2-3200R-333 |
| JEDEC SPD Revision | | Rev. 1.2 | Rev. 1.1 | Rev. 1.2 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 40 | t_{RC} and t_{RFC} Extension | 06 | 06 | 06 | 06 |
| 41 | $t_{RC.MIN}$ [ns] | 3C | 3C | 37 | 37 |
| 42 | $t_{RFC.MIN}$ [ns] | 7F | 7F | 7F | 7F |
| 43 | $t_{CK.MAX}$ [ns] | 80 | 80 | 80 | 80 |
| 44 | $t_{DQSQ.MAX}$ [ns] | 18 | 1E | 23 | 23 |
| 45 | $t_{QHS.MAX}$ [ns] | 22 | 28 | 2D | 2D |
| 46 | PLL Relock Time | 0F | 0F | 0F | 0F |
| 47 | $T_{CASE.MAX}$ Delta / ΔT_{4R4W} Delta | 50 | 51 | 51 | 51 |
| 48 | Psi(T-A) DRAM | 58 | 60 | 60 | 60 |
| 49 | ΔT_0 (DT0) | 37 | 37 | 33 | 33 |
| 50 | ΔT_{2N} (DT2N, UDIMM) or ΔT_{2Q} (DT2Q, RDIMM) | 21 | 1D | 1A | 1A |
| 51 | ΔT_{2P} (DT2P) | 21 | 23 | 23 | 23 |
| 52 | ΔT_{3N} (DT3N) | 24 | 1E | 18 | 18 |
| 53 | $\Delta T_{3P.fast}$ (DT3P fast) | 23 | 1F | 18 | 18 |
| 54 | $\Delta T_{3P.slow}$ (DT3P slow) | 17 | 16 | 16 | 16 |
| 55 | ΔT_{4R} (DT4R) / ΔT_{4R4W} Sign (DT4R4W) | 4A | 43 | 35 | 35 |
| 56 | ΔT_{5B} (DT5B) | 21 | 22 | 21 | 21 |
| 57 | ΔT_7 (DT7) | 28 | 2A | 25 | 25 |
| 58 | Psi(ca) PLL | C4 | C4 | C4 | C4 |
| 59 | Psi(ca) REG | 8C | 8C | 8C | 8C |
| 60 | ΔT_{PLL} (DTPLL) | 68 | 61 | 59 | 59 |
| 61 | ΔT_{REG} (DTREG) / Toggle Rate | 94 | 78 | 5C | 5C |
| 62 | SPD Revision | 12 | 11 | 12 | 11 |
| 63 | Checksum of Bytes 0-62 | 8F | A4 | D8 | D2 |
| 64 | Manufacturer's JEDEC ID Code (1) | 7F | 7F | 7F | 7F |
| 65 | Manufacturer's JEDEC ID Code (2) | 7F | 7F | 7F | 7F |



HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

| Product Type | | HYS72T256000HR-3S-A | HYS72T256000HR-3.7-A | HYS72T128001HR-5-A | HYS72T256000HR-5-A |
|--------------------|----------------------------------|---------------------|----------------------|--------------------|--------------------|
| Organization | | 2 GByte | 2 GByte | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×4) | 1 Rank (×4) | 1 Rank (×8) | 1 Rank (×4) |
| Label Code | | PC2-5300R-555 | PC2-4200R-444 | PC2-3200R-333 | PC2-3200R-333 |
| JEDEC SPD Revision | | Rev. 1.2 | Rev. 1.1 | Rev. 1.2 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 66 | Manufacturer's JEDEC ID Code (3) | 7F | 7F | 7F | 7F |
| 67 | Manufacturer's JEDEC ID Code (4) | 7F | 7F | 7F | 7F |
| 68 | Manufacturer's JEDEC ID Code (5) | 7F | 7F | 7F | 7F |
| 69 | Manufacturer's JEDEC ID Code (6) | 51 | 51 | 51 | 51 |
| 70 | Manufacturer's JEDEC ID Code (7) | 00 | 00 | 00 | 00 |
| 71 | Manufacturer's JEDEC ID Code (8) | 00 | 00 | 00 | 00 |
| 72 | Module Manufacturer Location | xx | xx | xx | xx |
| 73 | Product Type, Char 1 | 37 | 37 | 37 | 37 |
| 74 | Product Type, Char 2 | 32 | 32 | 32 | 32 |
| 75 | Product Type, Char 3 | 54 | 54 | 54 | 54 |
| 76 | Product Type, Char 4 | 32 | 32 | 31 | 32 |
| 77 | Product Type, Char 5 | 35 | 35 | 32 | 35 |
| 78 | Product Type, Char 6 | 36 | 36 | 38 | 36 |
| 79 | Product Type, Char 7 | 30 | 30 | 30 | 30 |
| 80 | Product Type, Char 8 | 30 | 30 | 30 | 30 |
| 81 | Product Type, Char 9 | 30 | 30 | 31 | 30 |
| 82 | Product Type, Char 10 | 48 | 48 | 48 | 48 |
| 83 | Product Type, Char 11 | 52 | 52 | 52 | 52 |
| 84 | Product Type, Char 12 | 33 | 33 | 35 | 35 |
| 85 | Product Type, Char 13 | 53 | 2E | 41 | 41 |
| 86 | Product Type, Char 14 | 41 | 37 | 20 | 20 |
| 87 | Product Type, Char 15 | 20 | 41 | 20 | 20 |
| 88 | Product Type, Char 16 | 20 | 20 | 20 | 20 |
| 89 | Product Type, Char 17 | 20 | 20 | 20 | 20 |
| 90 | Product Type, Char 18 | 20 | 20 | 20 | 20 |
| 91 | Module Revision Code | 5x | 5x | 3x | 5x |



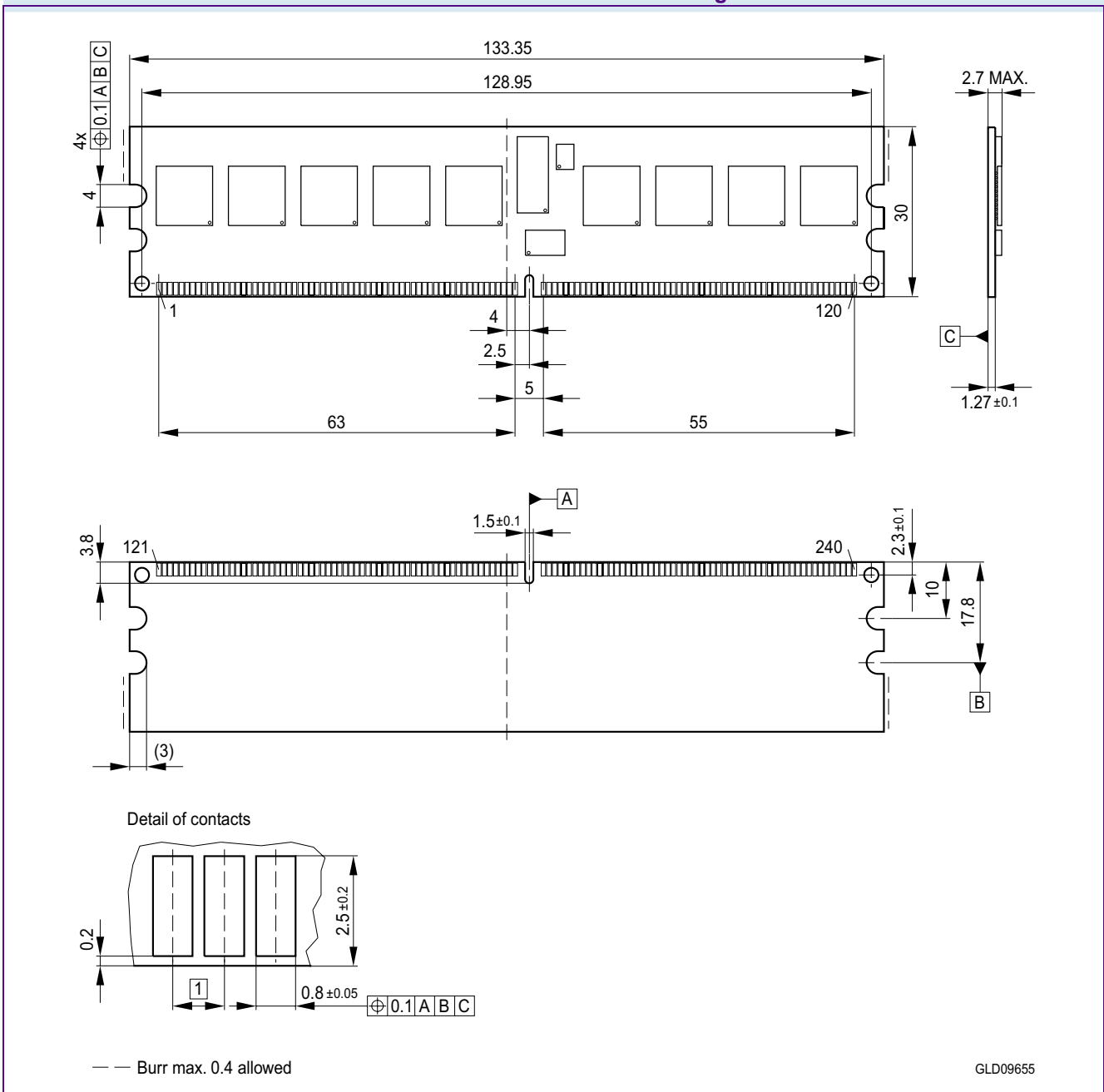
HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

| | | | | | |
|---------------------------|--------------------------------|---------------------|----------------------|--------------------|--------------------|
| Product Type | | HYS72T256000HR-3S-A | HYS72T256000HR-3.7-A | HYS72T128001HR-5-A | HYS72T256000HR-5-A |
| Organization | | 2 GByte | 2 GByte | 1 GByte | 2 GByte |
| | | ×72 | ×72 | ×72 | ×72 |
| | | 1 Rank (×4) | 1 Rank (×4) | 1 Rank (×8) | 1 Rank (×4) |
| Label Code | | PC2-5300R-555 | PC2-4200R-444 | PC2-3200R-333 | PC2-3200R-333 |
| JEDEC SPD Revision | | Rev. 1.2 | Rev. 1.1 | Rev. 1.2 | Rev. 1.1 |
| Byte# | Description | HEX | HEX | HEX | HEX |
| 92 | Test Program Revision Code | xx | xx | xx | xx |
| 93 | Module Manufacturing Date Year | xx | xx | xx | xx |
| 94 | Module Manufacturing Date Week | xx | xx | xx | xx |
| 95 - 98 | Module Serial Number | xx | xx | xx | xx |
| 99 - 127 | Not used | 00 | 00 | 00 | 00 |
| 128 - 255 | Blank for customer use | FF | FF | FF | FF |



5 Package Outlines

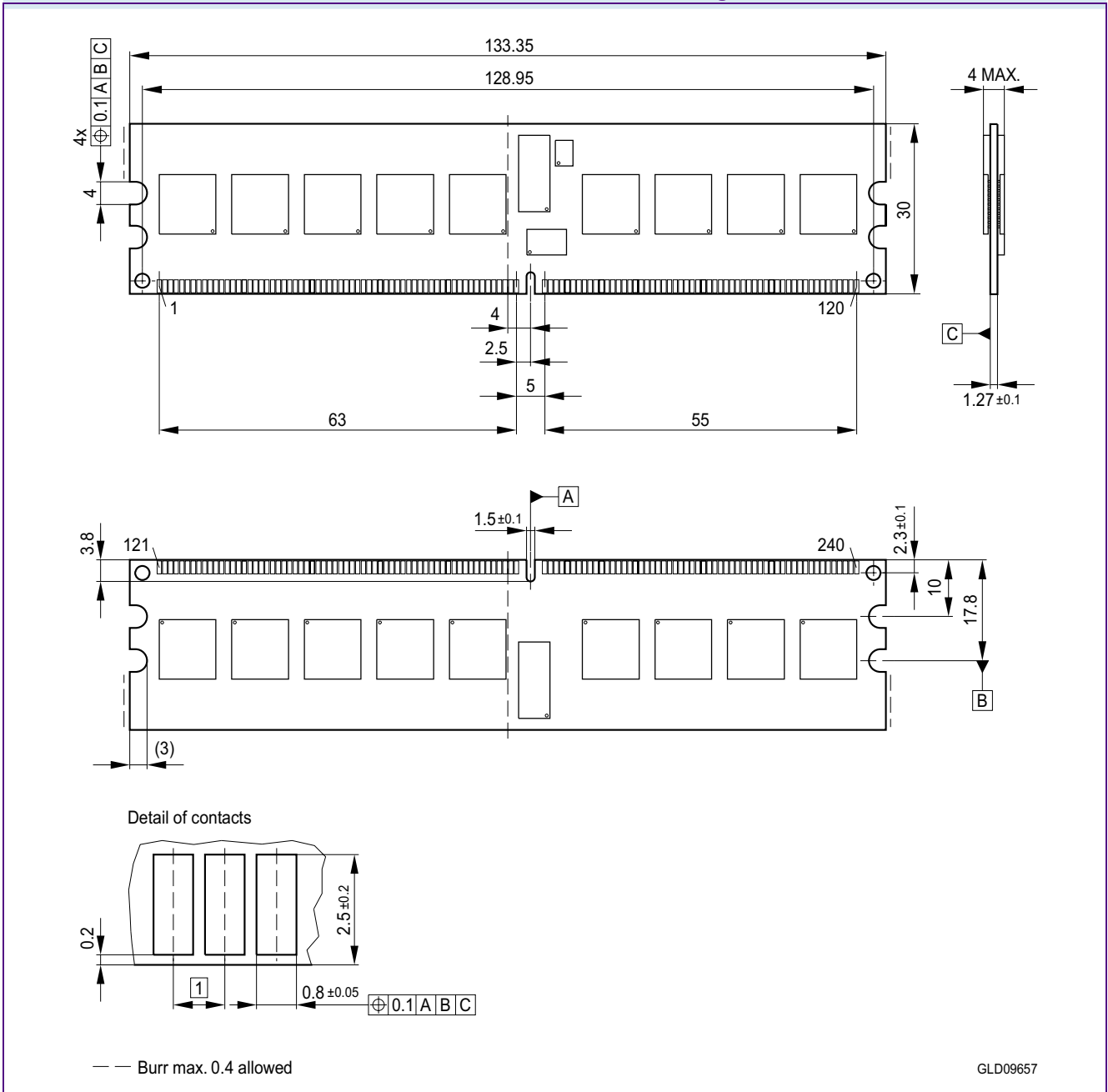
FIGURE 5
Package Outline Raw Card A L-DIM-240-11





HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

FIGURE 6
Package Outline Raw Card C L-DIM-240-13





6 Product Type Nomenclature (DDR2 DRAMs and DIMMs)

Qimonda's nomenclature uses simple coding combined with some proprietary coding. **Table 21** provides examples for module and component product type number as well as the

field number. The detailed field description together with possible values and coding explanation is listed for modules in **Table 22** and for components in **Table 23**.

TABLE 21
Nomenclature Fields and Examples

| Example for | Field Number | | | | | | | | | | |
|-------------|--------------|----|---|--------|----|---|---|---|---|----|----|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| Micro-DIMM | HYS | 64 | T | 64/128 | 0 | 2 | 0 | K | M | -5 | -A |
| DDR2 DRAM | HYB | 18 | T | 512/1G | 16 | | 0 | A | C | -5 | — |

TABLE 22
DDR2 DIMM Nomenclature

| Field | Description | Values | Coding |
|-------|--|---------|----------------|
| 1 | Qimonda Module Prefix | HYS | Constant |
| 2 | Module Data Width [bit] | 64 | Non-ECC |
| | | 72 | ECC |
| 3 | DRAM Technology | T | DDR2 |
| 4 | Memory Density per I/O [Mbit]; Module Density ¹⁾ | 32 | 256 MByte |
| | | 64 | 512 MByte |
| | | 128 | 1 GByte |
| | | 256 | 2 GByte |
| | | 512 | 4 GByte |
| 5 | Raw Card Generation | 0 .. 9 | Look up table |
| 6 | Number of Module Ranks | 0, 2, 4 | 1, 2, 4 |
| 7 | Product Variations | 0 .. 9 | Look up table |
| 8 | Package, Lead-Free Status | A .. Z | Look up table |
| 9 | Module Type | D | SO-DIMM |
| | | M | Micro-DIMM |
| | | R | Registered |
| | | U | Unbuffered |
| | | F | Fully Buffered |



HYS72T[128/256]00xHR-[3S/3.7/5]-A
Registered DDR2 SDRAM Modules

| Field | Description | Values | Coding |
|-------|--------------|--------|----------------|
| 10 | Speed Grade | -2.5F | PC2-6400 5-5-5 |
| | | -2.5 | PC2-6400 6-6-6 |
| | | -3 | PC2-5300 4-4-4 |
| | | -3S | PC2-5300 5-5-5 |
| | | -3.7 | PC2-4200 4-4-4 |
| | | -5 | PC2-3200 3-3-3 |
| 11 | Die Revision | -A | First |
| | | -B | Second |

1) Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column “Coding”.

TABLE 23
DDR2 DRAM Nomenclature

| Field | Description | Values | Coding |
|-------|---------------------------|--------|-----------------------|
| 1 | Qimonda Component Prefix | HYB | Constant |
| 2 | Interface Voltage [V] | 18 | SSTL_18 |
| 3 | DRAM Technology | T | DDR2 |
| 4 | Component Density [Mbit] | 256 | 256 Mbit |
| | | 512 | 512 Mbit |
| | | 1G | 1 Gbit |
| | | 2G | 2 Gbit |
| 5+6 | Number of I/Os | 40 | ×4 |
| | | 80 | ×8 |
| | | 16 | ×16 |
| 7 | Product Variations | 0 .. 9 | Look up table |
| 8 | Die Revision | A | First |
| | | B | Second |
| 9 | Package, Lead-Free Status | C | FBGA, lead-containing |
| | | F | FBGA, lead-free |
| 10 | Speed Grade | -25F | DDR2-800 5-5-5 |
| | | -2.5 | DDR2-800 6-6-6 |
| | | -3 | DDR2-667 4-4-4 |
| | | -3S | DDR2-667 5-5-5 |
| | | -3.7 | DDR2-533 4-4-4 |
| | | -5 | DDR2-400 3-3-3 |



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