

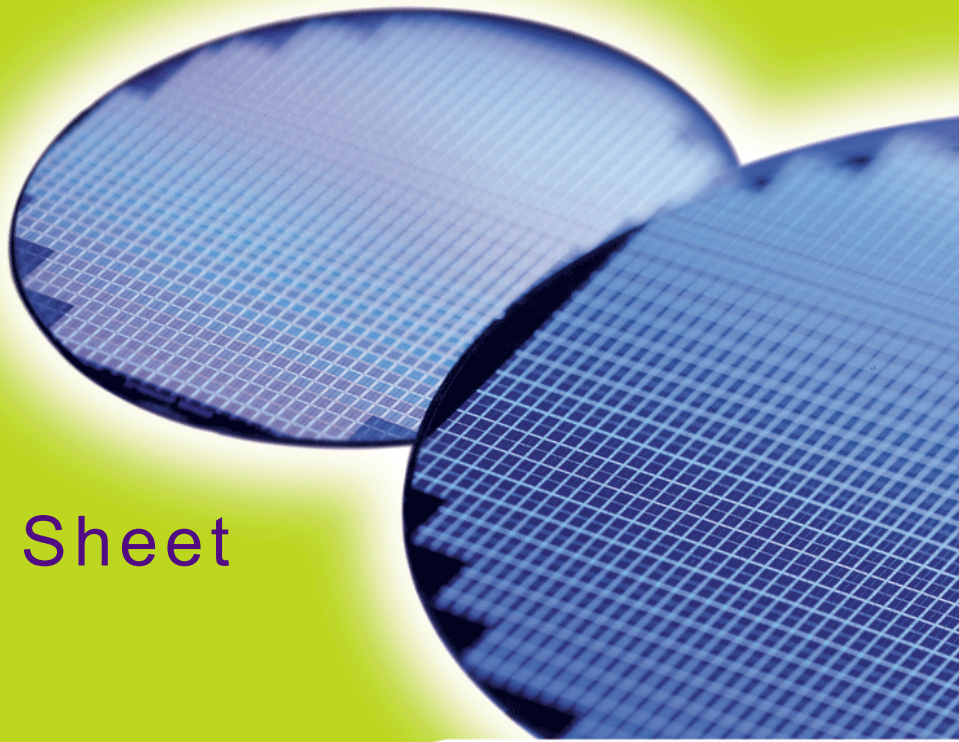
HYS72T64000HP-[3S/3.7]-A  
HYS72T1280x0HP-[3S/3.7]-A  
HYS72T256220HP-[3S/3.7]-A  
HYS72T256040HP-[3S/3.7]-A

*240-Pin Registered DDR2 SDRAM Modules*

*DDR2 SDRAM*

*RDIMM SDRAM*

*RoHS Compliant*



## Internet Data Sheet

*Rev. 1.02*

HYS72T[64/128/256]xx0HP-[3S/3.7]-A  
Registered DDR2 SDRAM Modules

HYS72T64000HP-[3S/3.7]-A, HYS72T1280x0HP-[3S/3.7]-A, HYS72T256220HP-[3S/3.7]-A, HYS72T256040HP-[3S/3.7]-A	
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# 1 Overview

This chapter gives an overview of the 1.8 V 240-Pin Registered DDR2 SDRAM Modules with parity bit product family and describes its main characteristics.

## 1.1 Features

- 240-Pin PC2–5300 and PC2–4200 DDR2 SDRAM memory modules.
- One rank 64M ×72, 128M ×72, and two ranks 128M ×72, 256M ×72, and four rank 256M ×72 module organization and 64M ×8, 128M ×4 chip organization
- Registered DIMM Parity bit for address and control bus
- 512 MB, 1 GB, and 2 GB module built with 512 Mbit DDR2 SDRAMs in P-TFBGA-60 chipsize packages.
- Standard Double-Data-Rate-Two Synchronous DRAMs (DDR2 SDRAM) with a single + 1.8 V (± 0.1 V) power supply
- All speed grades faster than DDR2–400 comply with DDR2–400 timing specifications.
- Programmable CAS Latencies (3, 4, 5, 6), Burst Length (4 & 8)
- Auto Refresh (CBR) and Self Refresh
- Programmable self refresh rate via EMRS2 setting
- Programmable partial array refresh via EMRS2 settings
- DCC enabling via EMRS2 setting
- All inputs and outputs SSTL\_18 compatible
- Off-Chip Driver Impedance Adjustment (OCD) and On-Die Termination (ODT)
- Serial Presence Detect with E<sup>2</sup>PROM
- RDIMM Dimensions (nominal): 30 mm high, 133.35 mm wide
- Based on standard reference card layouts Raw Card “G”, “H”, “J”, “N” and “F”
- RoHS compliant products<sup>1)</sup>

**TABLE 1**  
Performance Table

Product Type Speed Code			-3S	-3.7	Unit
DRAM Speed Grade			DDR2–667D	DDR2–533C	
Module Speed Grade			PC2–5300	PC2–4200	
CAS-RCD-RP latencies			5-5-5	4-4-4	$t_{CK}$
Max. Clock Frequency	@CL5	$f_{CK5}$	333	266	MHz
	@CL4	$f_{CK4}$	266	266	MHz
	@CL3	$f_{CK3}$	200	200	MHz
Min. RAS-CAS-Delay		$t_{RCD}$	15	15	ns
Min. Row Precharge Time		$t_{RP}$	15	15	ns
Min. Row Active Time		$t_{RAS}$	45	45	ns
Min. Row Cycle Time		$t_{RC}$	60	60	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.



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Registered DDR2 SDRAM Modules

## 1.2 Description

The Qimonda HYS72T[64/128/256]xx0HP-[3S/3.7]-A module family are Registered DIMM (with parity) modules with 30 mm height based on DDR2 technology.

DIMMs are available as ECC modules in 64M × 72 (512 MB), 128M × 72 (1 GB), 256M × 72 (2GB) organization and density, intended for mounting into 240-Pin connector sockets.

The memory array is designed with 512-Mbit Double-Data-Rate-Two (DDR2) Synchronous DRAMs. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces

capacitive loading to the system bus, but adds one cycle to the SDRAM timing. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E2PROM device using the 2-pin I2C protocol. The first 128 bytes are programmed with configuration data and the second 128 bytes are available to the customer.



**TABLE 2**  
Ordering Information for RoHS Compliant Products

Product Type <sup>1)</sup>	Compliance Code <sup>2)</sup>	Description	SDRAM Technology
<b>PC2-5300-555</b>			
HYS72T64000HP-3S-A	512 MB 1Rx8 PC2-5300P-555-12-F0	1 Rank ECC	512 Mbit (×8)
HYS72T128000HP-3S-A	1 GB 1Rx4 PC2-5300P-555-12-H0	1 Rank ECC	512 Mbit (×4)
HYS72T128020HP-3S-A	1 GB 2Rx8 PC2-5300P-555-12-G0	2 Ranks, ECC	512 Mbit (×8)
HYS72T256220HP-3S-A	2 GB 2Rx4 PC2-5300P-555-12-J2	2 Ranks, ECC	512 Mbit (×4)
HYS72T256040HP-3S-A	2 GB 4Rx8 PC2-5300P-555-12-N0	4 Ranks, ECC	512 Mbit (×8)
<b>PC2-4200-444</b>			
HYS72T64000HP-3.7-A	512 MB 1Rx8 PC2-4200P-444-12-F0	1 Rank ECC	512 Mbit (×8)
HYS72T128000HP-3.7-A	1 GB 1Rx4 PC2-4200P-444-12-H0	1 Rank ECC	512 Mbit (×4)
HYS72T128020HP-3.7-A	1 GB 2Rx8 PC2-4200P-444-12-G0	2 Ranks, ECC	512 Mbit (×8)
HYS72T256220HP-3.7-A	2 GB 2Rx4 PC2-4200P-444-12-J2	2 Ranks, ECC	512 Mbit (×4)
HYS72T256040HP-3.7-A	2 GB 4Rx8 PC2-5300P-555-12-N0	4 Ranks, ECC	512 Mbit (×8)

- 1) All Product Type number end with a place code, designating the silicon die revision. Example: HYS72T64000HP-3.7-A, indicating Rev. "B" dies are used for DDR2 SDRAM components. For all Qimonda DDR2 module and component nomenclature see **Chapter 6** of this data sheet.
- 2) The Compliance Code is printed on the module label and describes the speed grade, for example "PC2-4200R-444-12-R0", where 4200P means Registered DIMM modules (with Parity Bit) with 4.26 GB/sec Module Bandwidth and "444-12" means Column Address Strobe (CAS) latency = 4, Row Column Delay (RCD) latency = 4 and Row Precharge (RP) latency = 4 using the latest JEDEC SPD Revision 1.2 and produced on the Raw Card "R"

**TABLE 3**  
Address Format Table

DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/column bits	Raw Card
512 MB	64M × 72	1	ECC	9	14/2/10	F
1 GB	128M × 72	1	ECC	18	14/2/11	H
1 GB	128M × 72	2	ECC	18	14/2/10	G

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DIMM Density	Module Organization	Memory Ranks	ECC/ Non-ECC	# of SDRAMs	# of row/bank/column bits	Raw Card
2 GB	256M ×72	2	ECC	36	14/2/11	J
2 GB	256M ×72	4	ECC	36	14/2/10	N

**TABLE 4**  
Components on Modules

Product Type <sup>1)</sup>	DRAM Components <sup>1)2)</sup>	DRAM Density	DRAM Organisation
HYS72T64000HP	HYB18T512800AF	512 Mbit	64M × 8
HYS72T128000HP	HYB18T512400AF	512 Mbit	128M × 4
HYS72T128020HP	HYB18T512800AF	512 Mbit	64M × 8
HYS72T256220HP	HYB18T512400AF	512 Mbit	128M × 4
HYS72T256040HP	HYB18T512800AF	512 Mbit	64M × 8

1) Green Product

2) For a detailed description of all functionalities of the DRAM components on these modules see the component data sheet.



## 2 Pin Configuration

This chapter contains the pin configuration and block diagrams.

### 2.1 Pin Configuration

The pin configuration of the Registered DDR2 SDRAM DIMM is listed by function in **Table 5** (240 pins). The abbreviations used in columns Pin and Buffer Type are explained in **Table 6** and **Table 7** respectively. The pin numbering is depicted in **Figure 1**.

**TABLE 5**  
Pin Configuration of RDIMM

Pin No.	Name	Pin Type	Buffer Type	Function
<b>Clock Signals</b>				
185	CK0	I	SSTL	<b>Clock Signal CK0, Complementary Clock Signal CK0</b>
186	$\overline{\text{CK0}}$	I	SSTL	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of $\overline{\text{CK}}$ . A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
52	CKE0	I	SSTL	<b>Clock Enables 1:0</b>
171	CKE1	I	SSTL	Activates the DDR2 SDRAM CK signal when HIGH and deactivates the CK signal when LOW. By deactivating the clocks, CKE0 initiates the Power Down Mode or the Self Refresh Mode. <i>Note: 2-Ranks module</i>
	NC	NC	—	<b>Not Connected</b> <i>Note: 1-Rank module</i>
<b>Control Signals</b>				
193	$\overline{\text{S0}}$	I	SSTL	<b>Chip Select</b>
76	$\overline{\text{S1}}$	I	SSTL	Enables the associated DDR2 SDRAM command decoder when LOW and disables the command decoder when HIGH. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{\text{S0}}$ Rank 1 is selected by $\overline{\text{S1}}$ The input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When $\overline{\text{S}}$ is HIGH, all register outputs (except CK, ODT and Chip select) remain in the previous state. <i>Note: 2-Ranks module</i>
	NC	NC	—	<b>Not Connected</b> <i>Note: 1-Rank module</i>



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Pin No.	Name	Pin Type	Buffer Type	Function
220	$\overline{S2}$	I	SSTL	Rank 2 is selected by $\overline{S2}$
	NC	NC	—	<b>Not Connected</b> <i>Note: 1-Rank, 2-Ranks module</i>
221	$\overline{S3}$	I	SSTL	Rank 3 is selected by $\overline{S3}$
	NC	NC	—	<b>Not Connected</b> <i>Note: 1-Rank, 2-Ranks module</i>
192	$\overline{RAS}$	I	SSTL	<b>Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)</b> When sampled at the cross point of the rising edge of CK, and falling edge of $\overline{CK}$ , $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed by the SDRAM.
74	$\overline{CAS}$	I	SSTL	
73	$\overline{WE}$	I	SSTL	
18	$\overline{RESET}$	I	CMOS	<b>Register Reset</b> The RESET pin is connected to the RST pin on the register and to the OE pin on the PLL. When LOW, all register outputs will be driven LOW and the PLL clocks to the DRAMs and the register(s) will be set to low-level. The PLL will remain synchronized with the input clock.
<b>Address Signals</b>				
71	BA0	I	SSTL	<b>Bank Address Bus 1:0</b> Selects internal SDRAM memory bank
190	BA1	I	SSTL	
54	BA2	I	SSTL	<b>Bank Address Bus 2</b> Greater than 512Mb DDR2 SDRAMS
	NC	I	SSTL	<b>Not Connected</b> Less than 1Gb DDR2 SDRAMS
188	A0	I	SSTL	<b>Address Bus 12:0, Address Signal 10/AutoPrecharge</b> During a Bank Activate command cycle, defines the row address when sampled at the crosspoint of the rising edge of CK and falling edge of $\overline{CK}$ . During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of CK. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is HIGH, autoprecharge is selected and BA[1:0] defines the bank to be precharged. If AP is LOW, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is HIGH, all banks will be precharged regardless of the state of BA[1:0] inputs. If AP is LOW, then BA[1:0] are used to define which bank to precharge.
183	A1	I	SSTL	
63	A2	I	SSTL	
182	A3	I	SSTL	
61	A4	I	SSTL	
60	A5	I	SSTL	
180	A6	I	SSTL	
58	A7	I	SSTL	
179	A8	I	SSTL	
177	A9	I	SSTL	
70	A10	I	SSTL	
	AP	I	SSTL	
57	A11	I	SSTL	
176	A12	I	SSTL	
196	A13	I	SSTL	<b>Address Signal 13</b>
	NC	NC	—	<b>Not Connected</b> <i>Note: Non CA parity modules based on 256 Mbit component</i>



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Pin No.	Name	Pin Type	Buffer Type	Function
174	A14	I	SSTL	<b>Address Signal 14</b> <i>Note: CA Parity module</i>
	NC	NC	—	<b>Not Connected</b> <i>Note: Non CA parity module. Less than 1 GBit per DRAM die.</i>
173	A15	I	SSTL	<b>Address Signal 14</b> <i>Note: CA Parity module</i>
	NC	NC	—	<b>Not Connected</b> <i>Note: Non CA parity module. Less than 1 GBit per DRAM die.</i>
<b>Data Signals</b>				
3	DQ0	I/O	SSTL	<b>Data Bus 63:0</b> Data Input/Output pins
4	DQ1	I/O	SSTL	
9	DQ2	I/O	SSTL	
10	DQ3	I/O	SSTL	
122	DQ4	I/O	SSTL	
123	DQ5	I/O	SSTL	
128	DQ6	I/O	SSTL	
129	DQ7	I/O	SSTL	
12	DQ8	I/O	SSTL	
13	DQ9	I/O	SSTL	
21	DQ10	I/O	SSTL	
22	DQ11	I/O	SSTL	
131	DQ12	I/O	SSTL	
132	DQ13	I/O	SSTL	
140	DQ14	I/O	SSTL	
141	DQ15	I/O	SSTL	
24	DQ16	I/O	SSTL	
25	DQ17	I/O	SSTL	
30	DQ18	I/O	SSTL	
31	DQ19	I/O	SSTL	
143	DQ20	I/O	SSTL	
144	DQ21	I/O	SSTL	
149	DQ22	I/O	SSTL	
150	DQ23	I/O	SSTL	
33	DQ24	I/O	SSTL	
34	DQ25	I/O	SSTL	
39	DQ26	I/O	SSTL	
40	DQ27	I/O	SSTL	
152	DQ28	I/O	SSTL	
153	DQ29	I/O	SSTL	
158	DQ30	I/O	SSTL	





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Pin No.	Name	Pin Type	Buffer Type	Function
159	DQ31	I/O	SSTL	<b>Data Bus 63:0</b> Data Input/Output pins
80	DQ32	I/O	SSTL	
81	DQ33	I/O	SSTL	
86	DQ34	I/O	SSTL	
87	DQ35	I/O	SSTL	
199	DQ36	I/O	SSTL	
200	DQ37	I/O	SSTL	
205	DQ38	I/O	SSTL	
206	DQ39	I/O	SSTL	
89	DQ40	I/O	SSTL	
90	DQ41	I/O	SSTL	
95	DQ42	I/O	SSTL	
96	DQ43	I/O	SSTL	
208	DQ44	I/O	SSTL	
209	DQ45	I/O	SSTL	
214	DQ46	I/O	SSTL	
215	DQ47	I/O	SSTL	
98	DQ48	I/O	SSTL	
99	DQ49	I/O	SSTL	
107	DQ50	I/O	SSTL	
108	DQ51	I/O	SSTL	
217	DQ52	I/O	SSTL	
218	DQ53	I/O	SSTL	
226	DQ54	I/O	SSTL	
227	DQ55	I/O	SSTL	
110	DQ56	I/O	SSTL	
111	DQ57	I/O	SSTL	
116	DQ58	I/O	SSTL	
117	DQ59	I/O	SSTL	
229	DQ60	I/O	SSTL	
230	DQ61	I/O	SSTL	
235	DQ62	I/O	SSTL	
236	DQ63	I/O	SSTL	
<b>Check Bits</b>				
42	CB0	I/O	SSTL	<b>Check Bits 7:0</b> Check Bit Input / Output pins <i>Note: NC on Non-ECC module</i>
43	CB1	I/O	SSTL	
48	CB2	I/O	SSTL	
49	CB3	I/O	SSTL	



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Pin No.	Name	Pin Type	Buffer Type	Function
161	CB4	I/O	SSTL	<b>Check Bits 7:0</b> Check Bit Input / Output pins <i>Note: NC on Non-ECC module</i>
162	CB5	I/O	SSTL	
167	CB6	I/O	SSTL	
168	CB7	I/O	SSTL	
<b>Data Strobe Bus</b>				
7	DQS0	I/O	SSTL	<b>Data Strobes 17:0</b> The data strobes, associated with one data byte, are sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$ . If the module is to be operated in single ended strobe mode, all DQS signals must be tied on the system board to $V_{SS}$ through a 20 $\Omega$ to 10 k $\Omega$ resistor and DDR2 SDRAM mode registers programmed appropriately. <i>Note: See block diagram for corresponding DQ signals</i>
6	$\overline{DQS0}$	I/O	SSTL	
16	DQS1	I/O	SSTL	
15	$\overline{DQS1}$	I/O	SSTL	
28	DQS2	I/O	SSTL	
27	$\overline{DQS2}$	I/O	SSTL	
37	DQS3	I/O	SSTL	
36	$\overline{DQS3}$	I/O	SSTL	
84	DQS4	I/O	SSTL	
83	$\overline{DQS4}$	I/O	SSTL	
93	DQS5	I/O	SSTL	
92	$\overline{DQS5}$	I/O	SSTL	
105	DQS6	I/O	SSTL	
104	$\overline{DQS6}$	I/O	SSTL	
114	DQS7	I/O	SSTL	
113	$\overline{DQS7}$	I/O	SSTL	
46	DQS8	I/O	SSTL	
45	$\overline{DQS8}$	I/O	SSTL	
125	DQS9	I/O	SSTL	
126	$\overline{DQS9}$	I/O	SSTL	
134	DQS10	I/O	SSTL	
135	$\overline{DQS10}$	I/O	SSTL	
146	DQS11	I/O	SSTL	
147	$\overline{DQS11}$	I/O	SSTL	
155	DQS12	I/O	SSTL	
156	$\overline{DQS12}$	I/O	SSTL	
202	DQS13	I/O	SSTL	
203	$\overline{DQS13}$	I/O	SSTL	
211	DQS14	I/O	SSTL	
212	$\overline{DQS14}$	I/O	SSTL	
223	DQS15	I/O	SSTL	
224	$\overline{DQS15}$	I/O	SSTL	
232	DQS16	I/O	SSTL	



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Pin No.	Name	Pin Type	Buffer Type	Function
233	$\overline{\text{DQS16}}$	I/O	SSTL	<b>Data Strobes 17:0</b>
164	$\overline{\text{DQS17}}$	I/O	SSTL	
165	$\overline{\text{DQS17}}$	I/O	SSTL	
<b>Data Mask</b>				
125	DM0	I	SSTL	<b>Data Masks 8:0</b> The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is LOW but blocks the write operation if it is HIGH. In Read mode, DM lines have no effect. <i>Note: x8 based module</i>
134	DM1	I	SSTL	
146	DM2	I	SSTL	
155	DM3	I	SSTL	
202	DM4	I	SSTL	
211	DM5	I	SSTL	
223	DM6	I	SSTL	
232	DM7	I	SSTL	
164	DM8	I	SSTL	
<b>EEPROM</b>				
120	SCL	I	CMOS	<b>Serial Bus Clock</b> This signal is used to clock data into and out of the SPD EEPROM.
119	SDA	I/O	OD	<b>Serial Bus Data</b> This is a bidirectional pin used to transfer data into or out of the SPD EEPROM. A resistor must be connected from SDA to $V_{\text{DDSPD}}$ on the motherboard to act as a pull-up.
239	SA0	I	CMOS	<b>Serial Address Select Bus 2:0</b> These signals are tied at the system planar to either $V_{\text{SS}}$ or $V_{\text{DDSPD}}$ to configure the serial SPD EEPROM address range
240	SA1	I	CMOS	
101	SA2	I	CMOS	
<b>Parity</b>				
55	$\overline{\text{ERR\_OUT}}$	O	CMOS	<b>Parity bits</b> <i>Note: Only for modules with parity bit for address and control bus. Not connected on non-parity registered modules.</i>
68	PAR_IN	I	CMOS	
<b>Power Supplies</b>				
1	$V_{\text{REF}}$	AI	—	<b>I/O Reference Voltage</b> Reference voltage for the SSTL-18 inputs.
238	$V_{\text{DDSPD}}$	PWR	—	<b>EEPROM Power Supply</b> Serial EEPROM positive power supply, wired to a separated power pin at the connector which supports from 1.7 Volt to 3.6 Volt.
51, 56, 62, 72, 75, 78, 170, 175, 181, 191, 194	$V_{\text{DDQ}}$	PWR	—	<b>I/O Driver Power Supply</b> Power and ground for the DDR SDRAM
53, 59, 64, 67, 69, 172, 178, 184, 187, 189, 197	$V_{\text{DD}}$	PWR	—	<b>Power Supply</b> Power and ground for the DDR SDRAM



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Pin No.	Name	Pin Type	Buffer Type	Function
2, 5, 8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41, 44, 47, 50, 65, 66, 79, 82, 85, 88, 91, 94, 97, 100, 103, 106, 109, 112, 115, 118, 121, 124, 127, 130, 133, 136, 139, 142, 145, 148, 151, 154, 157, 160, 163, 166, 169, 198, 201, 204, 207, 210, 213, 216, 219, 222, 225, 228, 231, 234, 237	V <sub>SS</sub>	GND	—	<b>Ground Plane</b> Power and ground for the DDR SDRAM
<b>Other Pins</b>				
19, 102, 137, 138,	NC	NC	—	<b>Not connected</b> Pins not connected on Qimonda RDIMM's
195	ODT0	I	SSTL	<b>On-Die Termination Control 1:0</b> Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ signals if enabled via the DDR2 SDRAM mode register. <i>Note: 2-Ranks module</i>
77	ODT1	I	SSTL	
	NC	NC	—	<i>Note: 1-Rank modules</i>

**TABLE 6**  
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL <sub>18</sub> )
CMOS	CMOS Levels
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

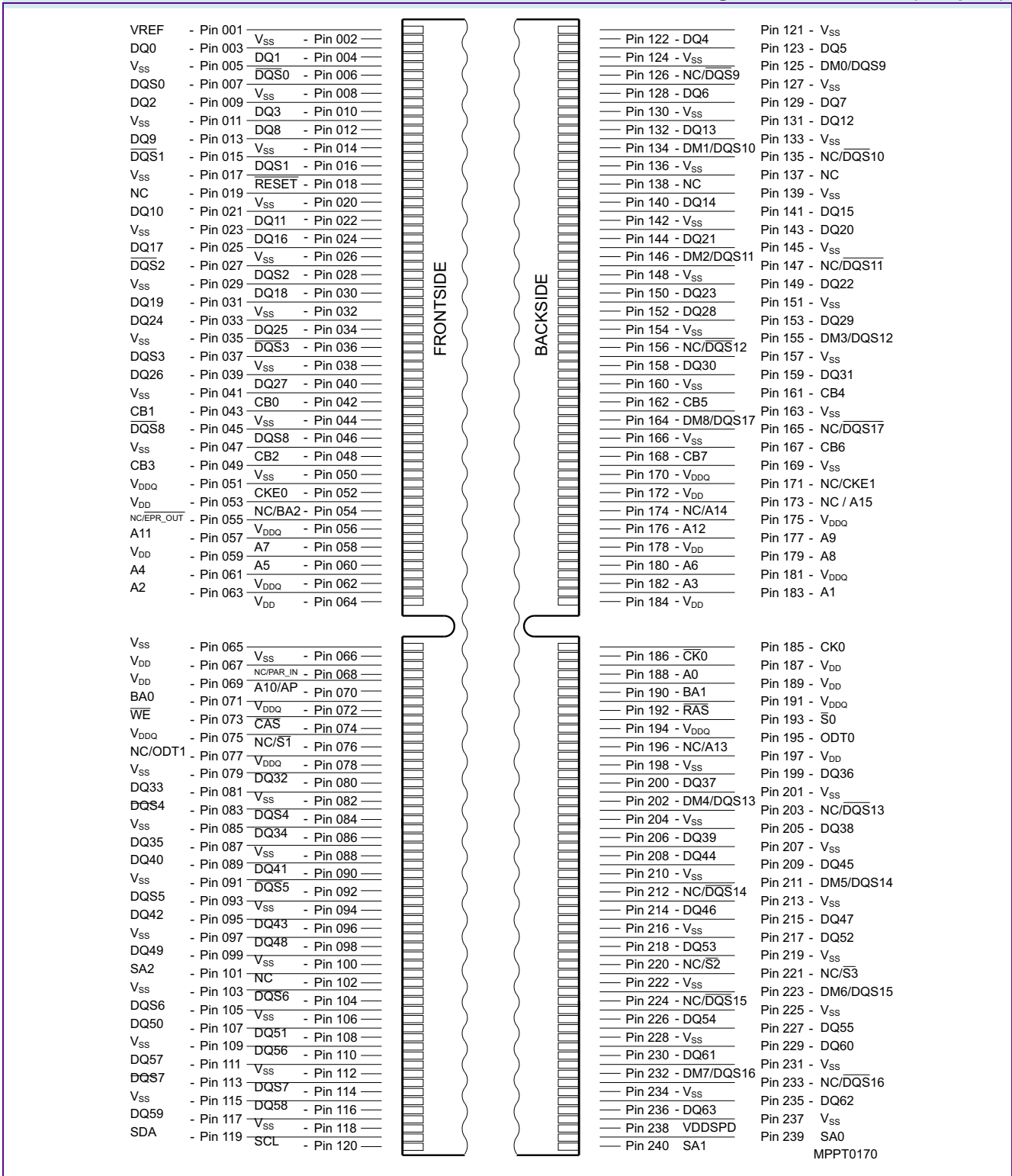
HYS72T[64/128/256]xx0HP-[3S/3.7]-A  
Registered DDR2 SDRAM Modules**TABLE 7**  
**Abbreviations for Pin Type**

<b>Abbreviation</b>	<b>Description</b>
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NU	Not Usable
NC	Not Connected



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**FIGURE 1**  
**Pin Configuration for RDIMM (240 pins)**





## 3 Electrical Characteristics

This chapter lists the electrical characteristics.

### 3.1 Absolute Maximum Ratings

Caution is needed not to exceed absolute maximum ratings of the DRAM device listed in **Table 8** at any time.

**TABLE 8**  
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
$V_{DD}$	Voltage on $V_{DD}$ pin relative to $V_{SS}$	-1.0	+2.3	V	1)
$V_{DDQ}$	Voltage on $V_{DDQ}$ pin relative to $V_{SS}$	-0.5	+2.3	V	1)2)
$V_{DDL}$	Voltage on $V_{DDL}$ pin relative to $V_{SS}$	-0.5	+2.3	V	1)2)
$V_{IN}, V_{OUT}$	Voltage on any pin relative to $V_{SS}$	-0.5	+2.3	V	1)
$T_{STG}$	Storage Temperature	-55	+100	°C	1)2)

1) When  $V_{DD}$  and  $V_{DDQ}$  and  $V_{DDL}$  are less than 500 mV;  $V_{REF}$  may be equal to or less than 300 mV.

2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

**Attention: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

**TABLE 9**  
DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
$T_{OPER}$	Operating Temperature	0	95	°C	1)2)3)4)

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.

2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.

3) Above 85 °C the Auto-Refresh command interval has to be reduced to  $t_{REFI} = 3.9 \mu s$

4) When operating this product in the 85 °C to 95 °C TCASE temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”. When the High Temperature Self Refresh is enabled there is an increase of  $I_{DD6}$  by approximately 50%



### 3.2 DC Operating Conditions

This chapter contains the DC operating condition tables.

**TABLE 10**  
Operating Conditions

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Operating temperature (ambient)	$T_{OPR}$	0	+65	°C	
DRAM Case Temperature	$T_{CASE}$	0	+95	°C	1)2)3)4)
Storage Temperature	$T_{STG}$	- 50	+100	°C	
Barometric Pressure (operating & storage)	PBar	+69	+105	kPa	5)
Operating Humidity (relative)	$H_{OPR}$	10	90	%	
Storage Humidity (without condensation)	$H_{STG}$	5	95	%	

- 1) DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs.
- 2) Within the DRAM Component Case Temperature Range all DRAM specifications will be supported
- 3) Above 85 °C DRAM Case Temperature the Auto-Refresh command interval has to be reduced to  $t_{REFI} = 3.9 \mu s$
- 4) When operating this product in the 85 °C to 95 °C  $T_{CASE}$  temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to "1". When the High Temperature Self Refresh is enabled there is an increase of  $I_{DD6}$  by approximately 50%.
- 5) Up to 3000 m.

**TABLE 11**  
Supply Voltage Levels and DC Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Device Supply Voltage	$V_{DD}$	1.7	1.8	1.9	V	
Output Supply Voltage	$V_{DDQ}$	1.7	1.8	1.9	V	1)
Input Reference Voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2)
SPD Supply Voltage	$V_{DDSPD}$	1.7	—	3.6	V	
DC Input Logic High	$V_{IH(DC)}$	$V_{REF} + 0.125$	—	$V_{DDQ} + 0.3$	V	
DC Input Logic Low	$V_{IL(DC)}$	- 0.30	—	$V_{REF} - 0.125$	V	
In / Output Leakage Current	$I_L$	- 5	—	5	μA	3)

- 1) Under all conditions,  $V_{DDQ}$  must be less than or equal to  $V_{DD}$
- 2) Peak to peak AC noise on  $V_{REF}$  may not exceed  $\pm 2\% V_{REF(DC)}$ .  $V_{REF}$  is also expected to track noise in  $V_{DDQ}$ .
- 3) Input voltage for any connector pin under test of  $0 V \leq V_{IN} \leq V_{DDQ} + 0.3 V$ ; all other pins at 0 V. Current is per pin





### 3.3 Timing Characteristics

This chapter describes the AC characteristics tables.

#### 3.3.1 Speed Grades Definitions

Speed Grade Definitions for: DDR2-667D (Table 12), DDR2-533C (Table 13)

**TABLE 12**

**Speed Grade Definition Speed Bins for DDR2-667D**

Speed Grade		DDR2-667D		Unit	Notes	
QAG Sort Name		-3S				
CAS-RCD-RP latencies		5-5-5		$t_{CK}$		
Parameter	Symbol	Min.	Max.	—		
Clock Frequency	@ CL = 3	$t_{CK}$	5	8	ns	1)2)3)4)
	@ CL = 4	$t_{CK}$	3.75	8	ns	1)2)3)4)
	@ CL = 5	$t_{CK}$	3	8	ns	1)2)3)4)
Row Active Time	$t_{RAS}$	45	70000	ns	1)2)3)4)5)	
Row Cycle Time	$t_{RC}$	60	—	ns	1)2)3)4)	
RAS-CAS-Delay	$t_{RCD}$	15	—	ns	1)2)3)4)	
Row Precharge Time	$t_{RP}$	15	—	ns	1)2)3)4)	

- 1) Timings are guaranteed with CK/CK differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0)
- 2) The CK/CK input reference level (for timing reference to CK/CK) is the point at which CK and CK cross. The DQS / DQS, RDQS / RDQS, input reference level is the crosspoint when in differential strobe mode
- 3) Inputs are not recognized as valid until  $V_{REF}$  stabilizes. During the period before  $V_{REF}$  stabilizes,  $CKE = 0.2 \times V_{DDQ}$  is recognized as low.
- 4) The output timing reference voltage level is  $V_{TT}$ .
- 5)  $t_{RAS,MAX}$  is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to  $9 \times t_{REFI}$ .

**TABLE 13**

**Speed Grade Definition Speed Bins for DDR2-533C**

Speed Grade		DDR2-533C		Unit	Note	
QAG Sort Name		-3.7				
CAS-RCD-RP latencies		4-4-4		$t_{CK}$		
Parameter	Symbol	Min.	Max.	—		
Clock Frequency	@ CL = 3	$t_{CK}$	5	8	ns	1)2)3)4)
	@ CL = 4	$t_{CK}$	3.75	8	ns	1)2)3)4)
	@ CL = 5	$t_{CK}$	3.75	8	ns	1)2)3)4)
Row Active Time	$t_{RAS}$	45	70000	ns	1)2)3)4)5)	
Row Cycle Time	$t_{RC}$	60	—	ns	1)2)3)4)	



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Speed Grade		DDR2-533C		Unit	Note
QAG Sort Name		-3.7			
CAS-RCD-RP latencies		4-4-4		$t_{CK}$	
Parameter	Symbol	Min.	Max.	—	
RAS-CAS-Delay	$t_{RCD}$	15	—	ns	1)2)3)4)
Row Precharge Time	$t_{RP}$	15	—	ns	1)2)3)4)

- 1) Timings are guaranteed with CK/ $\overline{CK}$  differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0)
- 2) The CK/ $\overline{CK}$  input reference level (for timing reference to CK/ $\overline{CK}$ ) is the point at which CK and  $\overline{CK}$  cross. The DQS /  $\overline{DQS}$ , RDQS /  $\overline{RDQS}$ , input reference level is the crosspoint when in differential strobe mode.
- 3) Inputs are not recognized as valid until  $V_{REF}$  stabilizes. During the period before  $V_{REF}$  stabilizes, CKE =  $0.2 \times V_{DDQ}$  is recognized as low.
- 4) The output timing reference voltage level is  $V_{TT}$ .
- 5)  $t_{RAS,MAX}$  is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to  $9 \times t_{REFI}$ .



### 3.3.2 Component AC Timing Parameters

Speed Grade Definitions for: DDR2-667 (Table 14), DDR2-533C (Table 15)

**TABLE 14**

**DRAM Component Timing Parameter by Speed Grade - DDR2-667**

Parameter	Symbol	DDR2-667		Unit	Notes <sup>1)2)3)4)5)6)7)8)</sup>
		Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	$t_{AC}$	-450	+450	ps	9)
CAS to CAS command delay	$t_{CCD}$	2	—	nCK	
Average clock high pulse width	$t_{CH.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Average clock period	$t_{CK.AVG}$	3000	8000	ps	
CKE minimum pulse width ( high and low pulse width)	$t_{CKE}$	3	—	nCK	12)
Average clock low pulse width	$t_{CL.AVG}$	0.48	0.52	$t_{CK.AVG}$	10)11)
Auto-Precharge write recovery + precharge time	$t_{DAL}$	WR + $t_{nRP}$	—	nCK	13)14)
Minimum time clocks remain ON after CKE asynchronously drops LOW	$t_{DELAY}$	$t_{IS} + t_{CK.AVG} + t_{IH}$	—	ns	
DQ and DM input hold time	$t_{DH.BASE}$	175	—	ps	19)20)15)
DQ and DM input pulse width for each input	$t_{DIPW}$	0.35	—	$t_{CK.AVG}$	
DQS output access time from CK / $\overline{\text{CK}}$	$t_{DQSQ}$	-400	+400	ps	9)
DQS input high pulse width	$t_{DQSH}$	0.35	—	$t_{CK.AVG}$	
DQS input low pulse width	$t_{DQSL}$	0.35	—	$t_{CK.AVG}$	
DQS-DQ skew for DQS & associated DQ signals	$t_{DQSQ}$	—	240	ps	16)
DQS latching rising transition to associated clock edges	$t_{DQSS}$	- 0.25	+ 0.25	$t_{CK.AVG}$	17)
DQ and DM input setup time	$t_{DS.BASE}$	100	—	ps	18)19)20)
DQS falling edge hold time from CK	$t_{DSH}$	0.2	—	$t_{CK.AVG}$	17)
DQS falling edge to CK setup time	$t_{DSS}$	0.2	—	$t_{CK.AVG}$	17)
CK half pulse width	$t_{HP}$	Min( $t_{CH.ABS}$ , $t_{CL.ABS}$ )	—	ps	21)
Data-out high-impedance time from CK / $\overline{\text{CK}}$	$t_{HZ}$	—	$t_{AC.MAX}$	ps	9)22)
Address and control input hold time	$t_{IH.BASE}$	275	—	ps	25)23)
Control & address input pulse width for each input	$t_{IPW}$	0.6	—	$t_{CK.AVG}$	
Address and control input setup time	$t_{IS.BASE}$	200	—	ps	24)25)
DQ low impedance time from CK/ $\overline{\text{CK}}$	$t_{LZ.DQ}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)22)
DQS/ $\overline{\text{DQS}}$ low-impedance time from CK / $\overline{\text{CK}}$	$t_{LZ.DQS}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	9)22)
MRS command to ODT update delay	$t_{MOD}$	0	12	ns	35)
Mode register set command cycle time	$t_{MRD}$	2	—	nCK	
OCD drive mode output delay	$t_{OIT}$	0	12	ns	35)
DQ/DQS output hold time from DQS	$t_{QH}$	$t_{HP} - t_{QHS}$	—	ps	26)
DQ hold skew factor	$t_{QHS}$	—	340	ps	27)



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Parameter	Symbol	DDR2-667		Unit	Notes <sup>1)2)3)4)5)6)7)8)</sup>
		Min.	Max.		
Average periodic refresh Interval	$t_{REFI}$	—	7.8	$\mu$ s	28)29)
		—	3.9	$\mu$ s	29)30)
Auto-Refresh to Active/Auto-Refresh command period	$t_{RFC}$	105	—	ns	31)
Precharge-All (4 banks) command period	$t_{RP}$	$t_{RP}$	—	ns	
Read preamble	$t_{RPRE}$	0.9	1.1	$t_{CK,AVG}$	32)33)
Read postamble	$t_{RPST}$	0.4	0.6	$t_{CK,AVG}$	32)34)
Internal Read to Precharge command delay	$t_{RTP}$	7.5	—	ns	35)
Write preamble	$t_{WPRE}$	0.35	—	$t_{CK,AVG}$	
Write postamble	$t_{WPST}$	0.4	0.6	$t_{CK,AVG}$	
Write recovery time	$t_{WR}$	15	—	ns	35)
Internal write to read command delay	$t_{WTR}$	7.5	—	ns	35)36)
Exit power down to read command	$t_{XARD}$	2	—	nCK	
Exit active power-down mode to read command (slow exit, lower power)	$t_{XARDS}$	7 – AL	—	nCK	
Exit precharge power-down to any valid command (other than NOP or Deselect)	$t_{XP}$	2	—	nCK	
Exit self-refresh to a non-read command	$t_{XSNR}$	$t_{RFC} + 10$	—	ns	35)
Exit self-refresh to read command	$t_{XSRD}$	200	—	nCK	
Write command to DQS associated clock edges	WL	RL-1		nCK	

- 1) For details and notes see the relevant Qimonda component data sheet
- 2)  $V_{DDQ} = 1.8\text{ V} \pm 0.1\text{ V}$ ;  $V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$ .
- 3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) Timings are guaranteed with CK/ $\overline{\text{CK}}$  differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 5) The CK /  $\overline{\text{CK}}$  input reference level (for timing reference to CK /  $\overline{\text{CK}}$ ) is the point at which CK and  $\overline{\text{CK}}$  cross. The DQS /  $\overline{\text{DQS}}$ , RDQS /  $\overline{\text{RDQS}}$ , input reference level is the crosspoint when in differential strobe mode.
- 6) Inputs are not recognized as valid until  $V_{REF}$  stabilizes. During the period before  $V_{REF}$  stabilizes,  $\text{CKE} = 0.2 \times V_{DDQ}$  is recognized as low.
- 7) The output timing reference voltage level is  $V_{TT}$ .
- 8) New units, ' $t_{CK,AVG}$ ' and 'nCK', are introduced in DDR2-667 and DDR2-800. Unit ' $t_{CK,AVG}$ ' represents the actual  $t_{CK,AVG}$  of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, ' $t_{CK}$ ' is used for both concepts. Example:  $t_{XP} = 2$  [nCK] means; if Power Down exit is registered at  $T_m$ , an Active command may be registered at  $T_m + 2$ , even if  $(T_m + 2 - T_m)$  is  $2 \times t_{CK,AVG} + t_{ERR,2PER(MIN)}$ .
- 9) When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{ERR(6-10PER)}$  of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has  $t_{ERR(6-10PER),MIN} = -272$  ps and  $t_{ERR(6-10PER),MAX} = +293$  ps, then  $t_{DQSCK,MIN(DERATED)} = t_{DQSCK,MIN} - t_{ERR(6-10PER),MAX} = -400$  ps - 293 ps = -693 ps and  $t_{DQSCK,MAX(DERATED)} = t_{DQSCK,MAX} - t_{ERR(6-10PER),MIN} = 400$  ps + 272 ps = +672 ps. Similarly,  $t_{LZ,DQ}$  for DDR2-667 derates to  $t_{LZ,DQ,MIN(DERATED)} = -900$  ps - 293 ps = -1193 ps and  $t_{LZ,DQ,MAX(DERATED)} = 450$  ps + 272 ps = +722 ps. (Caution on the MIN/MAX usage!)
- 10) Input clock jitter spec parameter. These parameters are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2-667 and DDR2-800 only. The jitter specified is a random jitter meeting a Gaussian distribution.
- 11) These parameters are specified per their average values, however it is understood that the relationship between the average timing and the absolute instantaneous timing holds all the times (min. and max of SPEC values are to be used for calculations).
- 12)  $t_{CKE,MIN}$  of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of  $t_{IS} + 2 \times t_{CK} + t_{IH}$ .

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- 13)  $DAL = WR + RU\{t_{RP}(ns) / t_{CK}(ns)\}$ , where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For  $t_{RP}$ , if the result of the division is not already an integer, round up to the next highest integer.  $t_{CK}$  refers to the application clock period. Example: For DDR2-533 at  $t_{CK} = 3.75$  ns with  $t_{WR}$  programmed to 4 clocks.  $t_{DAL} = 4 + (15 \text{ ns} / 3.75 \text{ ns}) \text{ clocks} = 4 + (4) \text{ clocks} = 8 \text{ clocks}$ .
- 14)  $t_{DAL,nCK} = WR [nCK] + t_{nRP,nCK} = WR + RU\{t_{RP} [ps] / t_{CK,AVG}[ps]\}$ , where WR is the value programmed in the EMR.
- 15) Input waveform timing  $t_{DH}$  with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe crosspoint to the input signal crossing at the  $V_{IH,DC}$  level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the  $V_{IL,DC}$  level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between  $V_{IL,DC,MAX}$  and  $V_{IH,DC,MIN}$ . See **Figure 3**.
- 16)  $t_{DQSQ}$ : Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS /  $\overline{DQS}$  and associated DQ in any given cycle.
- 17) These parameters are measured from a data strobe signal ((L/U/R)DQS /  $\overline{DQS}$ ) crossing to its respective clock signal (CK /  $\overline{CK}$ ) crossing. The spec values are not affected by the amount of clock jitter applied (i.e.  $t_{JIT,PER}$ ,  $t_{JIT,CC}$ , etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
- 18) Input waveform timing  $t_{DS}$  with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the  $V_{IH,AC}$  level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the  $V_{IL,AC}$  level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between  $V_{I(DC)MAX}$  and  $V_{I(DC)MIN}$ . See **Figure 3**.
- 19) If  $t_{DS}$  or  $t_{DH}$  is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
- 20) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS /  $\overline{DQS}$ ) crossing.
- 21)  $t_{HP}$  is the minimum of the absolute half period of the actual input clock.  $t_{HP}$  is an input parameter but not an input specification parameter. It is used in conjunction with  $t_{QHS}$  to derive the DRAM output timing  $t_{QH}$ . The value to be used for  $t_{QH}$  calculation is determined by the following equation;  $t_{HP} = \text{MIN}(t_{CH,ABS}, t_{CL,ABS})$ , where,  $t_{CH,ABS}$  is the minimum of the actual instantaneous clock high time;  $t_{CL,ABS}$  is the minimum of the actual instantaneous clock low time.
- 22)  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving ( $t_{HZ}$ ), or begins driving ( $t_{LZ}$ ).
- 23) Input waveform timing is referenced from the input signal crossing at the  $V_{IL,DC}$  level for a rising signal and  $V_{IH,DC}$  for a falling signal applied to the device under test. See **Figure 4**.
- 24) Input waveform timing is referenced from the input signal crossing at the  $V_{IH,AC}$  level for a rising signal and  $V_{IL,AC}$  for a falling signal applied to the device under test. See **Figure 4**.
- 25) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK /  $\overline{CK}$ ) crossing. The spec values are not affected by the amount of clock jitter applied (i.e.  $t_{JIT,PER}$ ,  $t_{JIT,CC}$ , etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
- 26)  $t_{QH} = t_{HP} - t_{QHS}$ , where:  $t_{HP}$  is the minimum of the absolute half period of the actual input clock; and  $t_{QHS}$  is the specification value under the max column. {The less half-pulse width distortion present, the larger the  $t_{QH}$  value is; and the larger the valid data eye will be.} Examples: 1) If the system provides  $t_{HP}$  of 1315 ps into a DDR2-667 SDRAM, the DRAM provides  $t_{QH}$  of 975 ps minimum. 2) If the system provides  $t_{HP}$  of 1420 ps into a DDR2-667 SDRAM, the DRAM provides  $t_{QH}$  of 1080 ps minimum.
- 27)  $t_{QHS}$  accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual  $t_{HP}$  at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.
- 28) The Auto-Refresh command interval has been reduced to 3.9  $\mu$ s when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
- 29)  $0^\circ\text{C} \leq T_{CASE} \leq 85^\circ\text{C}$
- 30)  $85^\circ\text{C} < T_{CASE} \leq 95^\circ\text{C}$
- 31) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
- 32)  $t_{RPST}$  end point and  $t_{RPRE}$  begin point are not referenced to a specific voltage level but specify when the device output is no longer driving ( $t_{RPST}$ ), or begins driving ( $t_{RPRE}$ ). **Figure 2** shows a method to calculate these points when the device is no longer driving ( $t_{RPST}$ ), or begins driving ( $t_{RPRE}$ ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
- 33) When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{JIT,PER}$  of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has  $t_{JIT,PER,MIN} = -72$  ps and  $t_{JIT,PER,MAX} = +93$  ps, then  $t_{RPRE,MIN(DERATED)} = t_{RPRE,MIN} + t_{JIT,PER,MIN} = 0.9 \times t_{CK,AVG} - 72 \text{ ps} = +2178 \text{ ps}$  and  $t_{RPRE,MAX(DERATED)} = t_{RPRE,MAX} + t_{JIT,PER,MAX} = 1.1 \times t_{CK,AVG} + 93 \text{ ps} = +2843 \text{ ps}$ . (Caution on the MIN/MAX usage!).
- 34) When the device is operated with input clock jitter, this parameter needs to be derated by the actual  $t_{JIT,DUTY}$  of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has  $t_{JIT,DUTY,MIN} = -72$  ps and  $t_{JIT,DUTY,MAX} = +93$  ps, then  $t_{RPST,MIN(DERATED)} = t_{RPST,MIN} + t_{JIT,DUTY,MIN} = 0.4 \times t_{CK,AVG} - 72 \text{ ps} = +928 \text{ ps}$  and  $t_{RPST,MAX(DERATED)} = t_{RPST,MAX} + t_{JIT,DUTY,MAX} = 0.6 \times t_{CK,AVG} + 93 \text{ ps} = +1592 \text{ ps}$ . (Caution on the MIN/MAX usage!).

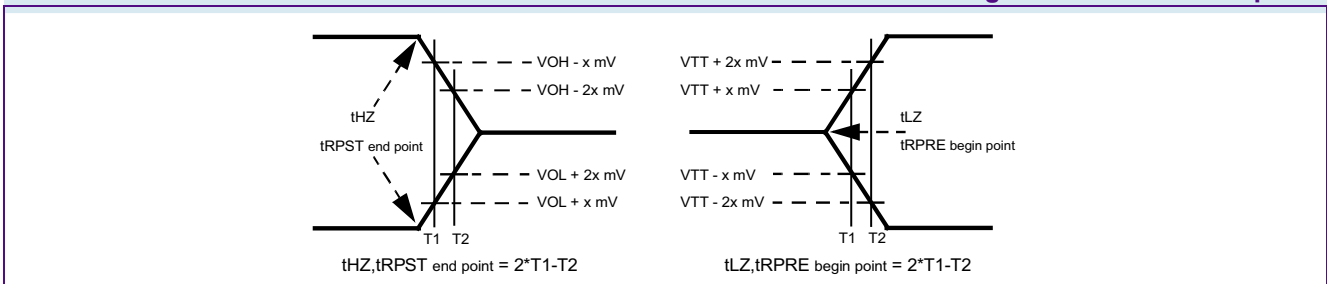


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- 35) For these parameters, the DDR2 SDRAM device is characterized and verified to support  $t_{nPARAM} = RU\{t_{PARAM} / t_{CK,AVG}\}$ , which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support  $t_{nRP} = RU\{t_{RP} / t_{CK,AVG}\}$ , which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2-667 5-5-5, of which  $t_{RP} = 15$  ns, the device will support  $t_{nRP} = RU\{t_{RP} / t_{CK,AVG}\} = 5$ , i.e. as long as the input clock jitter specifications are met, Precharge command at  $T_m$  and Active command at  $T_m + 5$  is valid even if  $(T_m + 5 - T_m)$  is less than 15 ns due to input clock jitter.
- 36)  $t_{WTR}$  is at least two clocks ( $2 \times t_{CK}$ ) independent of operation frequency.

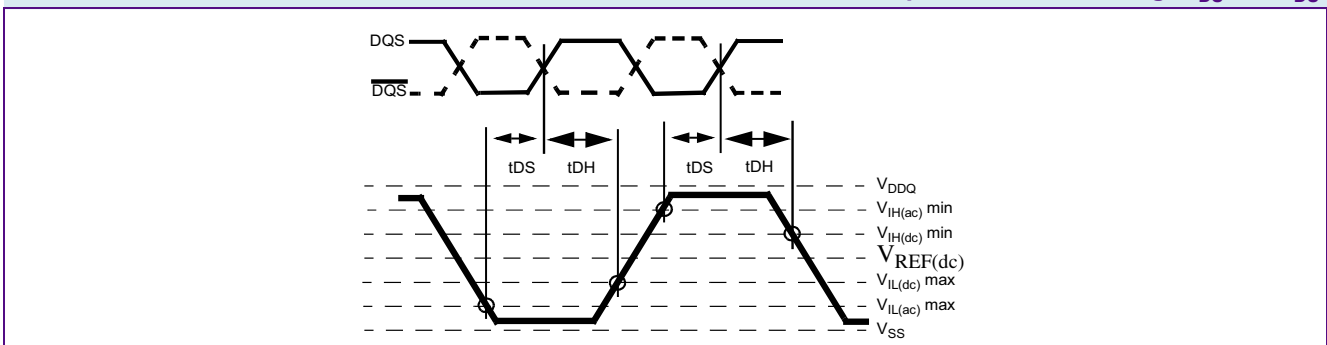
**FIGURE 2**

**Method for calculating transitions and endpoint**



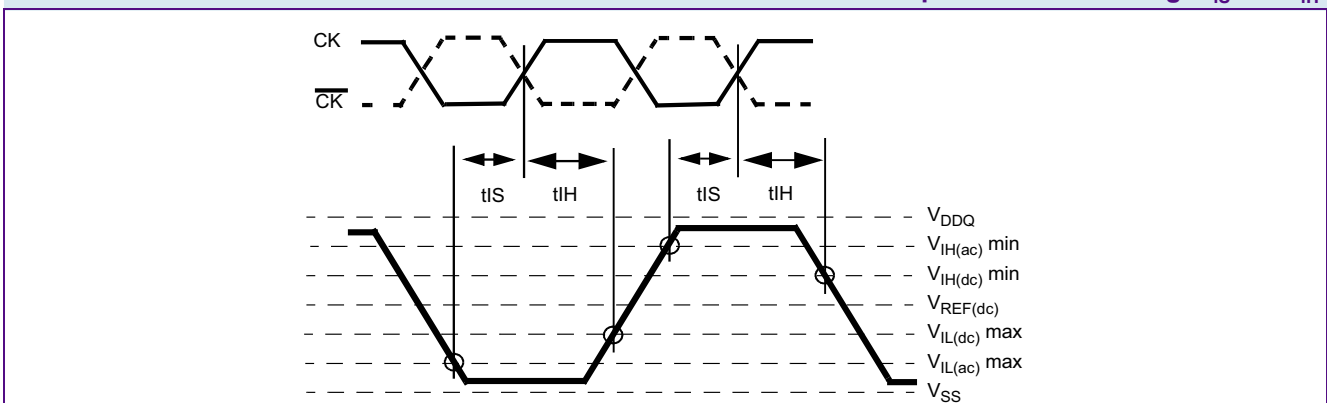
**FIGURE 3**

**Differential input waveform timing -  $t_{DS}$  and  $t_{DH}$**



**FIGURE 4**

**Differential input waveform timing -  $t_{IS}$  and  $t_{IH}$**





**TABLE 15**  
**DRAM Component Timing Parameter by Speed Grade - DDR2-533**

Parameter	Symbol	DDR2-533		Unit	Notes <sup>1)2)3)4)5)6)7)</sup>
		Min.	Max.		
DQ output access time from CK / $\overline{\text{CK}}$	$t_{AC}$	-500	+500	ps	
CAS A to $\overline{\text{CAS}}$ B command period	$t_{CCD}$	2	—	$t_{CK}$	
CK, $\overline{\text{CK}}$ high-level width	$t_{CH}$	0.45	0.55	$t_{CK}$	
CKE minimum high and low pulse width	$t_{CKE}$	3	—	$t_{CK}$	
CK, $\overline{\text{CK}}$ low-level width	$t_{CL}$	0.45	0.55	$t_{CK}$	
Auto-Precharge write recovery + precharge time	$t_{DAL}$	WR + $t_{RP}$	—	$t_{CK}$	8)18)
Minimum time clocks remain ON after CKE asynchronously drops LOW	$t_{DELAY}$	$t_{IS} + t_{CK} + t_{IH}$	—	ns	9)
DQ and DM input hold time (differential data strobe)	$t_{DH}(\text{base})$	225	—	ps	10)
DQ and DM input hold time (single ended data strobe)	$t_{DH1}(\text{base})$	-25	—	ps	11)
DQ and DM input pulse width (each input)	$t_{DIPW}$	0.35	—	$t_{CK}$	
DQS output access time from CK / $\overline{\text{CK}}$	$t_{DQSCK}$	-450	+450	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	$t_{CK}$	
DQS-DQ skew (for DQS & associated DQ signals)	$t_{DQSQ}$	—	300	ps	11)
Write command to 1st DQS latching transition	$t_{DQSS}$	- 0.25	+ 0.25	$t_{CK}$	
DQ and DM input setup time (differential data strobe)	$t_{DS}(\text{base})$	100	—	ps	11)
DQ and DM input setup time (single ended data strobe)	$t_{DS1}(\text{base})$	-25	—	ps	11)
DQS falling edge hold time from CK (write cycle)	$t_{DSH}$	0.2	—	$t_{CK}$	
DQS falling edge to CK setup time (write cycle)	$t_{DSS}$	0.2	—	$t_{CK}$	
Clock half period	$t_{HP}$	MIN. ( $t_{CL}, t_{CH}$ )			12)
Data-out high-impedance time from CK / $\overline{\text{CK}}$	$t_{HZ}$	—	$t_{AC,MAX}$	ps	13)
Address and control input hold time	$t_{IH}(\text{base})$	375	—	ps	11)
Address and control input pulse width (each input)	$t_{IPW}$	0.6	—	$t_{CK}$	
Address and control input setup time	$t_{IS}(\text{base})$	250	—	ps	11)
DQ low-impedance time from CK / $\overline{\text{CK}}$	$t_{LZ(DQ)}$	$2 \times t_{AC,MIN}$	$t_{AC,MAX}$	ps	14)
DQS low-impedance from CK / $\overline{\text{CK}}$	$t_{LZ(DQS)}$	$t_{AC,MIN}$	$t_{AC,MAX}$	ps	14)
MRS command to ODT update delay	$t_{MOD}$	0	12	ns	
Mode register set command cycle time	$t_{MRD}$	2	—	$t_{CK}$	
OCD drive mode output delay	$t_{OIT}$	0	12	ns	
Data output hold time from DQS	$t_{QH}$	$t_{HP} - t_{QHS}$	—		
Data hold skew factor	$t_{QHS}$	—	400	ps	



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Parameter	Symbol	DDR2-533		Unit	Notes <sup>1)2)3)4)5)6)7)</sup>
		Min.	Max.		
Average periodic refresh Interval	$t_{REFI}$	—	7.8	$\mu\text{s}$	14)15)
Average periodic refresh Interval	$t_{REFI}$	—	3.9	$\mu\text{s}$	16)18)
Auto-Refresh to Active/Auto-Refresh command period	$t_{RFC}$	105	—	ns	17)
Precharge-All (4 banks) command period	$t_{RP}$	$t_{RP}$	—	ns	
Read preamble	$t_{RPRE}$	0.9	1.1	$t_{CK}$	14)
Read postamble	$t_{RPST}$	0.40	0.60	$t_{CK}$	14)
Active bank A to Active bank B command period	$t_{RRD}$	7.5	—	ns	14)18)
Active bank A to Active bank B command period	$t_{RRD}$	10	—	ns	16)22)
Internal Read to Precharge command delay	$t_{RTP}$	7.5	—	ns	
Write preamble	$t_{WPRE}$	0.25	—	$t_{CK}$	
Write postamble	$t_{WPST}$	0.40	0.60	$t_{CK}$	19)
Write recovery time for write without Auto-Precharge	$t_{WR}$	15	—	ns	
Internal Write to Read command delay	$t_{WTR}$	7.5	—	ns	20)
Exit power down to any valid command (other than NOP or Deselect)	$t_{XARD}$	2	—	$t_{CK}$	21)
Exit active power-down mode to Read command (slow exit, lower power)	$t_{XARDS}$	6 – AL	—	$t_{CK}$	21)
Exit precharge power-down to any valid command (other than NOP or Deselect)	$t_{XP}$	2	—	$t_{CK}$	
Exit Self-Refresh to non-Read command	$t_{XSNR}$	$t_{RFC} + 10$	—	ns	
Exit Self-Refresh to Read command	$t_{XSRD}$	200	—	$t_{CK}$	
Write recovery time for write with Auto-Precharge	WR	$t_{WR}/t_{CK}$		$t_{CK}$	22)

- 1) For details and notes see the relevant Qimonda component data sheet
- 2)  $V_{DDQ} = 1.8\text{ V} \pm 0.1\text{ V}$ ;  $V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$ .
- 3) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
- 4) Timings are guaranteed with  $\overline{CK}/\overline{CK}$  differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.
- 5) The  $\overline{CK} / \overline{CK}$  input reference level (for timing reference to  $\overline{CK} / \overline{CK}$ ) is the point at which  $\overline{CK}$  and  $\overline{CK}$  cross. The  $\overline{DQS} / \overline{DQS}$ ,  $\overline{RDQS} / \overline{RDQS}$ , input reference level is the crosspoint when in differential strobe mode.
- 6) Inputs are not recognized as valid until  $V_{REF}$  stabilizes. During the period before  $V_{REF}$  stabilizes,  $\overline{CKE} = 0.2 \times V_{DDQ}$  is recognized as low.
- 7) The output timing reference voltage level is  $V_{TT}$ .
- 8) For each of the terms, if not already an integer, round to the next highest integer.  $t_{CK}$  refers to the application clock period. WR refers to the WR parameter stored in the MR.
- 9) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
- 10) For timing definition, refer to the Component data sheet.
- 11) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between  $\overline{DQS} / \overline{DQS}$  and associated DQ in any given cycle.
- 12) MIN ( $t_{CL}$ ,  $t_{CH}$ ) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for  $t_{CL}$  and  $t_{CH}$ ).





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- 13) The  $t_{HZ}$ ,  $t_{RPST}$  and  $t_{LZ}$ ,  $t_{RPRE}$  parameters are referenced to a specific voltage level, which specify when the device output is no longer driving ( $t_{HZ}$ ,  $t_{RPST}$ ), or begins driving ( $t_{LZ}$ ,  $t_{RPRE}$ ).  $t_{HZ}$  and  $t_{LZ}$  transitions occur in the same access time windows as valid data transitions. These parameters are verified by design and characterization, but not subject to production test.
- 14) The Auto-Refresh command interval has been reduced to 3.9  $\mu$ s when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
- 15)  $0\text{ }^{\circ}\text{C} \leq T_{CASE} \leq 85\text{ }^{\circ}\text{C}$
- 16)  $85\text{ }^{\circ}\text{C} < T_{CASE} \leq 95\text{ }^{\circ}\text{C}$
- 17) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
- 18) The  $t_{RRD}$  timing parameter depends on the page size of the DRAM organization. See **Table 2 “Ordering Information for RoHS Compliant Products” on Page 4.**
- 19) The maximum limit for the  $t_{WPST}$  parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
- 20) Minimum  $t_{WTR}$  is two clocks when operating the DDR2-SDRAM at frequencies  $\leq 200$  MHz.
- 21) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MR, A12 = “0”) a fast power-down exit timing  $t_{XARD}$  can be used. In “low active power-down mode” (MR, A12 = “1”) a slow power-down exit timing  $t_{XARDS}$  has to be satisfied.
- 22) WR must be programmed to fulfill the minimum requirement for the  $t_{WR}$  timing parameter, where  $WR_{MIN}[\text{cycles}] = t_{WR}(\text{ns})/t_{CK}(\text{ns})$  rounded up to the next integer value.  $t_{DAL} = WR + (t_{RP}/t_{CK})$ . For each of the terms, if not already an integer, round to the next highest integer.  $t_{CK}$  refers to the application clock period. WR refers to the WR parameter stored in the MRS.

### 3.3.3 ODT AC Electrical Characteristics

This chapter contains the ODT AC characteristic tables.

**TABLE 16**  
**ODT AC Character. and Operating Conditions for DDR2-667**

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
$t_{AOND}$	ODT turn-on delay	2	2	nCK	1)
$t_{AON}$	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX} + 0.7\text{ ns}$	ns	1)2)
$t_{AONPD}$	ODT turn-on (Power-Down Modes)	$t_{AC.MIN} + 2\text{ ns}$	$2 t_{CK} + t_{AC.MAX} + 1\text{ ns}$	ns	1)
$t_{AOFD}$	ODT turn-off delay	2.5	2.5	nCK	1)
$t_{AOF}$	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX} + 0.6\text{ ns}$	ns	1)3)
$t_{AOFPD}$	ODT turn-off (Power-Down Modes)	$t_{AC.MIN} + 2\text{ ns}$	$2.5 t_{CK} + t_{AC.MAX} + 1\text{ ns}$	ns	1)
$t_{ANPD}$	ODT to Power Down Mode Entry Latency	3	—	nCK	1)
$t_{AXPD}$	ODT Power Down Exit Latency	8	—	nCK	1)

- 1) New units, ' $t_{CK.AVG}$ ' and 'nCK', are introduced in DDR2-667 and DDR2-800. Unit ' $t_{CK.AVG}$ ' represents the actual  $t_{CK.AVG}$  of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, ' $t_{CK}$ ' is used for both concepts. Example:  $t_{XP} = 2\text{ [nCK]}$  means; if Power Down exit is registered at  $T_m$ , an Active command may be registered at  $T_m + 2$ , even if  $(T_m + 2 - T_m)$  is  $2 \times t_{CK.AVG} + t_{EPR.2PER(MIN)}$ .
- 2) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from  $t_{AOND}$ , which is interpreted differently per speed bin. For DDR2-667/800,  $t_{AOND}$  is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.
- 3) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from  $t_{AOFD}$ . Both are measured from  $t_{AOFD}$ , which is interpreted differently per speed bin. For DDR2-667/800, if  $t_{CK.AVG} = 3\text{ ns}$  is assumed,  $t_{AOFD} = 1.5\text{ ns}$  ( $0.5 \times 3\text{ ns}$ ) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edge.



**TABLE 17**  
**ODT AC Character. and Operating Conditions for DDR2-533**

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
$t_{AOND}$	ODT turn-on delay	2	2	$t_{CK}$	
$t_{AON}$	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX} + 1 \text{ ns}$	ns	1)
$t_{AONPD}$	ODT turn-on (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
$t_{AOFD}$	ODT turn-off delay	2.5	2.5	$t_{CK}$	
$t_{AOF}$	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX} + 0.6 \text{ ns}$	ns	2)
$t_{AOFPD}$	ODT turn-off (Power-Down Modes)	$t_{AC.MIN} + 2 \text{ ns}$	$2.5 t_{CK} + t_{AC.MAX} + 1 \text{ ns}$	ns	
$t_{ANPD}$	ODT to Power Down Mode Entry Latency	3	—	$t_{CK}$	
$t_{AXPD}$	ODT Power Down Exit Latency	8	—	$t_{CK}$	

- 1) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from  $t_{AOND}$ , which is interpreted differently per speed bin. For DDR2-400/533,  $t_{AOND}$  is 10 ns (= 2 x 5 ns) after the clock edge that registered a first ODT HIGH if  $t_{CK} = 5 \text{ ns}$ .
- 2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from  $t_{AOFD}$ . Both are measured from  $t_{AOFD}$ , which is interpreted differently per speed bin. For DDR2-400/533,  $t_{AOFD}$  is 12.5 ns (= 2.5 x 5 ns) after the clock edge that registered a first ODT HIGH if  $t_{CK} = 5 \text{ ns}$ .



### 3.4 $I_{DD}$ Specifications and Conditions

This chapter describes the  $I_{DD}$  Specifications and Conditions.

- **Table 18 “IDD Measurement Conditions” on Page 27**
- **Table 19 “Definitions for IDD” on Page 28**
- **Table 20 “IDD Specification for HYS72T[64/128/256]xx0HP-3S-A” on Page 29**
- **Table 21 “IDD Specification for HYS72T[64/128/256]xx0HP-3.7-A” on Page 30**

**TABLE 18**  
 **$I_{DD}$  Measurement Conditions**

Parameter	Symbol	Note 1)2)3)4)5)
<b>Operating Current 0</b> One bank Active - Precharge; $t_{CK} = t_{CK.MIN}$ , $t_{RC} = t_{RC.MIN}$ , $t_{RAS} = t_{RAS.MIN}$ , $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	$I_{DD0}$	
<b>Operating Current 1</b> One bank Active - Read - Precharge; $I_{OUT} = 0$ mA, $BL = 4$ , $t_{CK} = t_{CK.MIN}$ , $t_{RC} = t_{RC.MIN}$ , $t_{RAS} = t_{RAS.MIN}$ , $t_{RCD} = t_{RCD.MIN}$ , $AL = 0$ , $CL = CL_{MIN}$ ; $\overline{CS}$ is HIGH between valid commands. Address and control inputs are SWITCHING, Databus inputs are SWITCHING.	$I_{DD1}$	6)
<b>Precharge Standby Current</b> All banks idle; $\overline{CS}$ is HIGH; $\overline{CKE}$ is HIGH; $t_{CK} = t_{CK.MIN}$ ; Other control and address inputs are SWITCHING, Databus inputs are SWITCHING.	$I_{DD2N}$	
<b>Precharge Power-Down Current</b> Other control and address inputs are STABLE, Data bus inputs are FLOATING.	$I_{DD2P}$	
<b>Precharge Quiet Standby Current</b> All banks idle; $\overline{CS}$ is HIGH; $\overline{CKE}$ is HIGH; $t_{CK} = t_{CK.MIN}$ ; Other control and address inputs are STABLE, Data bus inputs are FLOATING.	$I_{DD2Q}$	
<b>Active Standby Current</b> Burst Read: All banks open; Continuous burst reads; $BL = 4$ ; $AL = 0$ , $CL = CL_{MIN}$ ; $t_{CK} = t_{CK.MIN}$ ; $t_{RAS} = t_{RAS.MAX}$ , $t_{RP} = t_{RP.MIN}$ ; $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING; $I_{OUT} = 0$ mA.	$I_{DD3N}$	
<b>Active Power-Down Current</b> All banks open; $t_{CK} = t_{CK.MIN}$ , $\overline{CKE}$ is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to LOW (Fast Power-down Exit);	$I_{DD3P(0)}$	
<b>Active Power-Down Current</b> All banks open; $t_{CK} = t_{CK.MIN}$ , $\overline{CKE}$ is LOW; Other control and address inputs are STABLE, Data bus inputs are FLOATING. MRS A12 bit is set to HIGH (Slow Power-down Exit);	$I_{DD3P(1)}$	
<b>Operating Current - Burst Read</b> All banks open; Continuous burst reads; $BL = 4$ ; $AL = 0$ , $CL = CL_{MIN}$ ; $t_{CK} = t_{CK.MIN}$ ; $t_{RAS} = t_{RAS.MAX}$ ; $t_{RP} = t_{RP.MIN}$ ; $\overline{CS}$ is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; $I_{OUT} = 0$ mA.	$I_{DD4R}$	6)
<b>Operating Current - Burst Write</b> All banks open; Continuous burst writes; $BL = 4$ ; $AL = 0$ , $CL = CL_{MIN}$ ; $t_{CK} = t_{CK.MIN}$ ; $t_{RAS} = t_{RAS.MAX}$ , $t_{RP} = t_{RP.MAX}$ ; $\overline{CS}$ is HIGH between valid commands. Address inputs are SWITCHING; Data Bus inputs are SWITCHING;	$I_{DD4W}$	
<b>Burst Refresh Current</b> $t_{CK} = t_{CK.MIN}$ , Refresh command every $t_{RFC} = t_{RFC.MIN}$ interval, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	$I_{DD5B}$	



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Parameter	Symbol	Note 1)2)3)4)5)
<b>Distributed Refresh Current</b> $t_{CK} = t_{CK,MIN}$ ; Refresh command every $t_{RFC} = t_{REFI}$ interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are SWITCHING, Data bus inputs are SWITCHING.	$I_{DD5D}$	
<b>Self-Refresh Current</b> CKE $\leq 0.2$ V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are FLOATING, Data bus inputs are FLOATING. $I_{DD6}$ current values are guaranteed up to $T_{CASE}$ of 85 °C max.	$I_{DD6}$	
<b>All Bank Interleave Read Current</b> All banks are being interleaved at minimum $t_{RC}$ without violating $t_{RRD}$ using a burst length of 4. Control and address bus inputs are STABLE during DESELECTS. $I_{out} = 0$ mA.	$I_{DD7}$	6)

- 1)  $V_{DDQ} = 1.8\text{ V} \pm 0.1\text{ V}$ ;  $V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}$
- 2)  $I_{DD}$  specifications are tested after the device is properly initialized and  $I_{DD}$  parameter are specified with ODT disabled.
- 3) Definitions for  $I_{DD}$  see **Table 19**
- 4) For two rank modules: All active current measurements in the same  $I_{DD}$  current mode. The other rank is in  $I_{DD2P}$  Precharge Power-Down Mode
- 5) For details and notes see the relevant Qimonda component data sheet
- 6)  $I_{DD1}$ ,  $I_{DD4R}$  and  $I_{DD7}$  current measurements are defined with the outputs disabled ( $I_{OUT} = 0$  mA). To achieve this on module level the output buffers can be disabled using an EMRS(1) (Extended Mode Register Command) by setting A12 bit to HIGH.

**TABLE 19**  
Definitions for  $I_{DD}$

Parameter	Description
LOW	$V_{IN} \leq V_{IL(ac),MAX}$ ; HIGH is defined as $V_{IN} \geq V_{IH(ac),MIN}$
STABLE	Inputs are stable at a HIGH or LOW level
FLOATING	Inputs are $V_{REF} = V_{DDQ}/2$
SWITCHING	Inputs are changing between HIGH and LOW every other clock (once per 2 cycles) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per cycle) for DQ signals not including mask or strobes



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**TABLE 20**

**$I_{DD}$  Specification for HYS72T[64/128/256]xx0HP-3S-A**

Product Type	HYS72T64000HP-3S-A	HYS72T128000HP-3S-A	HYS72T128020HP-3S-A	HYS72T256220HP-3S-A	HYS72T256040HP-3S-A	Units	Note <sup>1)</sup>
<b>Organization</b>	<b>512 MB</b>	<b>1 GB</b>	<b>1 GB</b>	<b>2 GB</b>	<b>2 GB</b>		
	<b>×72</b>	<b>×72</b>	<b>×72</b>	<b>×72</b>	<b>×72</b>		
	<b>1 Ranks</b>	<b>1 Ranks</b>	<b>2 Ranks</b>	<b>2 Ranks</b>	<b>4 Ranks</b>		
	<b>-3S</b>	<b>-3S</b>	<b>-3S</b>	<b>-3S</b>	<b>-3S</b>		
$I_{DD0}$	1020	1870	1280	1960	1370	mA	2)
$I_{DD1}$	1150	2130	1410	2220	1500	mA	2)
$I_{DD2P}$	430	690	690	780	780	mA	3)
$I_{DD2N}$	840	1500	1500	2400	2400	mA	3)
$I_{DD2Q}$	750	1320	1320	2040	2040	mA	3)
$I_{DD3P\_0}$ (fast)	560	940	940	1280	1280	mA	3)
$I_{DD3P\_1}$ (slow)	440	700	700	810	810	mA	3)4)
$I_{DD3N}$	840	1500	1500	2400	2400	mA	3)5)
$I_{DD4R}$	1560	2940	1810	3030	1900	mA	2)
$I_{DD4W}$	1650	3120	1900	3210	1990	mA	2)
$I_{DD5B}$	1650	3120	1900	3210	1990	mA	2)
$I_{DD5D}$	440	700	700	810	810	mA	3)6)
$I_{DD6}$	45	90	90	180	180	mA	3)6)
$I_{DD7}$	1710	3240	1960	3330	2050	mA	2)

1) Module  $I_{DD}$  is calculated on the basis of component  $I_{DD}$  and includes currents of Registers and PLL. ODT disabled.  $I_{DD1}$ ,  $I_{DD4R}$ , and  $I_{DD7}$ , are defined with the outputs disabled.

2) The other rank is in  $I_{DD2P}$  Precharge Power-Down Current mode

3) Both ranks are in the same  $I_{DD}$  current mode

4) Fast: MRS(12)=0

5) Slow: MRS(12)=1

6)  $I_{DD5D}$  and  $I_{DD6}$  values are for  $0^{\circ}\text{C} \leq T_{\text{Case}} \leq 85^{\circ}\text{C}$



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**TABLE 21**

**$I_{DD}$  Specification for HYS72T[64/128/256]xx0HP-3.7-A**

Product Type	HYS72T64000HP-3.7-A	HYS72T128000HP-3.7-A	HYS72T128020HP-3.7-A	HYS72T256220HP-3.7-A	HYS72T256040HP-3.7-A	Units	Note <sup>1)</sup>
<b>Organization</b>	<b>512 MB</b>	<b>1 GB</b>	<b>1 GB</b>	<b>2 GB</b>	<b>2 GB</b>		
	<b>×72</b>	<b>×72</b>	<b>×72</b>	<b>×72</b>	<b>×72</b>		
	<b>1 Ranks</b>	<b>1 Ranks</b>	<b>2 Ranks</b>	<b>2 Ranks</b>	<b>4 Ranks</b>		
	<b>-3.7</b>	<b>-3.7</b>	<b>-3.7</b>	<b>-3.7</b>	<b>-3.7</b>		
$I_{DD0}$	920	1670	1120	1740	1370	mA	2)
$I_{DD1}$	1010	1850	1210	1920	1500	mA	2)
$I_{DD2P}$	370	570	570	640	780	mA	3)
$I_{DD2N}$	690	1220	1220	1940	2400	mA	3)
$I_{DD2Q}$	600	1040	1040	1580	2040	mA	3)
$I_{DD3P\_0}$ (fast)	470	790	790	1080	1280	mA	3)
$I_{DD3P\_1}$ (slow)	380	590	590	680	810	mA	3)4)
$I_{DD3N}$	690	1220	1220	1940	2400	mA	3)5)
$I_{DD4R}$	1140	2120	1350	2190	1900	mA	2)
$I_{DD4W}$	1190	2210	1390	2280	1990	mA	2)
$I_{DD5B}$	1500	2840	1710	2910	1990	mA	2)
$I_{DD5D}$	380	610	610	720	810	mA	3)6)
$I_{DD6}$	36	72	72	144	180	mA	3)6)
$I_{DD7}$	1590	3030	1800	3100	2050	mA	2)

- 1) Module  $I_{DD}$  is calculated on the basis of component  $I_{DD}$  and includes currents of Registers and PLL. ODT disabled.  $I_{DD1}$ ,  $I_{DD4R}$ , and  $I_{DD7}$ , are defined with the outputs disabled.
- 2) The other rank is in  $I_{DD2P}$  Precharge Power-Down Current mode
- 3) Both ranks are in the same  $I_{DD}$  current mode
- 4) Fast: MRS(12)=0
- 5) Slow: MRS(12)=1
- 6)  $I_{DD5D}$  and  $I_{DD6}$  values are for  $0^{\circ}\text{C} \leq T_{\text{Case}} \leq 85^{\circ}\text{C}$



# 4 SPD Codes

This chapter lists all hexadecimal byte values stored in the EEPROM of the products described in this data sheet. SPD stands for serial presence detect. All values with XX in the table are module specific bytes which are defined during production.

### List of SPD Code Tables

- Table 22 “HYS72T[64/128/256]xx0HP-3S-A” on Page 31
- Table 23 “HYS72T[64/128/256]xx0HP-3.7-A” on Page 36

**TABLE 22**

**HYS72T[64/128/256]xx0HP-3S-A**

Product Type		HYS72T64000HP-3S-A	HYS72T128000HP-3S-A	HYS72T128020HP-3S-A	HYS72T256220HP-3S-A	HYS72T256040HP-3S-A
Organization		512MB ×72 1 Rank (×8)	1 GByte ×72 1 Rank (×4)	1 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×4)	2 GByte ×72 4 Ranks (×8)
Label Code		PC2-5300P-555	PC2-5300P-555	PC2-5300P-555	PC2-5300P-555	PC2-5300P-555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08	08
3	Number of Row Addresses	0E	0E	0E	0E	0E
4	Number of Column Addresses	0A	0B	0A	0B	0A
5	DIMM Rank and Stacking Information	60	60	61	61	63
6	Data Width	48	48	48	48	48
7	Not used	00	00	00	00	00
8	Interface Voltage Level	05	05	05	05	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	30	30	30	30	30
10	$t_{AC}$ SDRAM @ $CL_{MAX}$ (Byte 18) [ns]	45	45	45	45	45
11	Error Correction Support (non-ECC, ECC)	06	06	06	06	06



HYS72T[64/128/256]xx0HP-[3S/3.7]-A  
Registered DDR2 SDRAM Modules

Product Type		HYS72T64000HP-3S-A	HYS72T128000HP-3S-A	HYS72T128020HP-3S-A	HYS72T256220HP-3S-A	HYS72T256040HP-3S-A
Organization		512MB	1 GByte	1 GByte	2 GByte	2 GByte
		x72	x72	x72	x72	x72
		1 Rank (x8)	1 Rank (x4)	2 Ranks (x8)	2 Ranks (x4)	4 Ranks (x8)
Label Code		PC2-5300P-555	PC2-5300P-555	PC2-5300P-555	PC2-5300P-555	PC2-5300P-555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX	HEX
12	Refresh Rate and Type	82	82	82	82	82
13	Primary SDRAM Width	08	04	08	04	08
14	Error Checking SDRAM Width	08	04	08	04	08
15	Not used	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	Supported CAS Latencies	38	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01	01
20	DIMM Type Information	01	01	01	01	01
21	DIMM Attributes	04	05	05	07	07
22	Component Attributes	03	03	03	03	03
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	3D	3D	3D	3D	3D
24	$t_{AC}$ SDRAM @ $CL_{MAX} -1$ [ns]	50	50	50	50	50
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50	50	50	50	50
26	$t_{AC}$ SDRAM @ $CL_{MAX} -2$ [ns]	60	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D	2D
31	Module Density per Rank	80	01	80	01	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	20	20	20	20	20
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	27	27	27	27	27
34	$t_{DS.MIN}$ [ns]	10	10	10	10	10
35	$t_{DH.MIN}$ [ns]	17	17	17	17	17





HYS72T[64/128/256]xx0HP-[3S/3.7]-A  
Registered DDR2 SDRAM Modules

Product Type		HYS72T64000HP-3S-A	HYS72T128000HP-3S-A	HYS72T128020HP-3S-A	HYS72T256220HP-3S-A	HYS72T256040HP-3S-A
Organization		512MB	1 GByte	1 GByte	2 GByte	2 GByte
		x72	x72	x72	x72	x72
		1 Rank (x8)	1 Rank (x4)	2 Ranks (x8)	2 Ranks (x4)	4 Ranks (x8)
Label Code		PC2-5300P-555	PC2-5300P-555	PC2-5300P-555	PC2-5300P-555	PC2-5300P-555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX	HEX
36	$t_{WR,MIN}$ [ns]	3C	3C	3C	3C	3C
37	$t_{WTR,MIN}$ [ns]	1E	1E	1E	1E	1E
38	$t_{RTP,MIN}$ [ns]	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00
40	$t_{RC}$ and $t_{RFC}$ Extension	00	00	00	00	00
41	$t_{RC,MIN}$ [ns]	3C	3C	3C	3C	3C
42	$t_{RFC,MIN}$ [ns]	69	69	69	69	69
43	$t_{CK,MAX}$ [ns]	80	80	80	80	80
44	$t_{DQSQ,MAX}$ [ns]	18	18	18	18	18
45	$t_{QHS,MAX}$ [ns]	22	22	22	22	22
46	PLL Relock Time	0F	0F	0F	0F	0F
47	$T_{CASE,MAX}$ Delta / $\Delta T_{4R4W}$ Delta	53	53	53	53	53
48	Psi(T-A) DRAM	78	78	78	78	78
49	$\Delta T_0$ (DT0)	4B	4B	4B	4B	4B
50	$\Delta T_{2N}$ (DT2N, UDIMM) or $\Delta T_{2Q}$ (DT2Q, RDIMM)	2E	2E	2E	2E	2E
51	$\Delta T_{2P}$ (DT2P)	26	26	26	26	26
52	$\Delta T_{3N}$ (DT3N)	26	26	26	26	26
53	$\Delta T_{3P,fast}$ (DT3P fast)	2B	2B	2B	2B	2B
54	$\Delta T_{3P,slow}$ (DT3P slow)	1B	1B	1B	1B	1B
55	$\Delta T_{4R}$ (DT4R) / $\Delta T_{4R4W}$ Sign (DT4R4W)	4A	4A	4A	4A	4A
56	$\Delta T_{5B}$ (DT5B)	20	20	20	20	20
57	$\Delta T_7$ (DT7)	22	22	22	22	22
58	Psi(ca) PLL	C4	C4	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C	8C	8C



HYS72T[64/128/256]xx0HP-[3S/3.7]-A  
Registered DDR2 SDRAM Modules

Product Type		HYS72T64000HP-3S-A	HYS72T128000HP-3S-A	HYS72T128020HP-3S-A	HYS72T256220HP-3S-A	HYS72T256040HP-3S-A
Organization		512MB	1 GByte	1 GByte	2 GByte	2 GByte
		×72	×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)	2 Ranks (×4)	4 Ranks (×8)
Label Code		PC2-5300P-555	PC2-5300P-555	PC2-5300P-555	PC2-5300P-555	PC2-5300P-555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX	HEX
60	$\Delta T_{PLL}$ (DTPLL)	68	68	68	68	68
61	$\Delta T_{REG}$ (DTREG) / Toggle Rate	94	94	94	94	94
62	SPD Revision	12	12	12	12	12
63	Checksum of Bytes 0-62	47	C2	49	C5	4D
64	Manufacturer's JEDEC ID Code (1)	7F	7F	7F	7F	7F
65	Manufacturer's JEDEC ID Code (2)	7F	7F	7F	7F	7F
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F	7F	7F
69	Manufacturer's JEDEC ID Code (6)	51	51	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx
73	Product Type, Char 1	37	37	37	37	37
74	Product Type, Char 2	32	32	32	32	32
75	Product Type, Char 3	54	54	54	54	54
76	Product Type, Char 4	36	31	31	32	32
77	Product Type, Char 5	34	32	32	35	35
78	Product Type, Char 6	30	38	38	36	36
79	Product Type, Char 7	30	30	30	32	30
80	Product Type, Char 8	30	30	32	32	34
81	Product Type, Char 9	48	30	30	30	30
82	Product Type, Char 10	50	48	48	48	48
83	Product Type, Char 11	33	50	50	50	50



HYS72T[64/128/256]xx0HP-[3S/3.7]-A  
Registered DDR2 SDRAM Modules

Product Type		HYS72T64000HP-3S-A	HYS72T128000HP-3S-A	HYS72T128020HP-3S-A	HYS72T256220HP-3S-A	HYS72T256040HP-3S-A
Organization		512MB	1 GByte	1 GByte	2 GByte	2 GByte
		×72	×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)	2 Ranks (×4)	4 Ranks (×8)
Label Code		PC2- 5300P- 555	PC2- 5300P- 555	PC2- 5300P- 555	PC2- 5300P- 555	PC2- 5300P- 555
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX	HEX
84	Product Type, Char 12	53	33	33	33	33
85	Product Type, Char 13	41	53	53	53	53
86	Product Type, Char 14	20	41	41	41	41
87	Product Type, Char 15	20	20	20	20	20
88	Product Type, Char 16	20	20	20	20	20
89	Product Type, Char 17	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20
91	Module Revision Code	2x	2x	2x	2x	2x
92	Test Program Revision Code	xx	xx	xx	xx	xx
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00
128 - 255	Blank for customer use	FF	FF	FF	FF	FF



HYS72T[64/128/256]xx0HP-[3S/3.7]-A  
Registered DDR2 SDRAM Modules

**TABLE 23**  
**HYS72T[64/128/256]xx0HP-3.7-A**

Product Type		HYS72T64000HP-3.7-A	HYS72T128000HP-3.7-A	HYS72T128020HP-3.7-A	HYS72T256220HP-3.7-A	HYS72T256040HP-3.7-A
Organization		512MB	1 GByte	1 GByte	2 GByte	2 GByte
		×72	×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)	2 Ranks (×4)	4 Ranks (×8)
Label Code		PC2-4200P-444	PC2-4200P-444	PC2-4200P-444	PC2-4200P-444	PC2-4200P-444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX	HEX
0	Programmed SPD Bytes in EEPROM	80	80	80	80	80
1	Total number of Bytes in EEPROM	08	08	08	08	08
2	Memory Type (DDR2)	08	08	08	08	08
3	Number of Row Addresses	0E	0E	0E	0E	0E
4	Number of Column Addresses	0A	0B	0A	0B	0A
5	DIMM Rank and Stacking Information	60	60	61	61	63
6	Data Width	48	48	48	48	48
7	Not used	00	00	00	00	00
8	Interface Voltage Level	05	05	05	05	05
9	$t_{CK} @ CL_{MAX}$ (Byte 18) [ns]	3D	3D	3D	3D	3D
10	$t_{AC}$ SDRAM @ $CL_{MAX}$ (Byte 18) [ns]	50	50	50	50	50
11	Error Correction Support (non-ECC, ECC)	06	06	06	06	06
12	Refresh Rate and Type	82	82	82	82	82
13	Primary SDRAM Width	08	04	08	04	08
14	Error Checking SDRAM Width	08	04	08	04	08
15	Not used	00	00	00	00	00
16	Burst Length Supported	0C	0C	0C	0C	0C
17	Number of Banks on SDRAM Device	04	04	04	04	04
18	Supported CAS Latencies	38	38	38	38	38
19	DIMM Mechanical Characteristics	01	01	01	01	01
20	DIMM Type Information	01	01	01	01	01



HYS72T[64/128/256]xx0HP-[3S/3.7]-A  
Registered DDR2 SDRAM Modules

Product Type		HYS72T64000HP-3.7-A	HYS72T128000HP-3.7-A	HYS72T128020HP-3.7-A	HYS72T256220HP-3.7-A	HYS72T256040HP-3.7-A
Organization		512MB	1 GByte	1 GByte	2 GByte	2 GByte
		×72	×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)	2 Ranks (×4)	4 Ranks (×8)
Label Code		PC2-4200P-444	PC2-4200P-444	PC2-4200P-444	PC2-4200P-444	PC2-4200P-444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX	HEX
21	DIMM Attributes	04	05	05	07	07
22	Component Attributes	03	03	03	03	03
23	$t_{CK} @ CL_{MAX} -1$ (Byte 18) [ns]	3D	3D	3D	3D	3D
24	$t_{AC}$ SDRAM @ $CL_{MAX} -1$ [ns]	50	50	50	50	50
25	$t_{CK} @ CL_{MAX} -2$ (Byte 18) [ns]	50	50	50	50	50
26	$t_{AC}$ SDRAM @ $CL_{MAX} -2$ [ns]	60	60	60	60	60
27	$t_{RP.MIN}$ [ns]	3C	3C	3C	3C	3C
28	$t_{RRD.MIN}$ [ns]	1E	1E	1E	1E	1E
29	$t_{RCD.MIN}$ [ns]	3C	3C	3C	3C	3C
30	$t_{RAS.MIN}$ [ns]	2D	2D	2D	2D	2D
31	Module Density per Rank	80	01	80	01	80
32	$t_{AS.MIN}$ and $t_{CS.MIN}$ [ns]	25	25	25	25	25
33	$t_{AH.MIN}$ and $t_{CH.MIN}$ [ns]	37	37	37	37	37
34	$t_{DS.MIN}$ [ns]	10	10	10	10	10
35	$t_{DH.MIN}$ [ns]	22	22	22	22	22
36	$t_{WR.MIN}$ [ns]	3C	3C	3C	3C	3C
37	$t_{WTR.MIN}$ [ns]	1E	1E	1E	1E	1E
38	$t_{RTP.MIN}$ [ns]	1E	1E	1E	1E	1E
39	Analysis Characteristics	00	00	00	00	00
40	$t_{RC}$ and $t_{RFC}$ Extension	00	00	00	00	00
41	$t_{RC.MIN}$ [ns]	3C	3C	3C	3C	3C
42	$t_{RFC.MIN}$ [ns]	69	69	69	69	69
43	$t_{CK.MAX}$ [ns]	80	80	80	80	80
44	$t_{DQSQ.MAX}$ [ns]	1E	1E	1E	1E	1E



HYS72T[64/128/256]xx0HP-[3S/3.7]-A  
Registered DDR2 SDRAM Modules

Product Type		HYS72T64000HP-3.7-A	HYS72T128000HP-3.7-A	HYS72T128020HP-3.7-A	HYS72T256220HP-3.7-A	HYS72T256040HP-3.7-A
Organization		512MB	1 GByte	1 GByte	2 GByte	2 GByte
		×72	×72	×72	×72	×72
		1 Rank (×8)	1 Rank (×4)	2 Ranks (×8)	2 Ranks (×4)	4 Ranks (×8)
Label Code		PC2-4200P-444	PC2-4200P-444	PC2-4200P-444	PC2-4200P-444	PC2-4200P-444
JEDEC SPD Revision		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
Byte#	Description	HEX	HEX	HEX	HEX	HEX
45	$t_{QHS,MAX}$ [ns]	28	28	28	28	28
46	PLL Relock Time	0F	0F	0F	0F	0F
47	$T_{CASE,MAX}$ Delta / $\Delta T_{4R4W}$ Delta	51	51	51	51	51
48	Psi(T-A) DRAM	78	78	78	78	78
49	$\Delta T_0$ (DT0)	3F	3F	3F	3F	3F
50	$\Delta T_{2N}$ (DT2N, UDIMM) or $\Delta T_{2Q}$ (DT2Q, RDIMM)	22	22	22	22	22
51	$\Delta T_{2P}$ (DT2P)	1E	1E	1E	1E	1E
52	$\Delta T_{3N}$ (DT3N)	1E	1E	1E	1E	1E
53	$\Delta T_{3P,fast}$ (DT3P fast)	24	24	24	24	24
54	$\Delta T_{3P,slow}$ (DT3P slow)	17	17	17	17	17
55	$\Delta T_{4R}$ (DT4R) / $\Delta T_{4R4W}$ Sign (DT4R4W)	34	34	34	34	34
56	$\Delta T_{5B}$ (DT5B)	1E	1E	1E	1E	1E
57	$\Delta T_7$ (DT7)	20	20	20	20	20
58	Psi(ca) PLL	C4	C4	C4	C4	C4
59	Psi(ca) REG	8C	8C	8C	8C	8C
60	$\Delta T_{PLL}$ (DTPLL)	61	61	61	61	61
61	$\Delta T_{REG}$ (DTREG) / Toggle Rate	78	78	78	78	78
62	SPD Revision	12	12	12	12	12
63	Checksum of Bytes 0-62	19	94	1B	97	1F
64	Manufacturer's JEDEC ID Code (1)	7F	7F	7F	7F	7F
65	Manufacturer's JEDEC ID Code (2)	7F	7F	7F	7F	7F
66	Manufacturer's JEDEC ID Code (3)	7F	7F	7F	7F	7F
67	Manufacturer's JEDEC ID Code (4)	7F	7F	7F	7F	7F
68	Manufacturer's JEDEC ID Code (5)	7F	7F	7F	7F	7F



HYS72T[64/128/256]xx0HP-[3S/3.7]-A  
Registered DDR2 SDRAM Modules

<b>Product Type</b>		<b>HYS72T64000HP-3.7-A</b>	<b>HYS72T128000HP-3.7-A</b>	<b>HYS72T128020HP-3.7-A</b>	<b>HYS72T256220HP-3.7-A</b>	<b>HYS72T256040HP-3.7-A</b>
<b>Organization</b>		<b>512MB</b>	<b>1 GByte</b>	<b>1 GByte</b>	<b>2 GByte</b>	<b>2 GByte</b>
		<b>×72</b>	<b>×72</b>	<b>×72</b>	<b>×72</b>	<b>×72</b>
		<b>1 Rank (×8)</b>	<b>1 Rank (×4)</b>	<b>2 Ranks (×8)</b>	<b>2 Ranks (×4)</b>	<b>4 Ranks (×8)</b>
<b>Label Code</b>		<b>PC2-4200P-444</b>	<b>PC2-4200P-444</b>	<b>PC2-4200P-444</b>	<b>PC2-4200P-444</b>	<b>PC2-4200P-444</b>
<b>JEDEC SPD Revision</b>		<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>	<b>Rev. 1.2</b>
<b>Byte#</b>	<b>Description</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>	<b>HEX</b>
69	Manufacturer's JEDEC ID Code (6)	51	51	51	51	51
70	Manufacturer's JEDEC ID Code (7)	00	00	00	00	00
71	Manufacturer's JEDEC ID Code (8)	00	00	00	00	00
72	Module Manufacturer Location	xx	xx	xx	xx	xx
73	Product Type, Char 1	37	37	37	37	37
74	Product Type, Char 2	32	32	32	32	32
75	Product Type, Char 3	54	54	54	54	54
76	Product Type, Char 4	36	31	31	32	32
77	Product Type, Char 5	34	32	32	35	35
78	Product Type, Char 6	30	38	38	36	36
79	Product Type, Char 7	30	30	30	32	30
80	Product Type, Char 8	30	30	32	32	34
81	Product Type, Char 9	48	30	30	30	30
82	Product Type, Char 10	50	48	48	48	48
83	Product Type, Char 11	33	50	50	50	50
84	Product Type, Char 12	2E	33	33	33	33
85	Product Type, Char 13	37	2E	2E	2E	2E
86	Product Type, Char 14	41	37	37	37	37
87	Product Type, Char 15	20	41	41	41	41
88	Product Type, Char 16	20	20	20	20	20
89	Product Type, Char 17	20	20	20	20	20
90	Product Type, Char 18	20	20	20	20	20
91	Module Revision Code	2x	2x	2x	2x	2x
92	Test Program Revision Code	xx	xx	xx	xx	xx



HYS72T[64/128/256]xx0HP-[3S/3.7]-A  
Registered DDR2 SDRAM Modules

<b>Product Type</b>		HYS72T64000HP-3.7-A	HYS72T128000HP-3.7-A	HYS72T128020HP-3.7-A	HYS72T256220HP-3.7-A	HYS72T256040HP-3.7-A
<b>Organization</b>		512MB ×72 1 Rank (×8)	1 GByte ×72 1 Rank (×4)	1 GByte ×72 2 Ranks (×8)	2 GByte ×72 2 Ranks (×4)	2 GByte ×72 4 Ranks (×8)
<b>Label Code</b>		PC2-4200P-444	PC2-4200P-444	PC2-4200P-444	PC2-4200P-444	PC2-4200P-444
<b>JEDEC SPD Revision</b>		Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2	Rev. 1.2
<b>Byte#</b>	<b>Description</b>	HEX	HEX	HEX	HEX	HEX
93	Module Manufacturing Date Year	xx	xx	xx	xx	xx
94	Module Manufacturing Date Week	xx	xx	xx	xx	xx
95 - 98	Module Serial Number	xx	xx	xx	xx	xx
99 - 127	Not used	00	00	00	00	00
128 - 255	Blank for customer use	FF	FF	FF	FF	FF

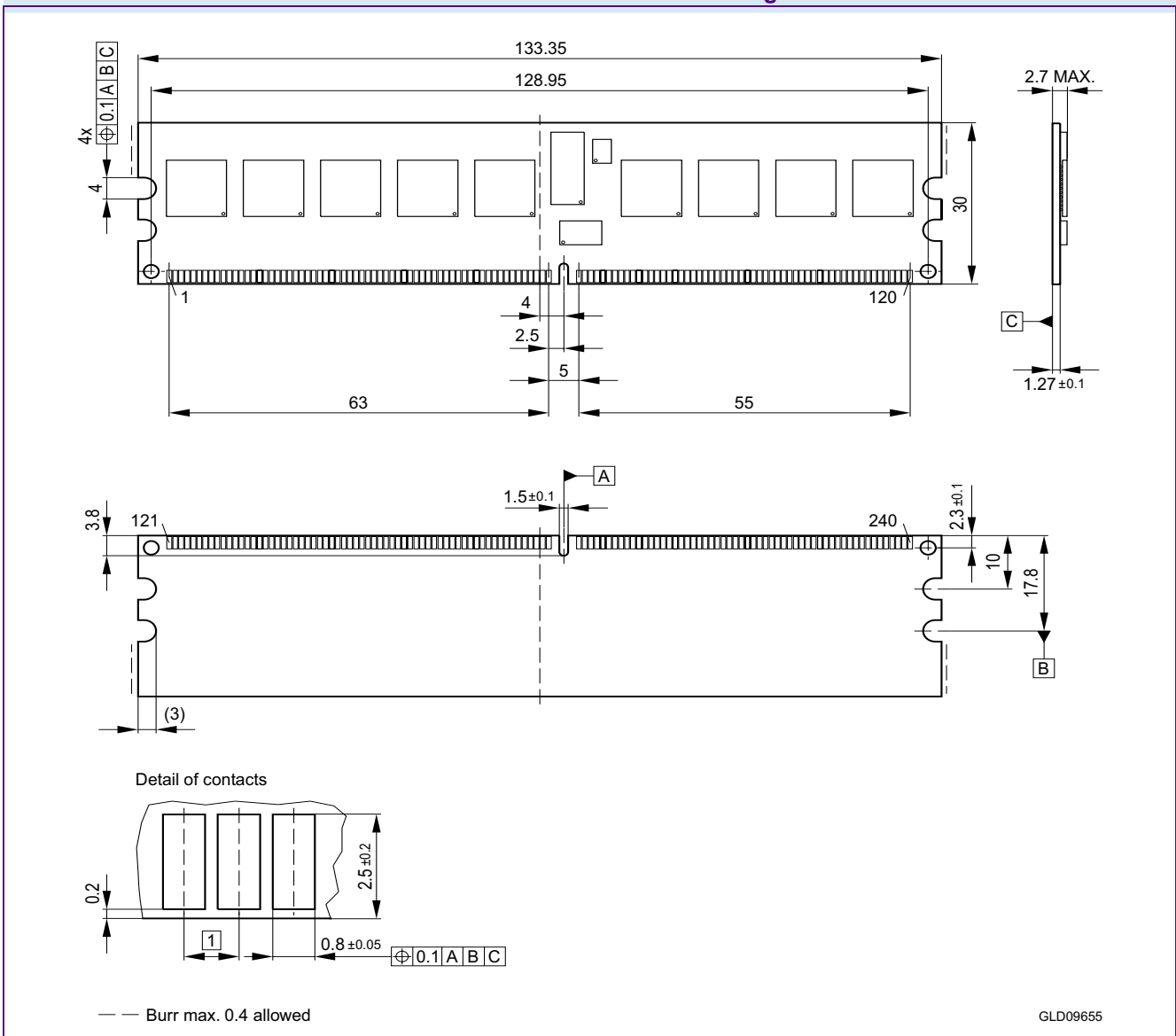




# 5 Package Outlines

This chapter contains the package outlines of the products.

**FIGURE 5**  
Package Outline Raw Card F L-DIM-240-11

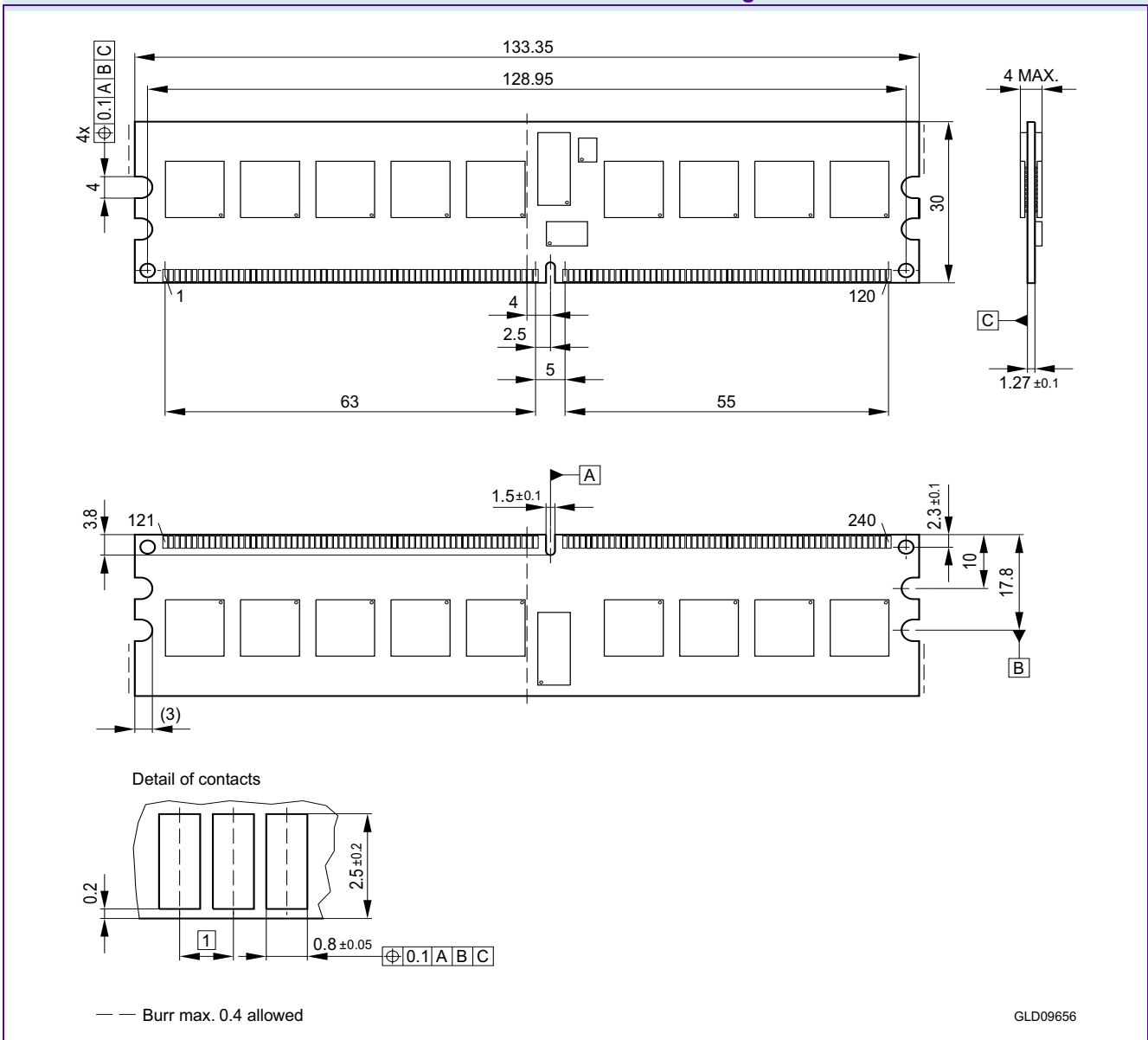


## Notes

1. Drawing according to ISO 8015
2. Dimensions in mm
3. General tolerances +/- 0.15



**FIGURE 6**  
Package Outline Raw Card G L-DIM-240-12

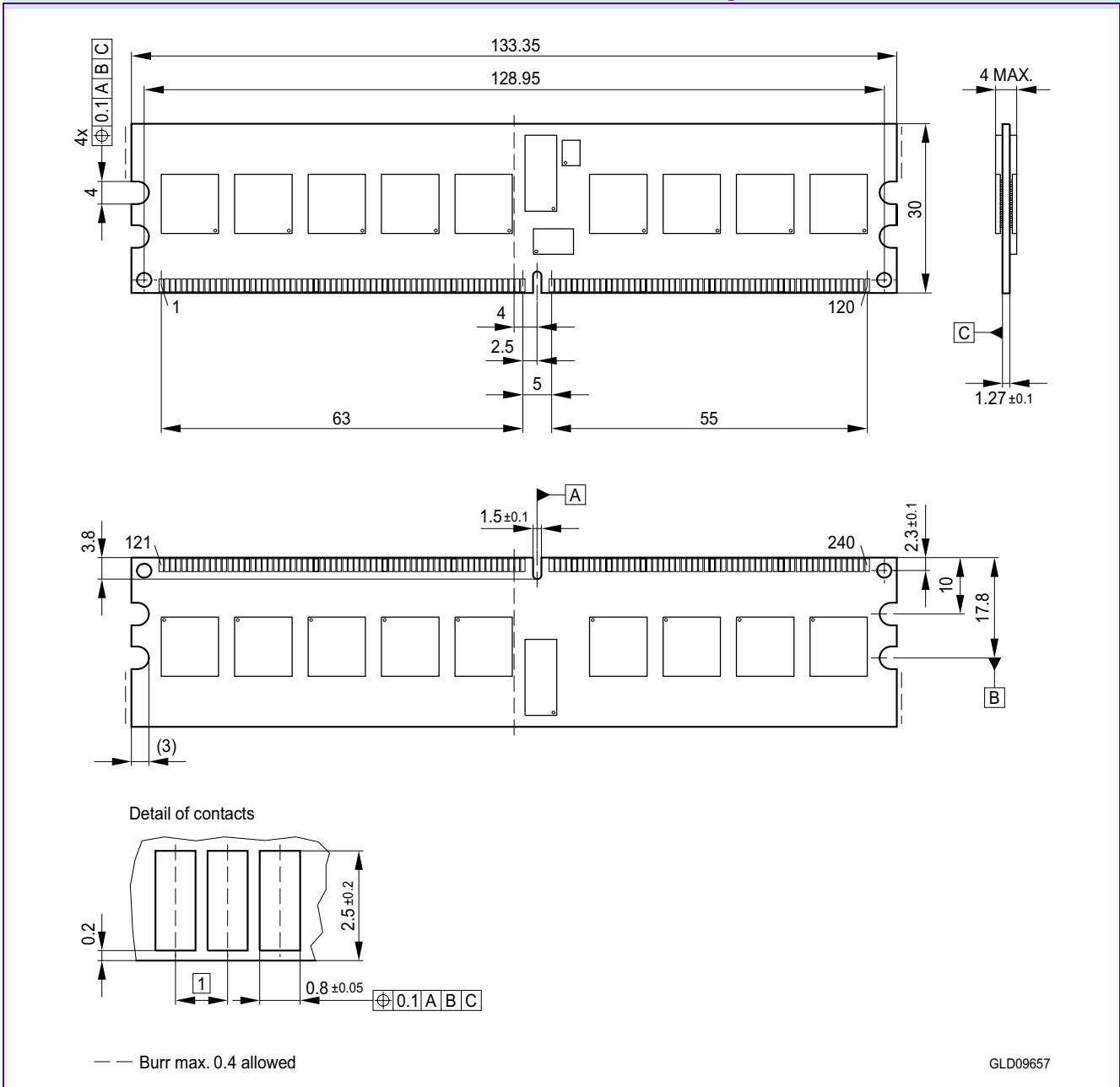


**Notes**

- 1. Drawing according to ISO 8015
- 2. Dimensions in mm
- 3. General tolerances +/- 0.15



**FIGURE 7**  
Package Outline Raw Card H L-DIM-240-13



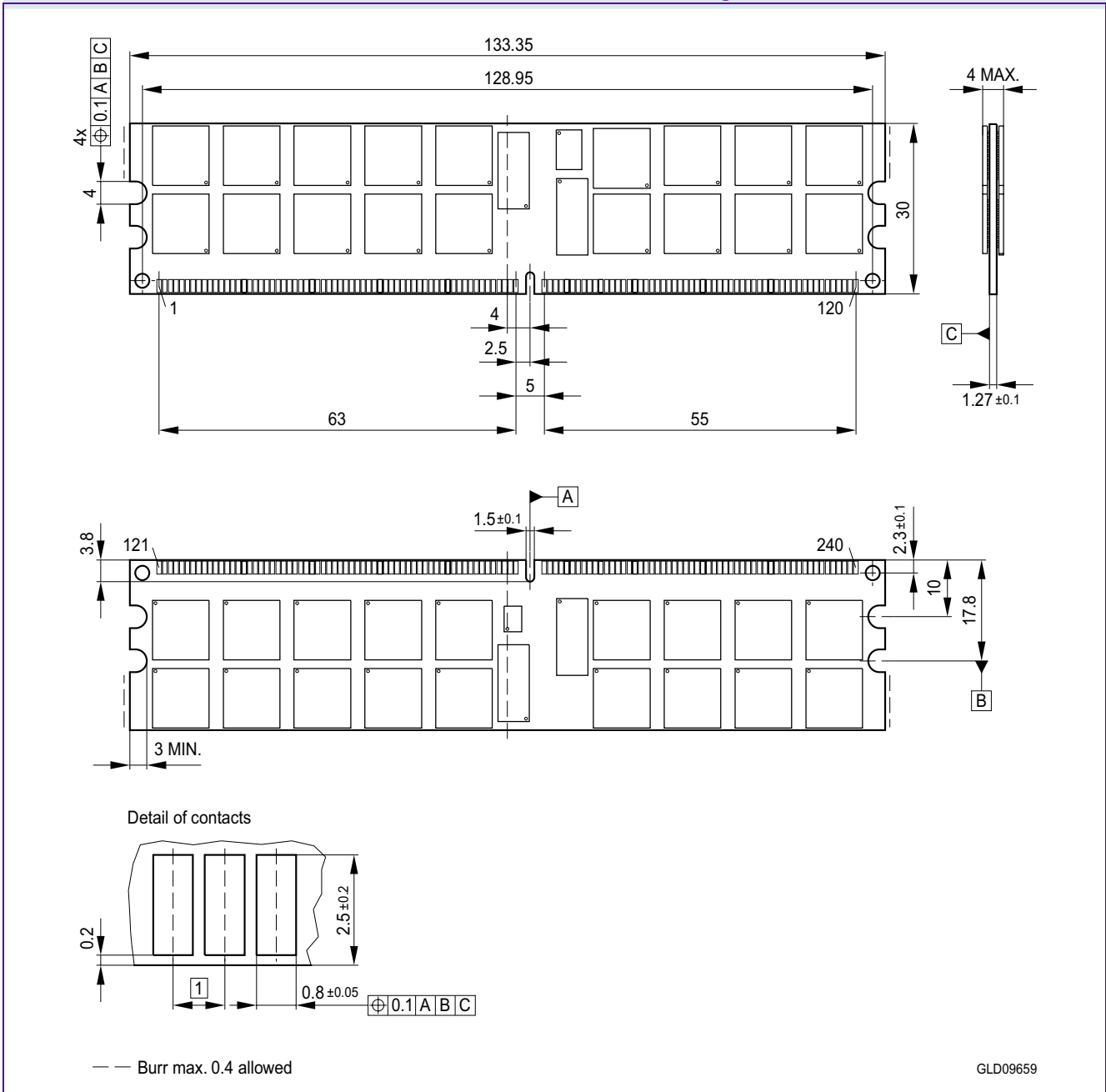
**Notes**

1. Drawing according to ISO 8015
2. Dimensions in mm
3. General tolerances +/- 0.15



HYS72T[64/128/256]xx0HP-[3S/3.7]-A  
Registered DDR2 SDRAM Modules

**FIGURE 8**  
Package Outline Raw Card J L-DIM-240-20

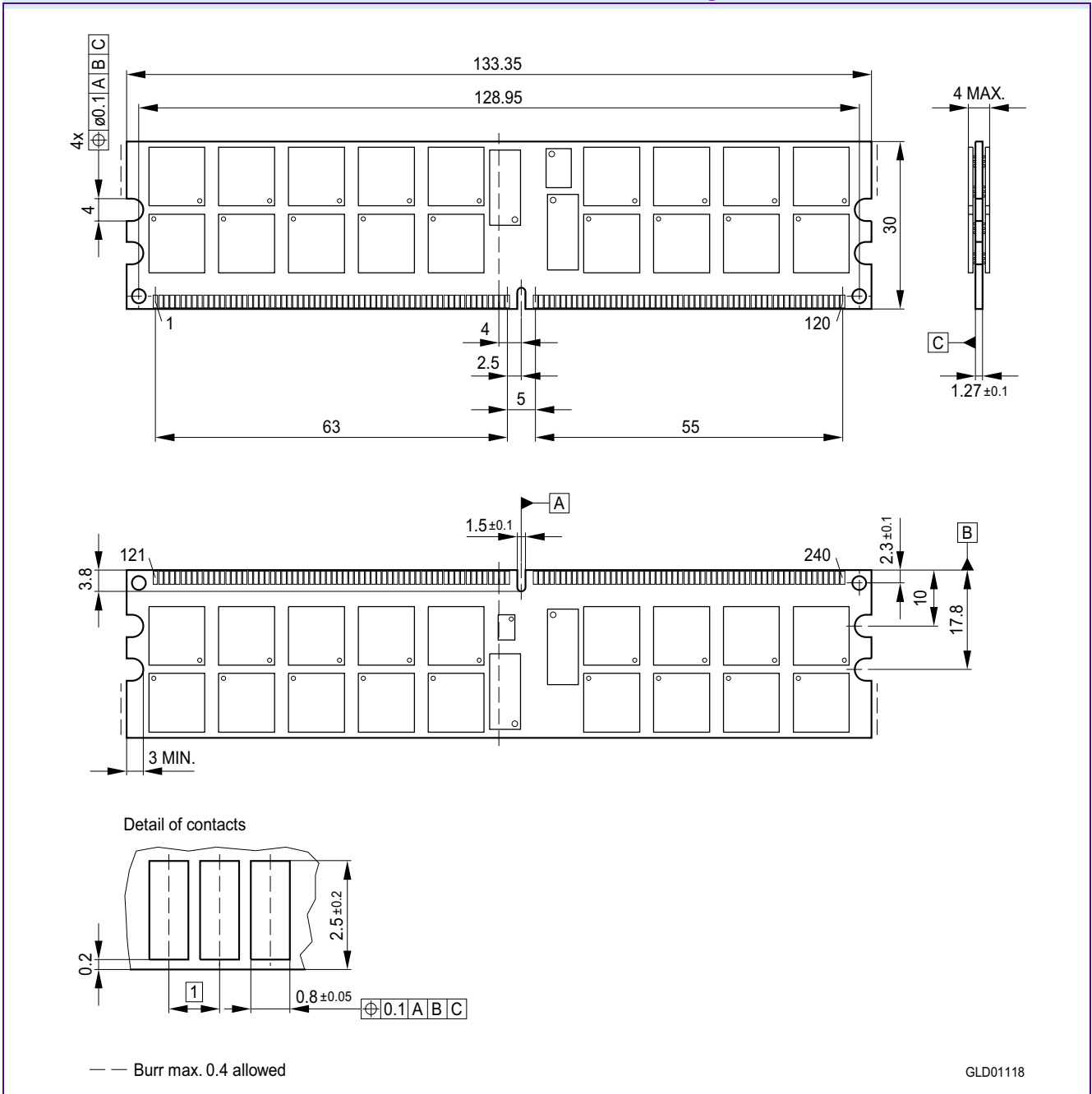


**Notes**

1. Drawing according to ISO 8015
2. Dimensions in mm
3. General tolerances +/- 0.15



**FIGURE 9**  
Package Outline Raw Card N L-DIM-240-44



**Notes**

1. Drawing according to ISO 8015
2. Dimensions in mm
3. General tolerances +/- 0.15



# 6 Product Type Nomenclature

Qimonda's nomenclature uses simple coding combined with some proprietary coding. **Table 24** provides examples for module and component product type number as well as the

field number. The detailed field description together with possible values and coding explanation is listed for modules in **Table 25** and for components in **Table 26**.

**TABLE 24**  
Nomenclature Fields and Examples

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
Micro-DIMM	HYS	64	T	64/128	0	2	0	K	M	-5	-A
DDR2 DRAM	HYB	18	T	512/1G	16		0	A	C	-5	

**TABLE 25**  
DDR2 DIMM Nomenclature

Field	Description	Values	Coding
1	Qimonda Module Prefix	HYS	Constant
2	Module Data Width [bit]	64	Non-ECC
		72	ECC
3	DRAM Technology	T	DDR2
4	Memory Density per I/O [Mbit]; Module Density <sup>1)</sup>	32	256 MByte
		64	512 MByte
		128	1 GByte
		256	2 GByte
		512	4 GByte
5	Raw Card Generation	0 .. 9	Look up table
6	Number of Module Ranks	0, 2, 4	1, 2, 4
7	Product Variations	0 .. 9	Look up table
8	Package, Lead-Free Status	A .. Z	Look up table
9	Module Type	D	SO-DIMM
		M	Micro-DIMM
		R	Registered
		U	Unbuffered
		F	Fully Buffered



HYS72T[64/128/256]xx0HP-[3S/3.7]-A  
Registered DDR2 SDRAM Modules

Field	Description	Values	Coding
10	Speed Grade	-2.5F	PC2-6400 5-5-5
		-2.5	PC2-6400 6-6-6
		-3	PC2-5300 4-4-4
		-3S	PC2-5300 5-5-5
		-3.7	PC2-4200 4-4-4
		-5	PC2-3200 3-3-3
11	Die Revision	-A	First
		-B	Second

1) Multiplying “Memory Density per I/O” with “Module Data Width” and dividing by 8 for Non-ECC and 9 for ECC modules gives the overall module memory density in MBytes as listed in column “Coding”.

**TABLE 26**  
DDR2 DRAM Nomenclature

Field	Description	Values	Coding
1	Qimonda Component Prefix	HYB	Constant
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	Look up table
8	Die Revision	A	First
		B	Second
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Speed Grade	-25F	DDR2-800 5-5-5
		-2.5	DDR2-800 6-6-6
		-3	DDR2-667 4-4-4
		-3S	DDR2-667 5-5-5
		-3.7	DDR2-533 4-4-4
		-5	DDR2-400 3-3-3



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