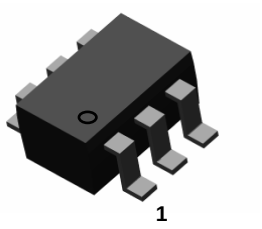
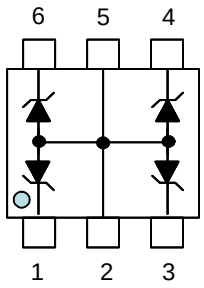
PANJIT SEMI CONDUCTOR

PRELIMINARY

QUAD TVS/ZENER ARRAY FOR ESD AND LATCH-UP PROTECTION

This Quad TVS/Zener Array family have been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating in the 3.0Vdc. This TVS array offers an integrated solution to protect up to 4 data lines where the board space is a premium.





SOT23-6L

SPECIFICATION FEATURES

- **150W (8/20µs), 24W (10/1000µs) Power Dissipation**
- **Low Leakage Current, Maximum of 2µA at rated voltage**
- **Very Low Clamping Voltage**
- **IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance**
- **Industry Standard Surface Mount Package SOT23-6L**
- **100% Tin Matte Finish (RoHS Compliance)**

APPLICATIONS

- **Personal Digital Assistant (PDA)**
- **SIM Card Port Protection (Mobile Phone)**
- **Portable Instrumentation**
- **Mobile Phones and Accessories**
- **Memory Card Port Protection**

MAXIMUM RATINGS (Per Device)

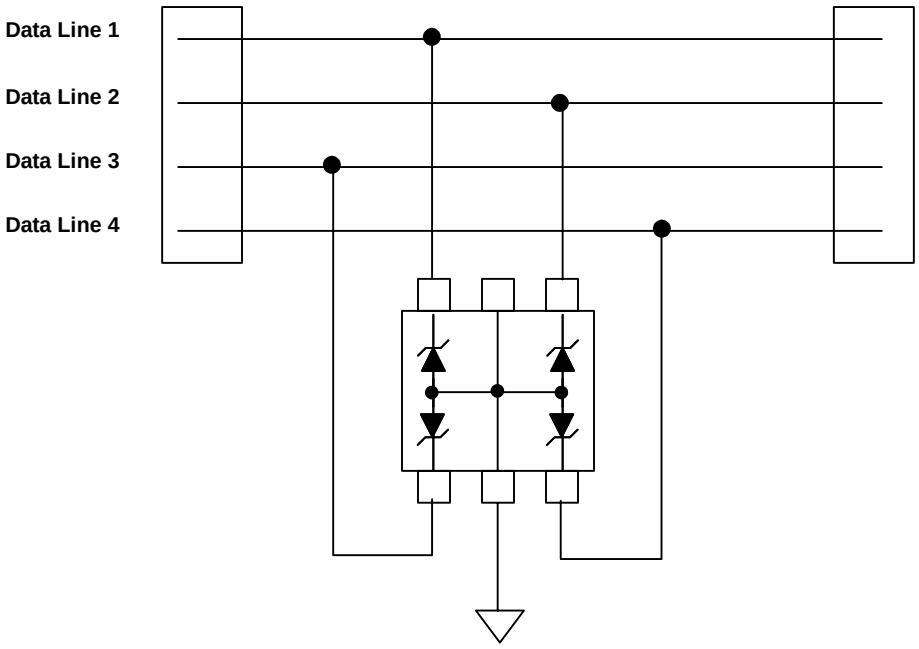
Rating	Symbol	Value	Units
Peak Pulse Power (8/20µs Waveform)	P_{pp}	150	W
ESD Voltage (HBM)	V_{ESD}	25	kV
Operating Temperature Range	T_J	-55 to +150	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				3.0	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1 mA	5.3	5.6	5.88	V
Reverse Leakage Current	I_R	V_R = 3.0V			2	µA
Clamping Voltage (8/20µs)	V_c	I_{pp} = 5 Amps			8	V
Clamping Voltage (8/20µs)	V_c	I_{pp} = 10 Amps			9.5	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 2,5			250	pF
Off State Junction Capacitance	Cj	3 Vdc Bias f = 1MHz Between I/O pins and pin 2,5			160	pF

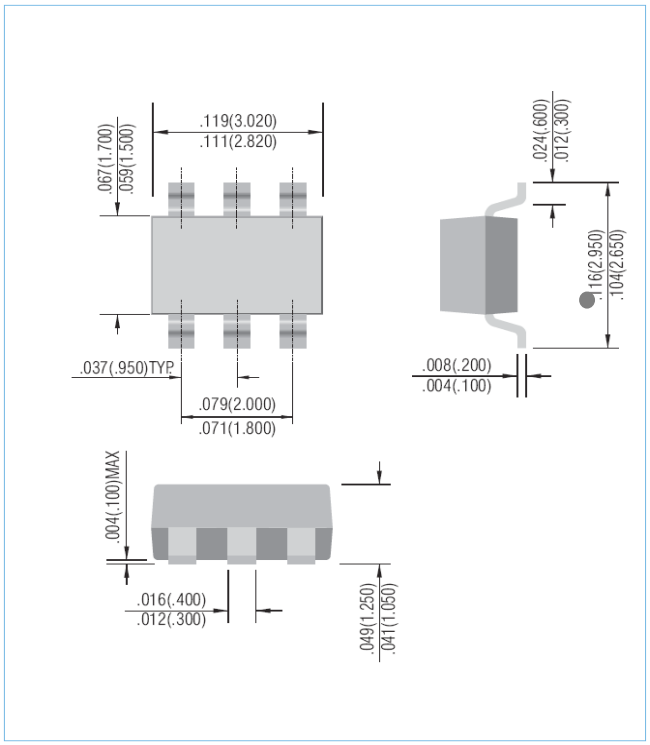
PRELIMINARY

TYPICAL APPLICATION EXAMPLE AND PACKAGE DIMENSIONS



Ground (Pins 2 and 5)

SOT-23-6L Unit: inch (mm)



SOT23-6L Unit: inch (mm)