

FIVE BI-DIRECTIONAL TVS ARRAY FOR ESD PROTECTION

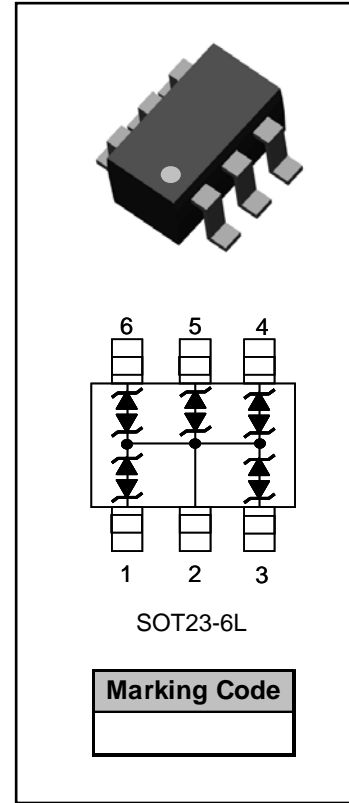
This Penta TVS Array has been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5Vdc and below. This TVS array offers an integrated solution to protect up to 5 data lines where the board space is a premium.

SPECIFICATION FEATURES

- 80W Power Dissipation (8/20μs Waveform)
- Low Leakage Current, Maximum of 1μA @ 5Vdc
- Very low Clamping voltage
- IEC61000-4-2 ESD 15kV air, 8kV Contact Compliance
- Industry standard SOT23-6L
- 100% Tin Matte Finish (RoHS Compliant)

APPLICATIONS

- Video I/O ports protection
- Set Top Boxes
- Portable Instrumentation



MAXIMUM RATINGS

Rating	Symbol	Value	Units
Peak Pulse Power (8/20μs Waveform)	P_{pp}	80	W
Peak Pulse Current (8/20μs Waveform)	I_{pp}	5.0	A
ESD Voltage (HBM)	V_{ESD}	>25	kV
Operating Temperature Range	T_J	-55 to +150	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

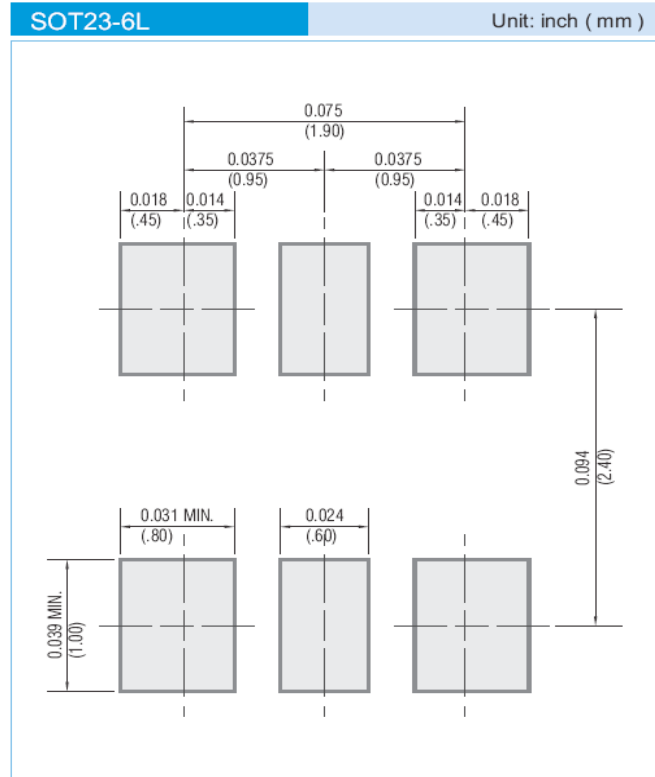
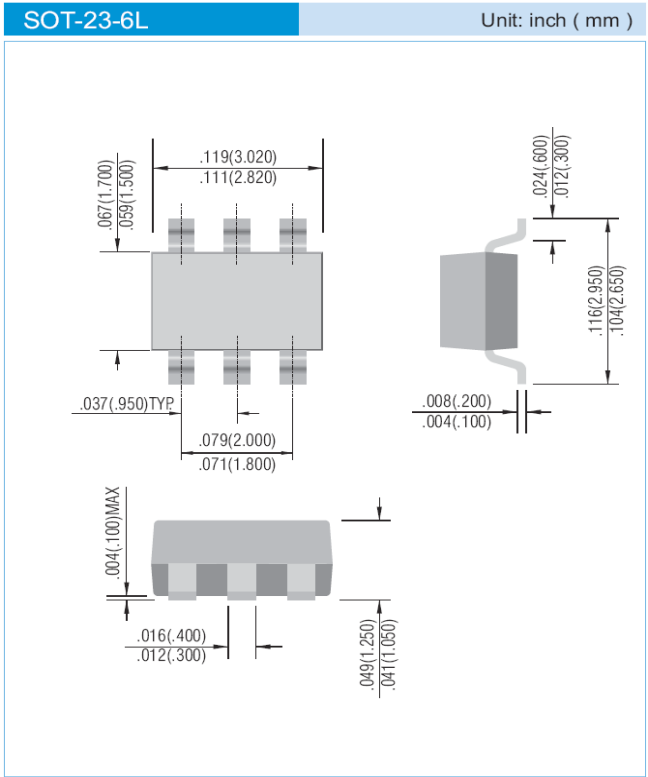
ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				5.0	V
Reverse Breakdown Voltage	V_{BR}	$I_{BR} = 1\text{mA}$	6.2		8.0	V
Reverse Leakage Current	I_R	$V_R = 5\text{V}$			1	μA
Clamping Voltage (8/20μs)	V_c	$I_{pp} = 1\text{A}$			12	V
Clamping Voltage (8/20μs)	V_c	$I_{pp} = 4\text{A}$			15	V
Off State Junction Capacitance	C_j	0 Vdc Bias f = 1MHz Between I/O pins and pin 2			15	pF
Off State Junction Capacitance	C_j	5 Vdc Bias f = 1MHz Between I/O pins and pin 2			7	pF



PACKAGE LAYOUT DIMENSIONS

DRAFT SPEC



© Copyright PanJit International, Inc 2006

The information presented in this document is believed to be accurate and reliable. The specifications and information herein are subject to change without notice. Pan Jit makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose. Pan Jit products are not authorized for use in life support devices or systems. Pan Jit does not convey any license under its patent rights or rights of others.