SC251
Step-down DC-DC Converter with Bias LDO for WCDMA Amplifiers

Description

The SC251 is a synchronous step-down converter designed for use as an adaptive voltage supply for WCDMA RF power amplifiers (PAs). An analog control input is used to adjust the output voltage dynamically between 0.5V and 3.4V using a non-linear transfer function. The non-linear relationship maximizes total system efficiency by providing the PA with the minimum voltage it needs to maintain linearity. For output voltages greater than 3.4V the input is connected directly to the output via an internal PMOS switch. An optional gate drive (GD) output to control an external low on-resistance PMOS switch is also provided for systems applications that require minimal voltage drop. The SC251 also provides a 2.85V LDO reference output that can be used to supply a PA bias input.

Low power and high power modes are provided to match performance with dual mode PAs. In low power mode the output voltage follows an exponential relationship with the VDAC input until it reaches 3.4V. When the VMODE pin changes state, V_{OUT} follows an alternate exponential relationship.

The SC251 is capable of supplying output current up to 800mA. Standby current is <1µA when the device is disabled. The internal clock runs at 1MHz so that small surface mount inductors and capacitors can be used.

Features

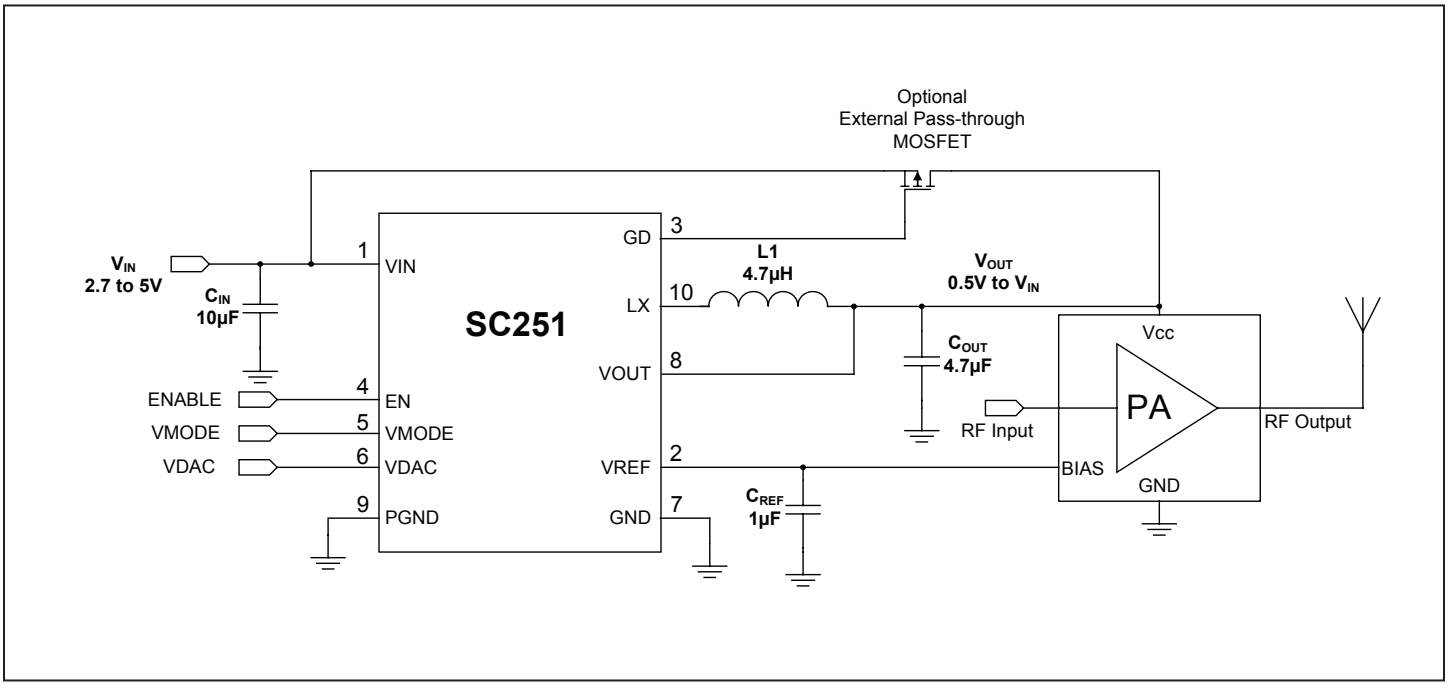
- V_{OUT} exponentially proportional to V_{DAC} for maximum efficiency (patent pending)
- Output range and pass-through mode - 0.5V to 3.4V
- Output current - 800mA
- Shutdown current - < 1µA
- LDO PA bias supply - 2.85V, 10mA
- Internal clock - 1MHz
- Continuous short circuit protection on VOUT
- Duty cycle mode - 100%
- Internal PMOS bypass transistor
- Gate drive available for external bypass transistor
- Over 90% efficiency
- Low and high power modes for optimum dual-mode PA efficiency
- Switching time (lowest to highest output) < 40µs
- Micro-lead frame package MLPD-10, 3mm x 3mm

Applications

- 3G mobile phones - RF PA power supply
- WCDMA power amplifier modules
- Wireless modems

Typical Application Circuit

Patent Pending



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specifed in the Electrical Characteristics section is not recommended.

Parameter	Symbol	Maximum	Units
Input Supply Voltage	V_{IN}	-0.3 to 7	V
Logic Inputs/Outputs (EN, VMODE, VDAC, GD)	V_N	-0.3 to V_{IN} +0.3 ,7V Max	V
Output Voltage	V_{OUT}	-0.3 to V_{IN} +0.3 ,7V Max	V
LX Voltage	V_{LX}	-1 to V_{IN} +1, 7V Max	V
Thermal Impedance Junction to Ambient(1)	θ_{JA}	49	°C/W
VOUT Short-Circuit to GND	t_{sc}	Continuous	s
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature	T_S	-60 to +160	°C
Maximum Junction Temperature	T_J	-40 to +150	°C
Peak IR Reflow Temperature	T_{LEAD}	260	°C
ESD Protection Level(2)	V_{ESD}	2	kV

Notes:
1. Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under exposed pad pre JESD51 standards.
2. Tested according JEDEC standard JESD22-A114-B

Electrical Characteristics

Unless otherwise noted: V_{IN} = 4V, EN = V_{IN}, V_{MODE} = GND (High Power), V_{DAC} = 1.1V, T_A = -40 to 85°C. Typical values are at T_A = +25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		2.7		5	V
V_{OUT} Accuracy	V_{OUT}	V_{DAC} = 0.3V, V_{MODE} = V_{IN}, I_{OUT} = 20mA	0.44	0.48	0.52	V
		V_{MODE} = V_{IN}, I_{OUT} = 60mA	3.16	3.40	3.64	
		I_{OUT} = 200mA	1.38	1.62	1.86	
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = 2.7V to 5V, I_{OUT} = 200mA, T_A = -40 to 85°C		±1.2		%
Load Regulation (PWM)	$V_{OUT\ LOAD}$	I_{OUT} = 0A to 800mA, T_A = -40 to 85°C		±0.5		%
Peak Inductor Current	$I_{LX\ PK}$		1		1.7	A
Bypass FET current limit	I_{PASS}		1		2.5	A
Quiescent Current	$I_{Q\ NORM}$			2.5		mA
	$I_{Q\ PASS}$	V_{DAC} = 1.3V		1.5		

Electrical Characteristics (Cont.)

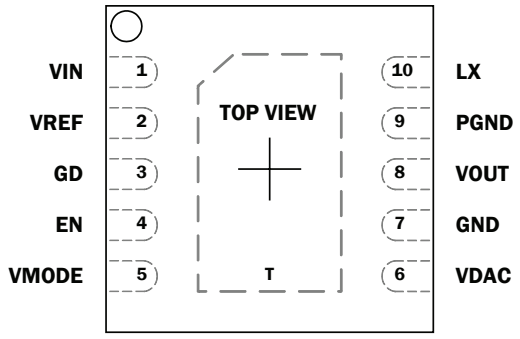
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Shutdown Current	I_{SD}	EN = GND		0.1	3	µA
P-Channel Current Limit	$I_{LIM(P)}$		0.9	1.3	1.7	A
V_{DAC} Pass-through Mode Threshold	$V_{DAC\ PASS}$	V_{DAC} rising	1.24	1.28	1.32	V
		V_{DAC} falling	1.2	1.245		
V_{DAC} Pass-through Mode Hysteresis	$V_{DAC\ HYST}$			40		mV
V_{REF} Output	V_{REF}	I_{REF} = 10mA	2.75	2.85	2.95	V
V_{REF} LDO Dropout	$V_{REF\ DO}$	I_{REF} = 10mA			100	mV
V_{REF} Load Current	I_{REF}				10	mA
V_{REF} Load Regulation	$V_{REF\ LDREG}$	I_{REF} = 0.1mA to 10mA			0.05	%/mA
V_{REF} Line Regulation	$V_{REF\ LNREG}$	I_{REF} = 1 mA			0.3	%/V
GD Load Capacitance	C_{GD}			10		nF
GD Source Current	I_{GDH}	T_A = 25°C		0.5	2	mA
GD Sink Current	I_{GDL}	V_{DAC} = 1.4V, T_A = 25°C		75	150	mA
R_{DSon} of P-Channel FET	R_{PFET}	V_{IN} = 3V, I_{OUT} = 100mA		0.4		Ω
R_{DSon} of N-Channel FET	R_{NFET}	V_{IN} = 3V, I_{OUT} = 100mA		0.25		Ω
R_{DSon} of Bypass P-Channel FET	R_{PASS}	I_{OUT} = 600mA, V_{IN} = 3V, V_{DAC} = 1.4V		0.2		Ω
LX Pin PMOS Leakage	I_{LLXP}	EN=GND, V_{IN} = 3.6V, LX = GND		0.1		µA
VOUT Pin Bypass FET Leakage	I_{LVOUT}	EN=GND, V_{IN} = 3.6V, V_{OUT} = GND		0.1	3	µA
Oscillator Frequency	f_{OSC}	V_{DAC} > 0.95V	0.85	1	1.15	MHz
		V_{DAC} < 0.95V	0.65		1.15	
Logic Input High	V_{IH}	EN / VMODE increasing	1.6			V
Logic Input Low	V_{IL}	EN / VMODE decreasing			0.6	V
Logic Input Current High	I_{IH}	EN / VMODE = 5.0V			±2	µA
Logic Input Current Low	I_{IL}	EN / VMODE = 0V			±2	µA
Enable Transient Over/ Undershoot (1)	OS_{EN}				20	%

Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Enable Transient Settling Time (1)	t_{EN-ST}				40	µs
VDAC Transient Over/Undershoot (1)	OS_{VDAC}				20	%
VDAC Transient Settling Time (1)	$t_{VDAC-ST}$				40	µs
Pass-Through Transition Over/Undershoot (1)	OS_{PASS}				20	%
Pass-Through Transition Settling Time (1)	$t_{PASS-ST}$				40	µs
Thermal Shutdown	T_{SD}			160		°C
Thermal Shutdown Hysteresis	T_{SDH}			15		°C

Notes:
1) Not tested - guaranteed by design.

Pin Configuration



MLPD10: 3X3 10 LEAD

Ordering Information

DEVICE	PACKAGE
SC251MLTRT (1) (2)	MLP 3x3-10
SC251EVB	Evaluation Board

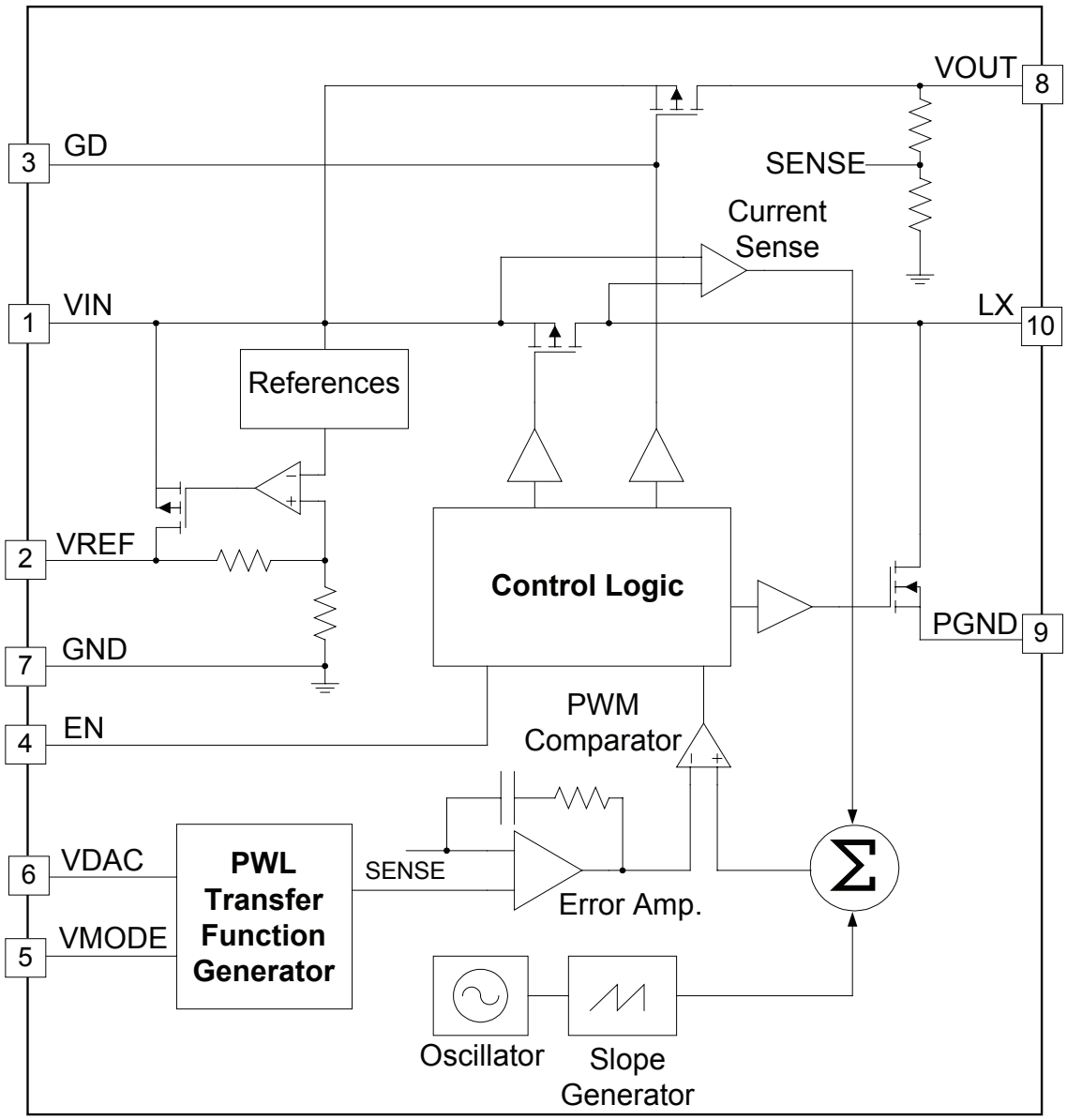
Notes:
1) Lead-free packaging only. This product is fully WEEE and RoHS compliant.
2) Available in tape and reel only. A reel contains 3000 devices.

Marking Information

Top Mark

yy = two-digit year of manufacture
ww = two-digit week of manufacture
xxxx = lot number

Block Diagram



Pin Description

Pin#	Pin Name	Pin Function
1	VIN	Input supply pin.
2	VREF	A 2.85V LDO reference voltage supply - 10mA max load that can be used as a supply for power amplifier bias inputs.
3	GD	A push pull external PFET Gate drive control output - connect to the gate of an external MOSFET to control a low resistance path between V_{IN} and V_{OUT} when low voltage drop is needed (optional - if not used leave floating). A low state turns on the MOSFET.
4	EN	Enable pin - controls both the switching converter and the VREF output. Active high.
5	VMODE	Input control to select the V_{DAC} to V_{OUT} profile (high = low power, low = high power).
6	VDAC	Analog control voltage input - ranges between 0.3 and 1.2V for exponential control of V_{OUT}, V_{DAC} > 1.28 enables pass-through mode (using internal pass MOSFET or optional low R_{DSON} MOSFET controlled by GD).
7	GND	System and logic ground.
8	VOUT	Output voltage pin.
9	PGND	Ground reference for internal N-channel MOSFET.
10	LX	Switch node connection to inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
T	Thermal Pad	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not connected internally.

Applications Information

SC251 Detailed Description

The SC251 is a step-down, fixed frequency pulse-width modulated DC-DC converter designed for use with RF power amplifiers (PAs) in WCDMA handsets and modules.

The output is used to supply DC power to the PA rather than connecting the DC input pin directly to the battery supply. A substantial system power efficiency improvement can be achieved by allowing the system controller to adaptively adjust the DC voltage to the PA, reducing the total power consumption of the device. To maximize efficiency at all RF output gain settings, the PA supply voltage is adjusted exponentially, minimizing PA supply headroom and losses. The benefit of having an exponential V_{OUT} vs. V_{DAC} relationship is clearly seen when plotted on the same graph as linear relationships, see following figure. The SC251 V_{OUT} vs. V_{DAC} transfer function is optimized to provide the lowest supply voltage to maintain the PA's linearity. This provides the best possible balance between Adjacent Channel Leakage Ratio (ACLR) margin and efficiency requirements.

By using a switching regulator, less current is needed than when the PA is connected directly to the battery or an LDO. Reduced current consumption results in more talk-time for the handset.

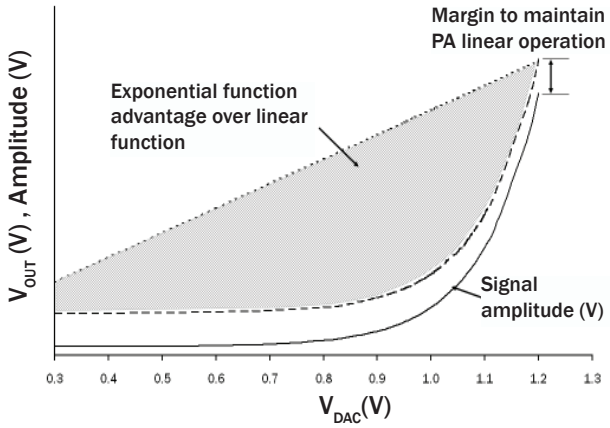


Figure 1 - Advantage of exponential Transfer Function

Operation Modes

The SC251 output voltage is dependent on the V_{DAC} analog control voltage and the V_{MODE} digital control input. In each mode V_{OUT} follows a different V_{DAC} transfer function that is designed to produce maximum power amplifier efficiency. When V_{MODE} is high the device is in low power mode, and when V_{MODE} is low the device switches to high power mode. The relationships between V_{OUT} and V_{DAC} in both modes are optimized to achieve the best efficiency from a dual-mode PA design These relationships are shown in the following figure. The system controller determines the output power level needed from the PA and adjusts the V_{DAC} voltage accordingly. The SC251 monitors the V_{DAC} voltage and adjusts the output voltage supply to the PA to optimize efficiency and maintain PA linearity.

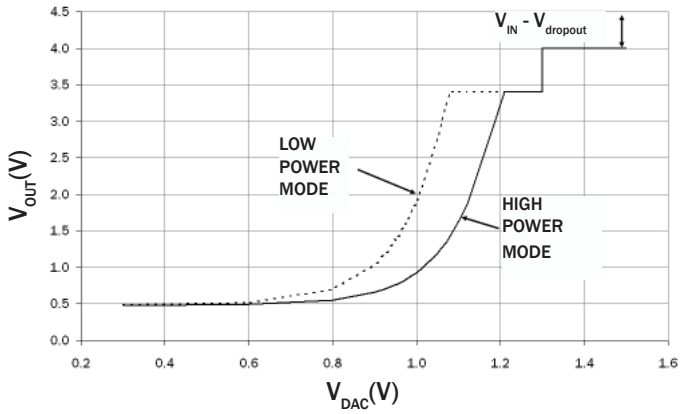


Figure 2 - V_{DAC} to V_{OUT} Transfer Functions

Low Power Mode

The SC251 enters low power mode when the V_{MODE} pin is pulled high. In this mode the V_{DAC} to V_{OUT} transfer function is set to follow the dotted line curve shown in Figure 2. The output voltage starts at 0.5V for low power settings and increases exponentially until it reaches the maximum of 3.4V. If the power control for the PA requires the output voltage to exceed 3.4V, then the SC251 goes into pass-through mode and V_{OUT} is equal to V_{IN} minus the voltage dropped across the pass-through device (see pass-through mode for more details).

A typical WCDMA load profile for low power mode, with the minimum and maximum current limits, is shown in Figure 3.

Applications Information (Cont.)

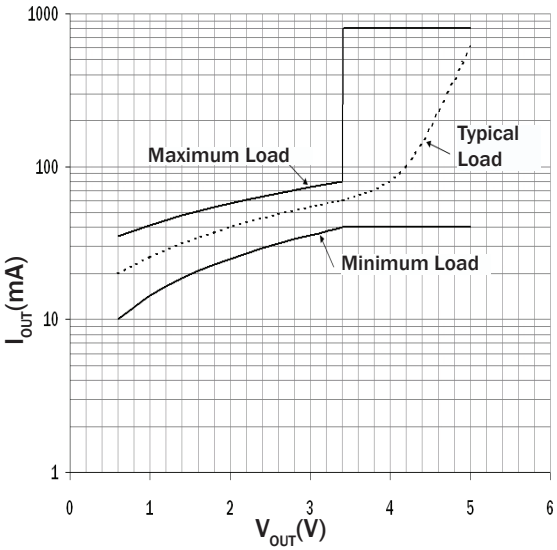


Figure 3 - Load Profile-Low Power Mode

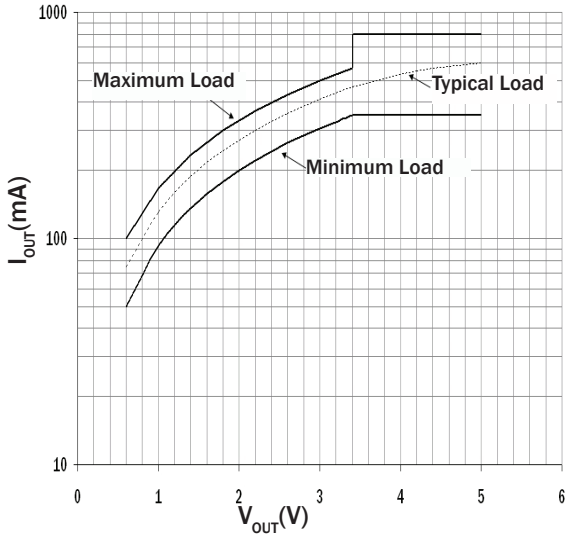


Figure 4 - Load Profile-High Power Mode

High Power Mode

The SC251 enters high power mode when the VMODE pin is pulled low. In this mode the V_{DAC} to V_{OUT} transfer function is set to follow the solid line curve shown in Figure 2. The output voltage again starts at 0.5V and increases exponentially as the power demand increases until it reaches the maximum of 3.4V. A typical WCDMA load profile for high power mode with the minimum and maximum current limits is shown in Figure 4. If the power control for the PA requires the output voltage to exceed 3.4V, then the SC251 goes into pass-through mode and V_{OUT} is equal to V_{IN} minus the voltage dropped across the pass-through device ($V_{dropout}$).

In high power mode the PA gain is constant, but output impedance is lower and the subsequent input voltage required to achieve the desired output power is less than in low power mode. The SC251 output, therefore, switches to the solid line curve in the V_{DAC}-to- V_{OUT} in Figure 2. The lower output voltage required improves efficiency over a single mode system by lowering the voltage required for a fixed current load.

100% Duty Cycle Operation

When the input supply voltage approaches the programmed output voltage the PMOS on-time extends until the supply voltage gets within 400mV of the output voltage. At this point both the internal pass device and the PMOS switching device automatically turns on, connecting V_{IN} to V_{OUT}. The bypass device and PMOS switching device remains fully on until either the V_{IN} voltage is increased by 150mV or the programmed V_{OUT} voltage is reduced such that $V_{IN} - V_{OUT}$ is greater than 650mV. Bypassing the impedance of the inductor and switching PMOS device improves efficiency by minimizing the voltage drop from V_{OUT} to V_{IN}.

Pass-Through Mode

This mode is entered when the V_{DAC} voltage reaches 1.28V. If the demanded output voltage is within 400mV of the input voltage the device automatically enters pass-through as this exceeds the maximum controlled duty cycle of the power converter. In pass-through mode the device enables an internal P-channel MOSFET that bypasses the converter, connecting the output directly to the input. The R_{DSon} of this FET is extremely low so there is little voltage drop across the part. If the system designer determines that the pass-through resistance is too high for the application, there is an optional gate-drive output that can be used with an external switch.

The GD pin becomes active-low only when V_{DAC} is greater than 1.4V. This pin can be connected to the gate of an external low-R_{DSon} P-channel MOSFET whose source and drain are connected to V_{IN} and V_{OUT}, respectively. This option allows the lowest insertion loss possible between V_{IN} and V_{OUT} . Note that GD should not be loaded with a DC current. GD is monitored so that the part remains in pass-through until GD reaches within 600mV of V_{IN}.

Bias Supply Output

In addition to the main output the SC251 also provides a low current LDO reference output that can be used as a

Applications Information (Cont.)

bias supply for power amplifiers. This output provides a regulated 2.85V with output current capability up to 10mA. The 2.85V output is guaranteed for input supply voltages in excess of 2.95V. When input voltages below 2.95V are used, V_{REF} is equal to V_{IN} - $V_{REF\ DO}$. This reference supply is controlled by the same enable pin as the switching regulator.

Protection Features

The SC251 provides the following protection features:

- Thermal shutdown
- Current limit
- Under voltage lockout

Thermal Shutdown

The device has a thermal shutdown feature to protect the device if the junction temperature exceeds 160°C. In thermal shutdown the on-chip power devices are disabled, effectively tri-stating the LX output. Switching will resume when the temperature drops by 15°C.

Short Circuit Protection

The PMOS and NMOS power devices of the buck switcher stage are protected by current limit functions. In the event of a short to ground on the output, the LX pin will switch with minimum duty cycle. The duty cycle is short enough to allow the inductor to discharge during each cycle, thereby preventing the inductor current from "staircasing".

The pass-through PMOS is protected by a current limit function. When the part is enabled in pass-through, the output capacitor charges up with a large surge current. In order to support this surge current and to protect against short circuits, an internal timer is used. A short circuit condition must exist for more than 128 clock cycles before the pass-through device is disabled. After an additional 2048 clock cycles, the pass-through device will turn back on. This cycle will continue until the short circuit is removed. This method allows the part to manage thermal dissipation and recover when the fault condition is removed.

Under Voltage Lockout

The part will turn itself off if the input supply voltage falls below 2.4V typical. The device is allowed to turn on again when the input supply voltage increases above the lockout voltage. Hysteresis is included to prevent chattering.

Inductor Selection

The SC251 is designed for use with a 4.7µH inductor. The magnitude of the inductor current ripple is dependent on the inductor value and can be determined by the following equation:

$$\Delta I_L = \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{L \times f_{osc}}$$

The inductor should have a low DC Resistance (DCR) to minimize the conduction losses and maximize efficiency. As a minimum requirement, the DC current rating of the inductor should be equal to the maximum load current plus half of the inductor current ripple as shown by the following equation:

$$I_{LPK} = I_{OUT(MAX)} + \frac{\Delta I_L}{2}$$

Final inductor selection will depend on various design considerations such as efficiency, EMI, size and cost. Table 1 lists the manufacturers of practical inductor options.

C_{IN} Selection

The source input current to a buck converter is non-continuous. To prevent large input voltage ripple a low ESR ceramic capacitor is required. A minimum value of 10µF should be used for sufficient input voltage filtering and a 22µF should be used for improved input voltage filtering.

C_{OUT} Selection

The internal compensation is designed to work with a certain output filter corner frequency defined by the equation:

$$f_C = \frac{1}{2\pi\sqrt{L \times C_{OUT}}}$$

This single pole filter is designed to operate with an output capacitor value of 4.7µF.

Output voltage ripple is a combination of the voltage ripple from the inductor current charging and discharging the output capacitor and the voltage created from the inductor current ripple through the output capacitor ESR. Selecting an output capacitor with a low ESR reduces the

Applications Information (Cont.)

output voltage ripple component that is dependent upon this ESR, as can be seen in the following equation:

$$\Delta V_{OUT(ESR)} = \Delta I_{L(ripple)} \times ESR_{(COUT)}$$

Capacitors with X7R or X5R ceramic dielectric should be used for their low ESR and superior temperature and voltage characteristics. Y5V capacitors should not be used as their temperature coefficients make them impractical for this application. The following tables lists the manufacturers of recommended capacitor and inductor options.

Table 1: Recommended Inductors

Manufacturer/Part #	Value µH	DCR Ω	Saturation Current A	Tolerance ±%	Dimensions (LxWxH) mm
BI Technologies HM66304R7	4.7	0.072	1.32	20	4.7 × 4.7 × 3.0
Coilcraft D01608C-472ML	4.7	0.09	1.5	20	6.6 × 4.5 × 3.0
TDK VLCF4018T- 4R7N1R0-2	4.7	0.101	1.07	30	4.3 × 4.0 × 1.8

Table 2: Recommended Capacitors

Manufacturer/Part #	Value µF	Rated Voltage VDC	Temperature Characteristic	Case Size
Murata GRM219R 61A475KE34B	4.7	6.3	X5R	0603
TDK C1608JF0J475Z	4.7	6.3	X5R	0603
Murata GRM219R 60J106K E19B	10	6.3	X5R	0603
TDK C2012JB0J106K	10	6.3	X5R	0805

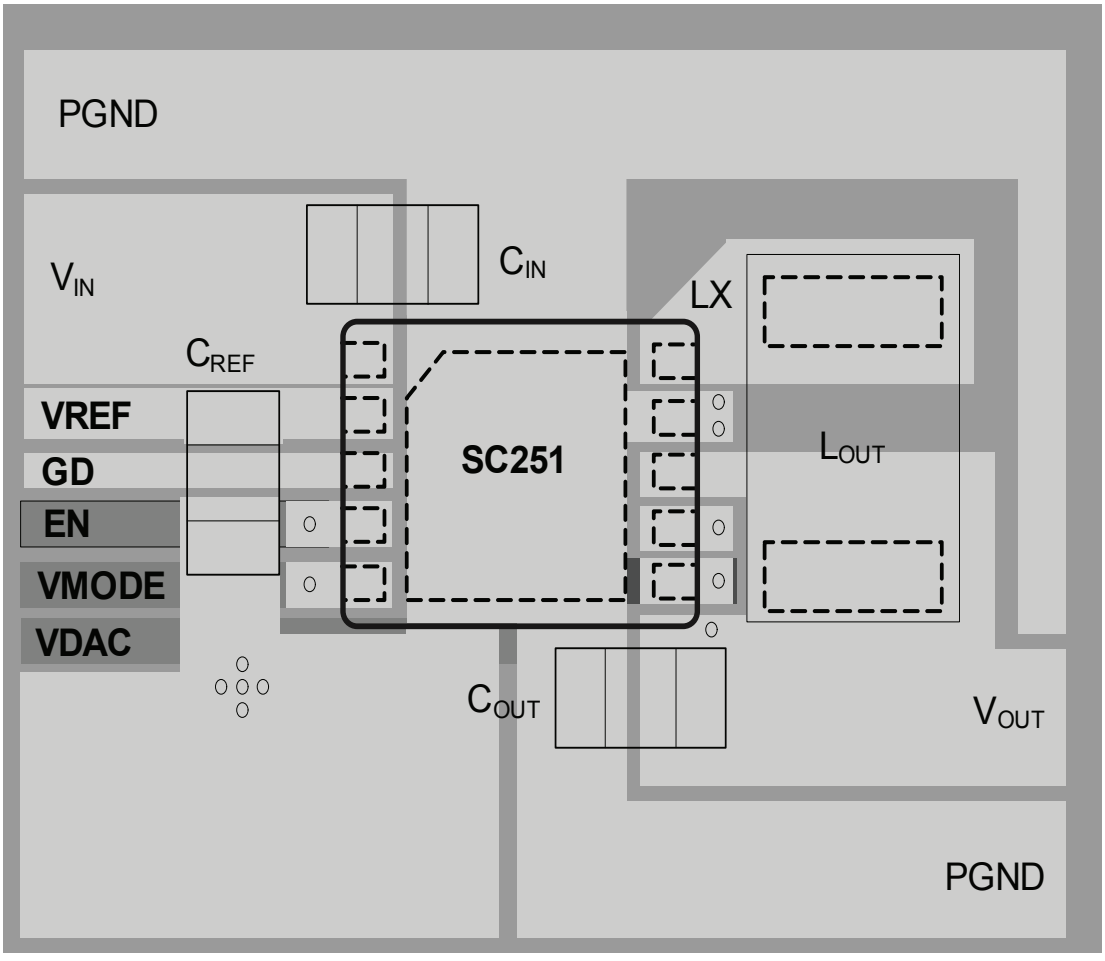
Applications Information (Cont.)

PCB Layout Considerations

Poor layout can degrade the performance of the DC-DC converter and can be a contributory factor in EMI problems, ground bounce and resistive voltage losses. Poor regulation and instability can result.

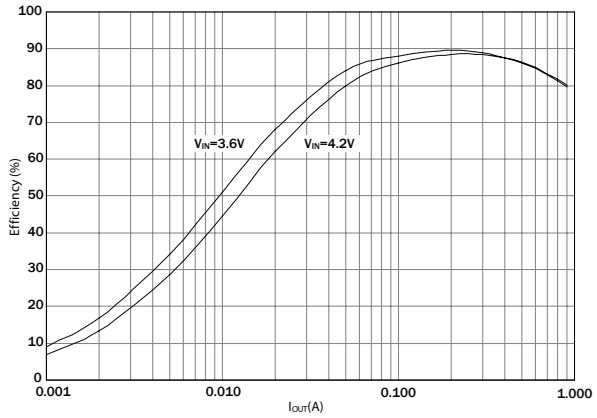
A few simple design rules can be implemented to ensure good layout:

1. Place the inductor and filter capacitors as close to the device as possible and use short wide traces between the power components.
2. Route the output voltage feedback and V_{DAC} path away from the inductor and LX node to minimize noise and magnetic interference.
3. Maximize ground metal on component side to improve the return connection and thermal dissipation. Separation between the LX node and GND should be maintained to avoid coupling of switching noise to the ground plane.
4. To further reduce noise interference on sensitive circuit nodes, use a ground plane with several vias connecting to the component side ground.

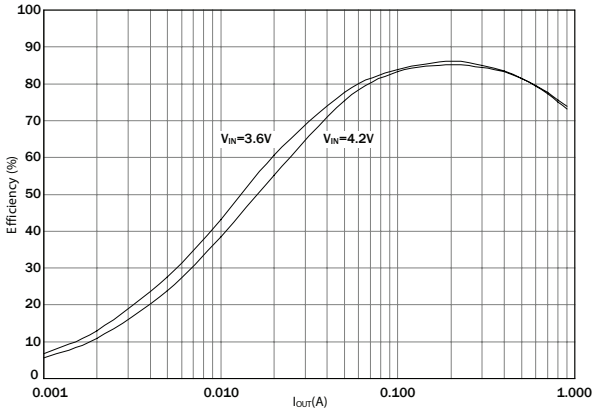


Typical Characteristics

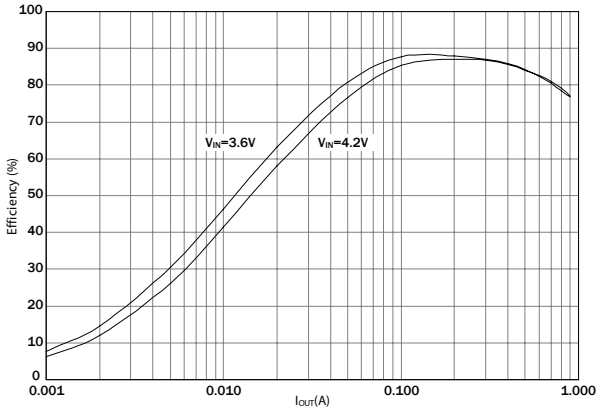
Efficiency vs. Load
V_{OUT}=1.8V



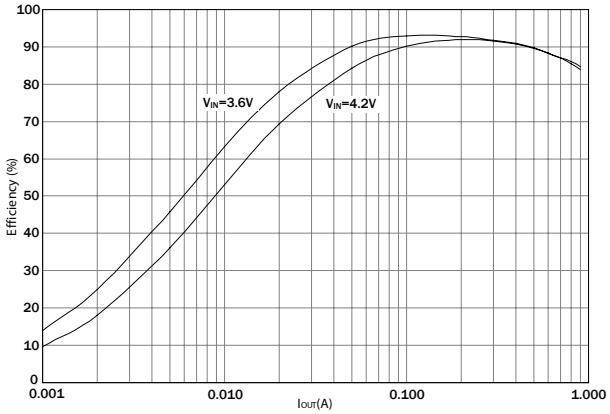
Efficiency vs. Load
V_{OUT}=1.2V



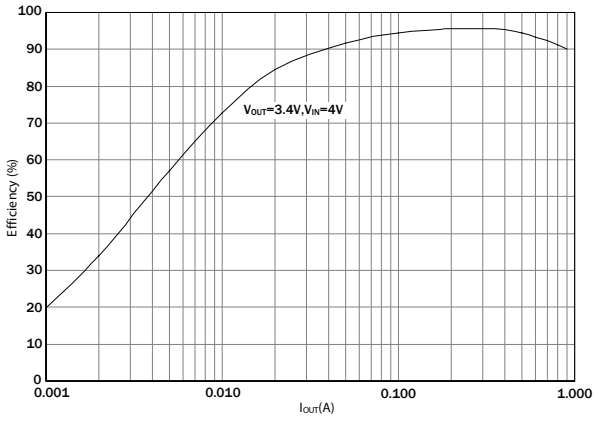
Efficiency vs. Load
V_{OUT}=1.5V



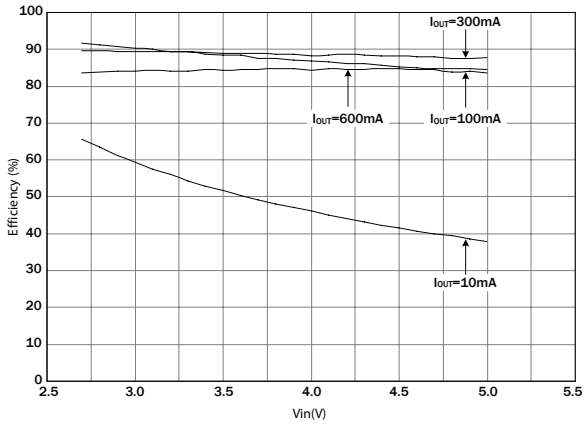
Efficiency vs. Load
V_{OUT}=2.5V



Efficiency vs. Load
V_{OUT}=3.4V (Pass-Through)

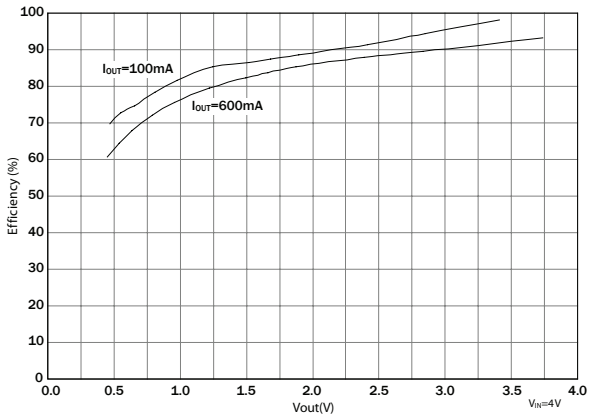


Efficiency vs. V_{IN}
V_{OUT}=1.8V

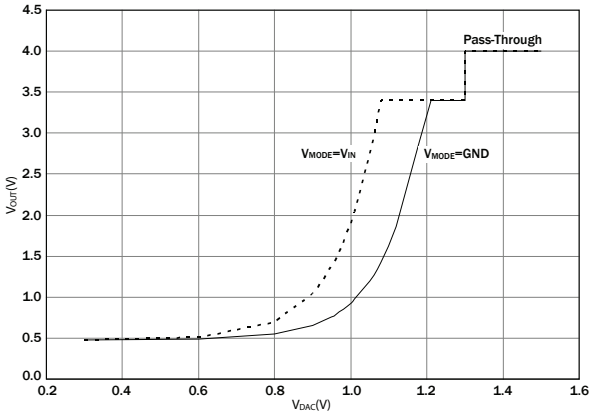


Typical Characteristics (Cont.)

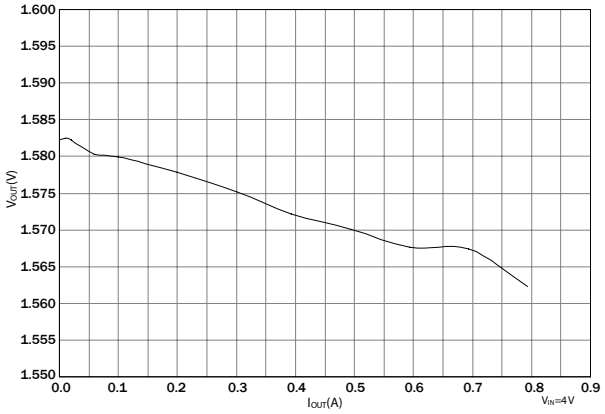
Efficiency vs. V_{OUT}



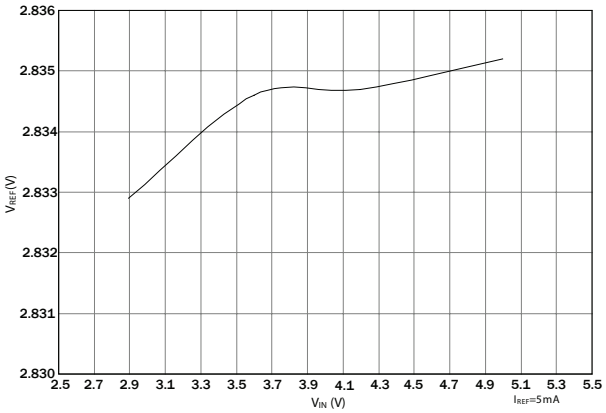
V_{OUT} vs. V_{DAC}



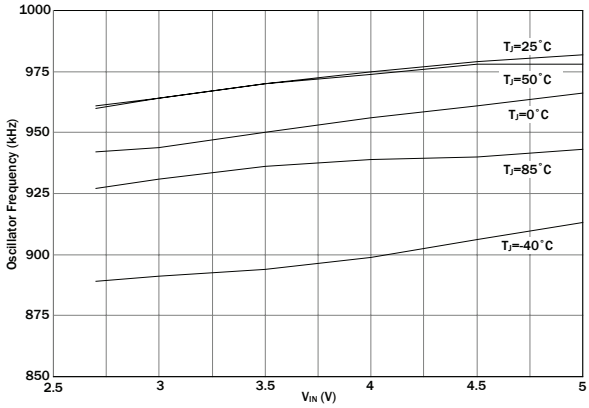
V_{OUT} vs. I_{OUT}



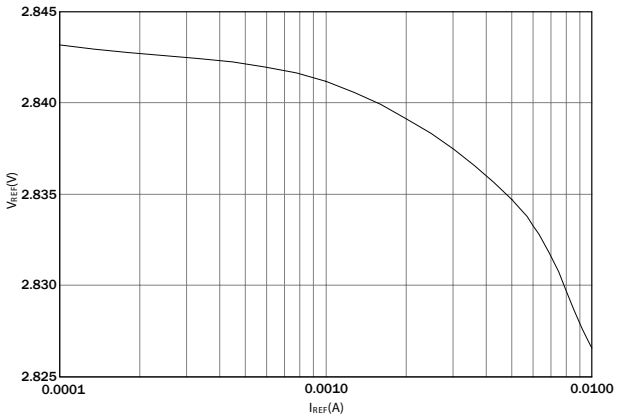
V_{REF} vs. V_{IN}



Oscillator Frequency vs. V_{IN}

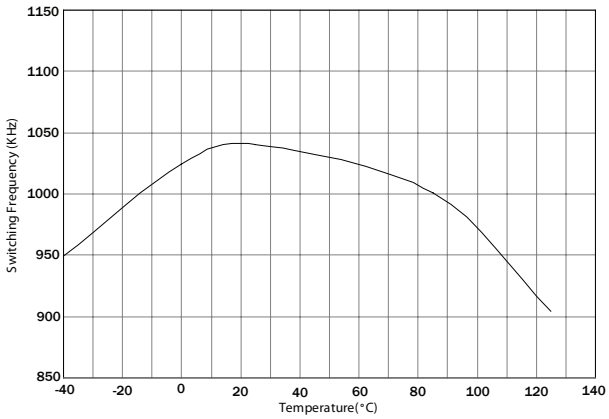


V_{REF} vs. I_{REF}

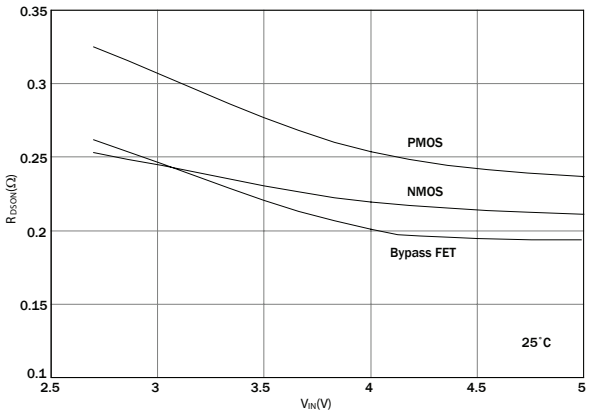


Typical Characteristics (Cont.)

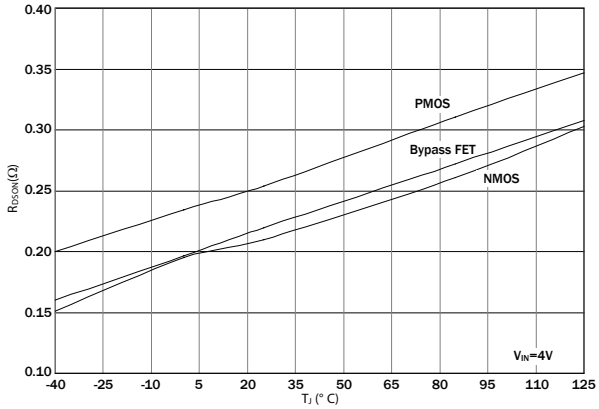
Oscillator Frequency vs. Temperature



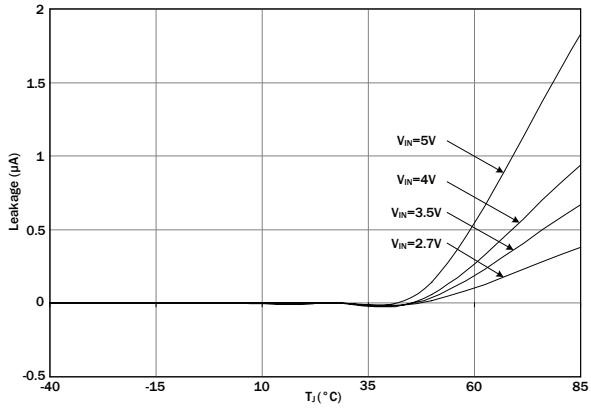
R_{DSON} vs. V_{IN}



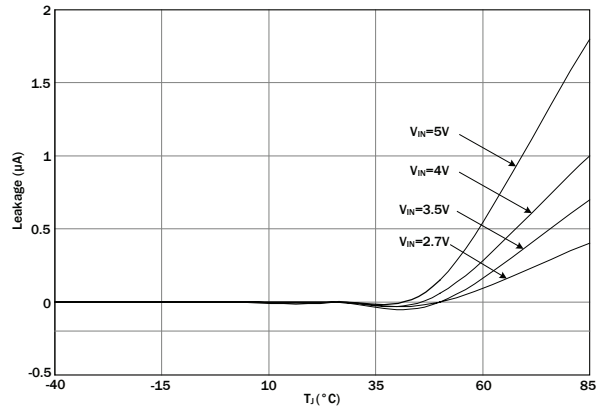
R_{DSON} vs. Temperature



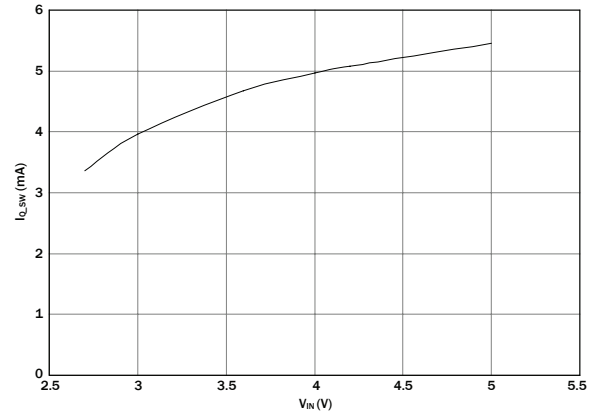
PMOS FET Leakage vs. Temperature



PASS FET Leakage vs. Input Voltage

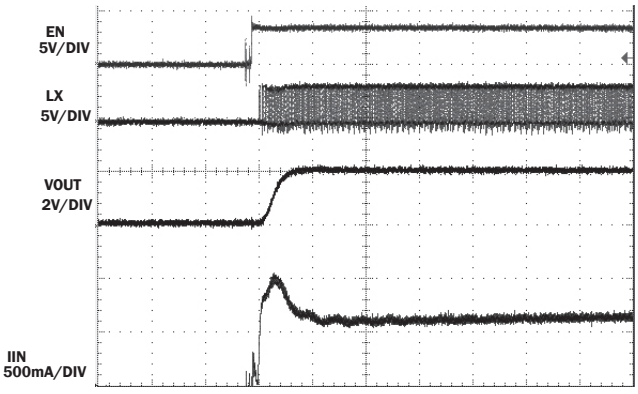


Dynamic Supply Current vs. V_{IN}

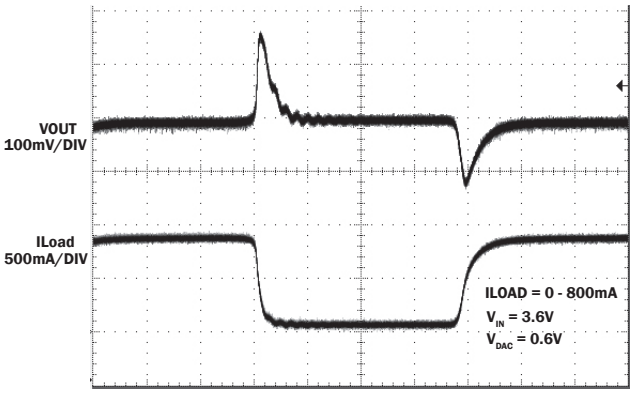


Typical Characteristics (Cont.)

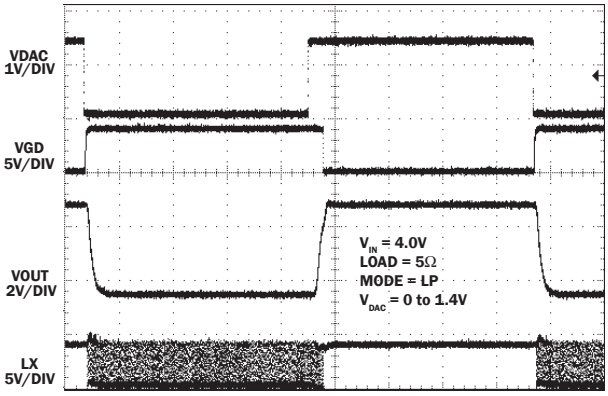
Enable Startup



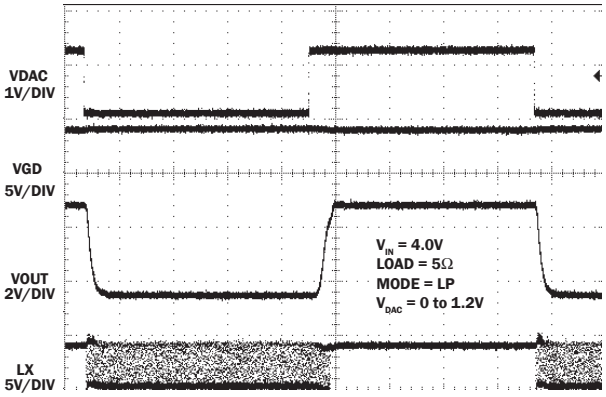
Load Step Response



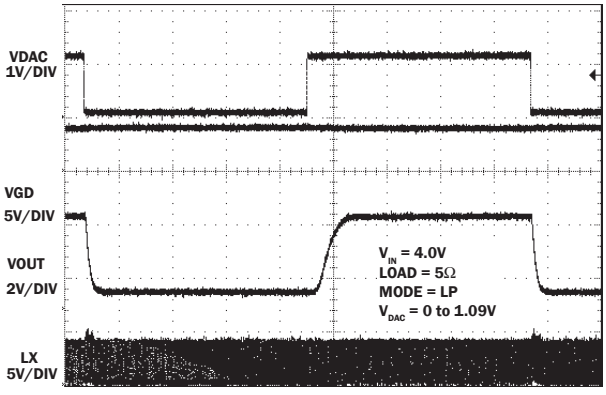
V_{DAC} Step Response (Passthrough)



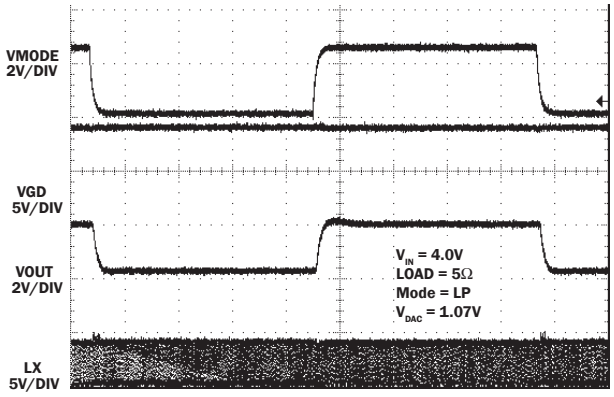
V_{DAC} Step Response (100% duty)



V_{DAC} Step Response

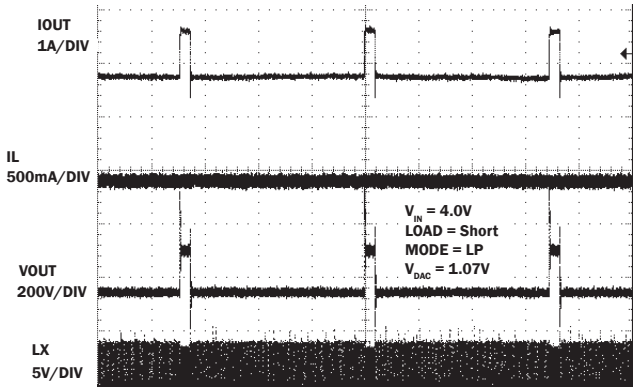


V_{MODE} Step Response



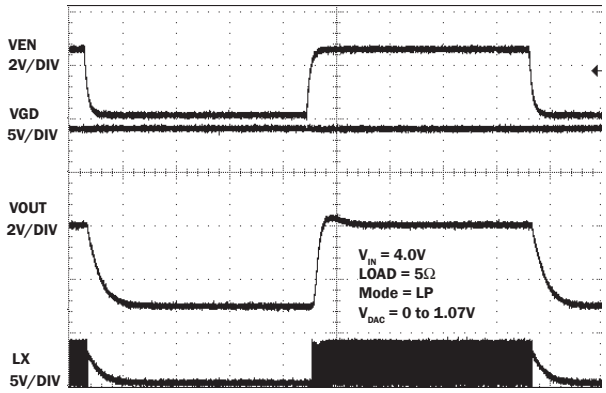
Typical Characteristics (Cont.)

Passthrough Current Limit Operation



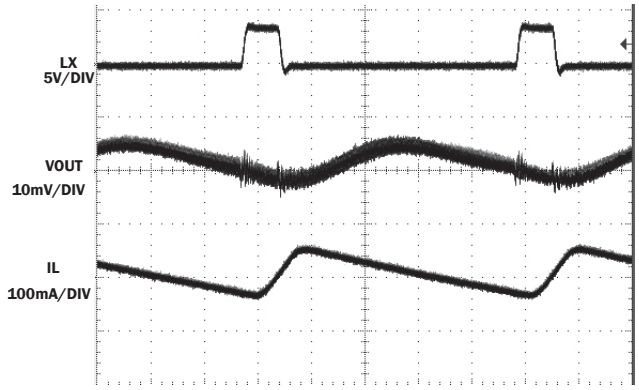
1ms/DIV

Enable Step Response



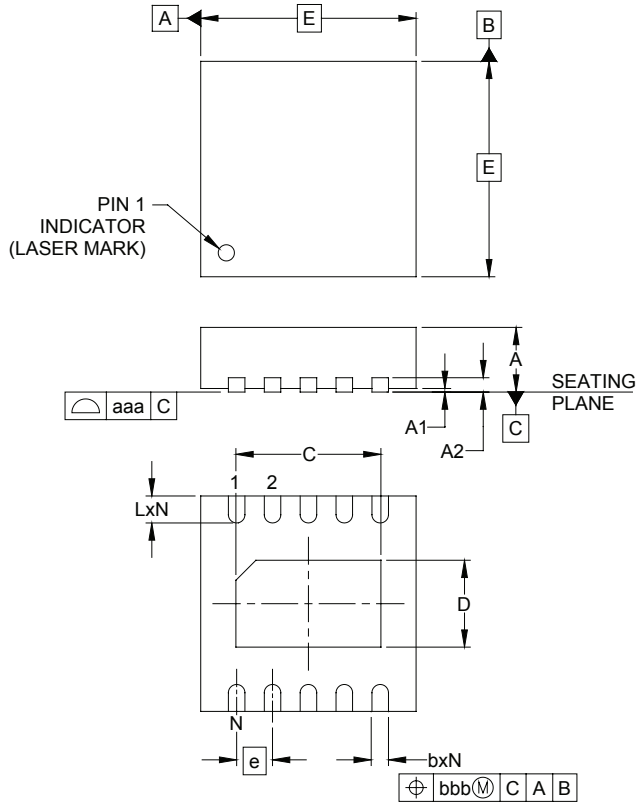
100µs/DIV

Output Ripple Waveform



200ns/DIV

Outline Drawing - MLP-10 3x3

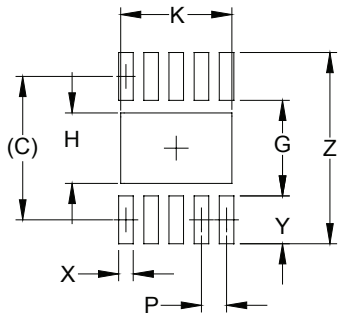


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.009	.011	0.18	0.23	0.30
C	.074	.079	.083	1.87	2.02	2.12
D	.042	.048	.052	1.06	1.21	1.31
E	.114	.118	.122	2.90	3.00	3.10
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	10			10		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS TERMINALS.

Land Pattern - MLP-10 3x3



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.112)	(2.85)
G	.075	1.90
H	.055	1.40
K	.087	2.20
P	.020	0.50
X	.012	0.30
Y	.037	0.95
Z	.150	3.80

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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