FAIRCHILD SEMICONDUCTOR®

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74ACT534
Octal D-Type Flip-Flop with 3-STATE Outputs

Features

- I_{CC} and I_{OZ} reduced by 50%
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- 3-STATE outputs for bus-oriented applications
- Outputs source/sink 24mA
- ACT534 has TTL-compatible inputs
- Inverted output version of ACT374

General Description

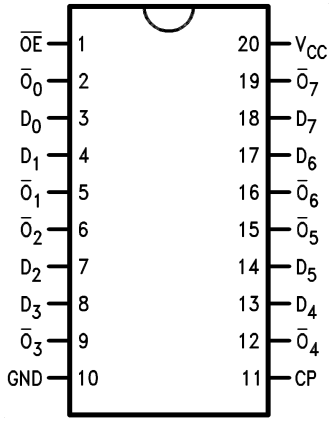
The ACT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The ACT534 is the same as the ACT374 except that the outputs are inverted.

Ordering Information

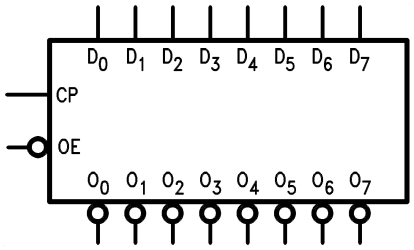
Order Number	Package Number	Package Description
74ACT534SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ACT534SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

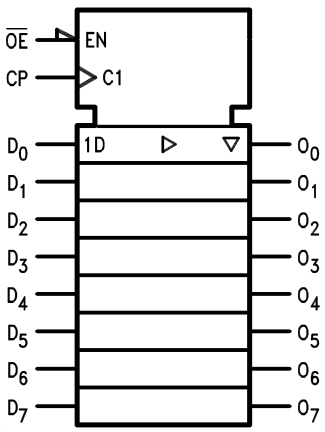
Connection Diagram



Logic Symbols



IEEE/IEC



Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	Complementary 3-STATE Outputs

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Functional Description

The ACT534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Output
CP	**OE**	**D**	$\overline{\mathbf{O}}$
⌐	L	H	L
⌐	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level

L = LOW Voltage Level

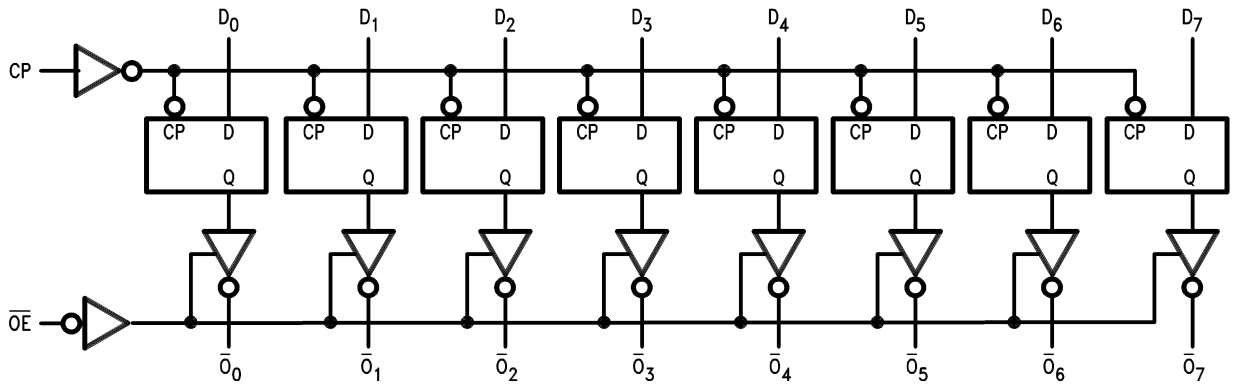
X = Immaterial

⌐ = LOW-to-HIGH Clock Transition

Z = High Impedance

$\overline{O}_0$ = Value stored from previous clock cycle

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 1.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
I_{IK}	DC Input Diode Current	
	$V_I = –0.5V$	–20mA
	$V_I = V_{CC} + 0.5V$	+20mA
V_I	DC Input Voltage	–0.5V to V_{CC} + 0.5V
I_{OK}	DC Output Diode Current	
	$V_O = –0.5V$	–20mA
	$V_O = V_{CC} + 0.5V$	+20mA
V_O	DC Output Voltage	–0.5V to V_{CC} + 0.5V
I_O	DC Output Source or Sink Current	±50mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate:	125mV/ns
	V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C	T_A = –40°C to +85°C		Units
				Typ.	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	2.0	2.0	V
		5.5		1.5	2.0	2.0	
V_{IL}	Maximum LOW Level Input Voltage	4.5	V_{OUT} = 0.1V or V_{CC} – 0.1V	1.5	0.8	0.8	V
		5.5		1.5	0.8	0.8	
V_{OH}	Minimum HIGH Level Output Voltage	4.5	I_{OUT} = –50μA	4.49	4.4	4.4	V
		5.5		5.49	5.4	5.4	
		4.5	V_{IN} = V_{IL} or V_{IH}: I_{OH} = –24mA		3.86	3.76	
		5.5	I_{OH} = –24mA(1)		4.86	4.76	
V_{OL}	Maximum LOW Level Output Voltage	4.5	I_{OUT} = 50μA	0.001	0.1	0.1	V
		5.5		0.001	0.1	0.1	
		4.5	V_{IN} = V_{IL} or V_{IH}: I_{OL} = 24mA		0.36	0.44	
		5.5	I_{OL} = 24mA(1)		0.36	0.44	
I_{IN}	Maximum Input Leakage Current	5.5	V_I = V_{CC}, GND		±0.1	±1.0	μA
I_{OZ}	Maximum 3-STATE Current	5.5	V_I = V_{IL}, V_{IH}; V_O = V_{CC}, GND		±0.25	±2.5	μA
I_{CCT}	Maximum I_{CC}/Input	5.5	V_I = V_{CC} – 2.1V	0.6		1.5	mA
I_{OLD}	Minimum Dynamic Output Current(2)	5.5	V_{OLD} = 1.65V Max.			75	mA
I_{OHD}		5.5	V_{OHD} = 3.85V Min.			–75	mA
I_{CC}	Maximum Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND		4.0	40.0	μA

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)[3]	T_A = +25°C, C_L = 50pF			T_A = –40°C to +85°C, C_L = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
f_{MAX}	Maximum Clock Frequency	5.0		100		120		MHz
t_{PLH}	Propagation Delay, CP to $\overline{Q}_n$	5.0	2.5	6.5	11.5	2.0	12.5	ns
t_{PHL}	Propagation Delay, CP to $\overline{Q}_n$	5.0	2.0	6.0	10.5	2.0	12.0	ns
t_{PZH}	Output Enable Time	5.0	2.5	6.5	12.0	2.0	12.5	ns
t_{PZL}	Output Enable Time	5.0	2.0	6.0	11.0	2.0	11.5	ns
t_{PHZ}	Output Disable Time	5.0	1.5	7.0	12.5	1.0	13.5	ns
t_{PLZ}	Output Disable Time	5.0	1.5	5.5	10.5	1.0	10.5	ns

Note:

3. Voltage range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements

Symbol	Parameter	V_{CC} (V)[4]	T_A = +25°C, C_L = 50pF	T_A = –40°C to +85°C, C_L = 50pF		Units
			Typ.	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW, D_n to CP	5.0	1.0	3.5	4.0	ns
t_H	Hold Time, HIGH or LOW, D_n to CP	5.0	–1.0	1.0	1.5	ns
t_W	CP Pulse Width, HIGH or LOW	5.0	2.0	3.5	3.5	ns

Note:

4. Voltage range 5.0 is 5.0V ± 0.5V.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = OPEN	4.5	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 5.0V	40.0	pF

Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

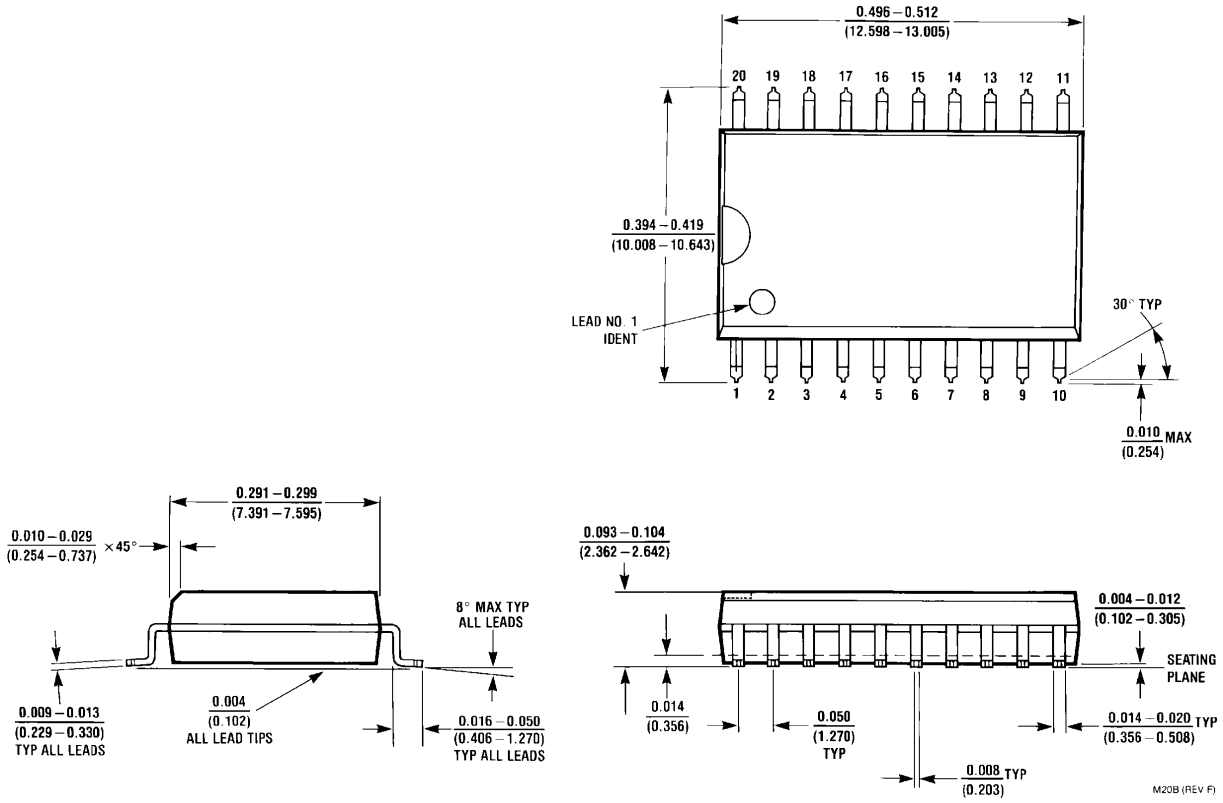
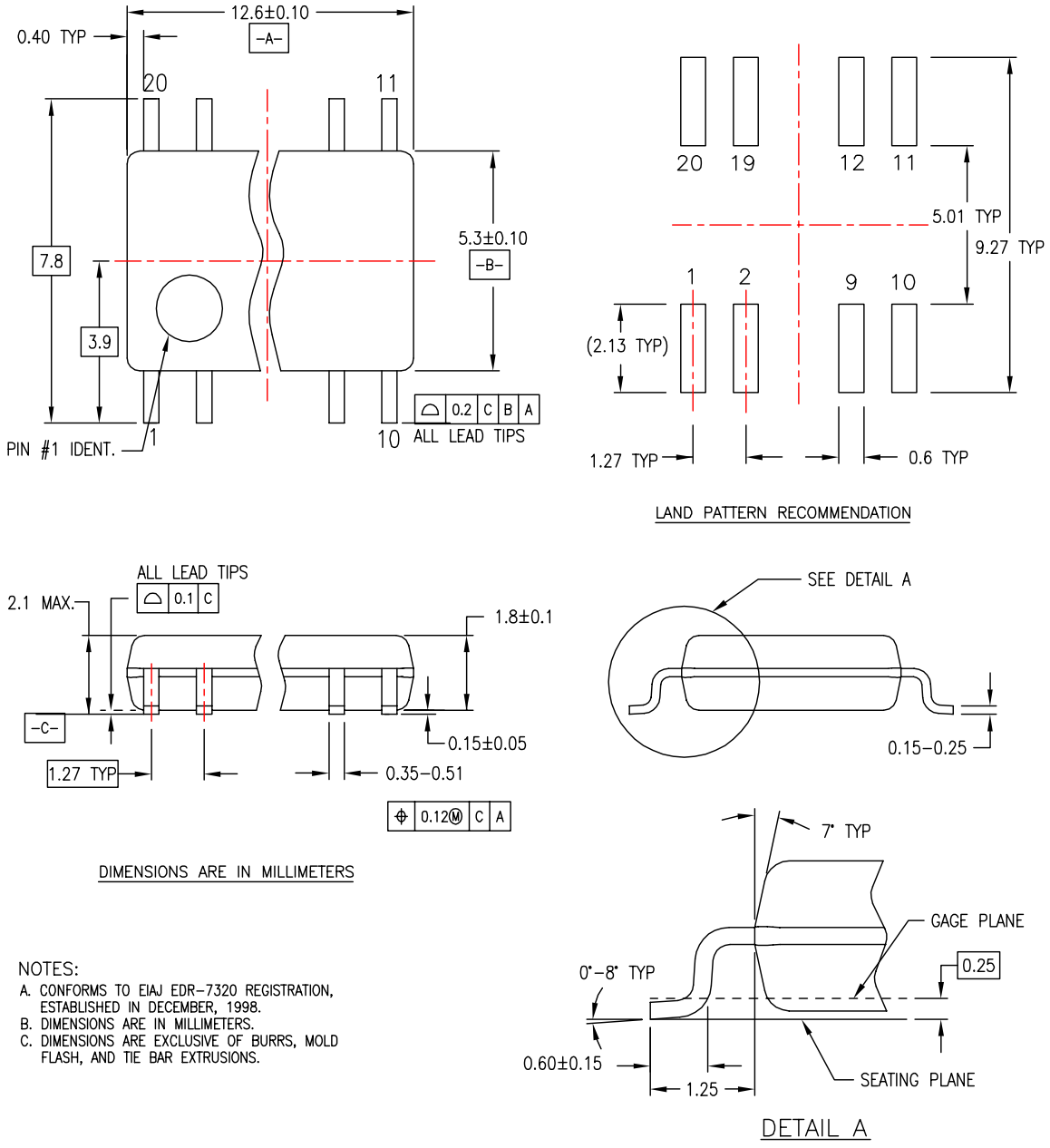


Figure 2. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

Figure 3. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

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