

## Low Charge Injection 16-Channel High Voltage Analog Switch with Bleed Resistors

### Features

- ▶ HVCMOS technology for high performance
- ▶ Integrated bleed resistors on the outputs
- ▶ 16 Channels of high voltage analog switch
- ▶ 3.3V input logic level compatible
- ▶ 20MHz data shift clock frequency
- ▶ Very low quiescent power dissipation-10 $\mu$ A
- ▶ Low parasitic capacitance
- ▶ DC to 10MHz analog signal frequency
- ▶ -60dB typical off-isolation at 5MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ Cascadable serial data register with latches
- ▶ Flexible operating supply voltages

### Applications

- ▶ Medical ultrasound imaging
- ▶ NDT metal flaw detection
- ▶ Piezoelectric transducer drivers
- ▶ Optical MEMS modules

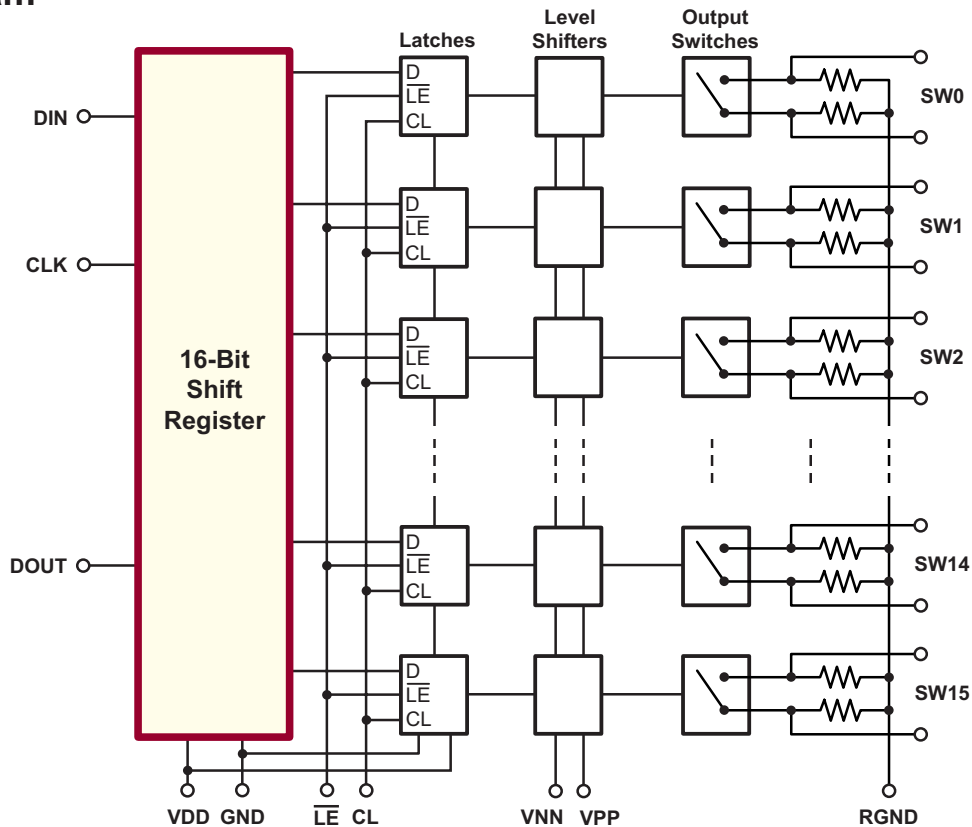
### General Description

The Supertex HV2701 is a low charge injection, 16-channel, high voltage, analog switch integrated circuit (IC) with bleed resistors. The device can be used in applications requiring high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging and piezoelectric transducer drivers. The bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers.

Input data is shifted into a 16-bit shift register that can then be retained in a 16-bit latch. To reduce any possible clock feed-through noise, the latch enable bar should be left high until all bits are clocked in. Data is clocked in during the rising edge of the clock. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g.,  $V_{PP}/V_{NN}$ : +40V/-160V, +100V/-100V, and +160V/-40V.

### Block Diagram



Ordering Information

DEVICE	Package Options
	48-Lead LQFP (FG) <i>(7x7x1.4mm body, 0.50mm pitch)</i>
HV2701	HV2701FG-G

-G indicates package is RoHS compliant ('Green')



Absolute Maximum Ratings

Parameter	Value
V <sub>DD</sub> Logic supply	-0.5V to +7V
V <sub>PP</sub> -V <sub>NN</sub> differential supply	220V
V <sub>PP</sub> Positive supply	-0.5V to V <sub>NN</sub> +200V
V <sub>NN</sub> Negative supply	+0.5V to -200V
Logic input voltage	-0.5V to V <sub>DD</sub> +0.3V
Analog signal range	V <sub>NN</sub> to V <sub>PP</sub>
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to 150°C
Power dissipation	1.0W

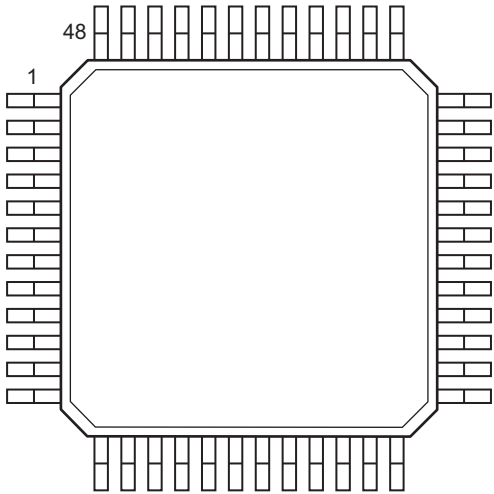
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Recommended Operation Conditions

Symbol	Parameter	Value
V <sub>DD</sub>	Logic power supply voltage	3.0V to 5.5V
V <sub>PP</sub>	Positive high voltage supply	+40V to V <sub>NN</sub> +200V
V <sub>NN</sub>	Negative high voltage supply	-40V to -160V
V <sub>IH</sub>	High level input voltage	0.9V <sub>DD</sub> to V <sub>DD</sub>
V <sub>IL</sub>	Low level input voltage	0V to 0.1V <sub>DD</sub>
V <sub>SIG</sub>	Analog signal voltage peak-to-peak	V <sub>NN</sub> +10V to V <sub>PP</sub> - 0V
T <sub>A</sub>	Operating free air temperature	0°C to 70°C

- Notes:
1. Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
  2. V<sub>SIG</sub> must be within V<sub>NN</sub> and V<sub>PP</sub> or floating during power up/down transition.
  3. Rise and fall times of power supplies V<sub>DD</sub>, V<sub>PP</sub> and V<sub>NN</sub> should not be less than 1.0msec.

Pin Configuration



48-Lead LQFP Package (FG)  
*(top view)*

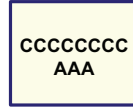
Product Marking

Top Marking



- YY = Year Sealed
- WW = Week Sealed
- L = Lot Number
- C = Country of Origin\*
- A = Assembler ID\*

Bottom Marking



- = "Green" Packaging
- \*May be part of top marking

48-Lead LQFP Package (FG)

## DC Electrical Characteristics

(over recommended operating conditions unless otherwise noted)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R <sub>ONS</sub>	Small signal switch on-resistance	-	30	-	26	38	-	48	Ω	I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +40V V <sub>NN</sub> = -160V
		-	25	-	22	27	-	32		I <sub>SIG</sub> = 200mA	
		-	25	-	22	27	-	30		I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +100V V <sub>NN</sub> = -100V
		-	18	-	18	24	-	27		I <sub>SIG</sub> = 200mA	
		-	23	-	20	25	-	30		I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +160V V <sub>NN</sub> = -40V
		-	22	-	16	25	-	27		I <sub>SIG</sub> = 200mA	
ΔR <sub>ONS</sub>	Small signal switch on-resistance matching	-	20	-	5.0	20	-	20	%	I <sub>SIG</sub> = 5.0mA, V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V	
R <sub>ONL</sub>	Large signal switch on-resistance	-	-	-	15	-	-	-	Ω	V <sub>SIG</sub> = V <sub>PP</sub> -10V, I <sub>SIG</sub> = 1.0A	
R <sub>INT</sub>	Value of output bleed resistor	-	-	20	35	50	-	-	KΩ	Output Switch to RGND I <sub>RINT</sub> = 0.5mA	
I <sub>SOL</sub>	Switch off leakage per switch*	-	5.0	-	1.0	10	-	15	μA	V <sub>SIG</sub> = V <sub>PP</sub> -10V and V <sub>NN</sub> +10V	
V <sub>OS</sub>	DC offset switch off*	-	300	-	100	300	-	300	mV	No Load	
	DC offset switch on*	-	500	-	100	500	-	500	mV		
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current	-	-	-	10	50	-	-	μA	All switches off	
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current	-	-	-	-10	-50	-	-	μA	All switches off	
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current	-	-	-	10	50	-	-	μA	All switches on, I <sub>SW</sub> = 5.0mA	
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current	-	-	-	-10	-50	-	-	μA	All switches on, I <sub>SW</sub> = 5.0mA	
I <sub>SW</sub>	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V <sub>SIG</sub> duty cycle < 0.1%	
f <sub>SW</sub>	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I <sub>PP</sub>	Average V <sub>PP</sub> supply current	-	6.5	-	-	7.0	-	8.0	mA	V <sub>PP</sub> = +40V V <sub>NN</sub> = -160V	All output switches are turning On and Off at 50KHz with no load.
		-	4.0	-	-	5.5	-	5.5		V <sub>PP</sub> = +100V V <sub>NN</sub> = -100V	
		-	4.0	-	-	5.0	-	5.5		V <sub>PP</sub> = +160V V <sub>NN</sub> = -40V	
I <sub>NN</sub>	Average V <sub>NN</sub> supply current	-	6.5	-	-	7.0	-	8.0	mA	V <sub>PP</sub> = +40V V <sub>NN</sub> = -160V	
		-	4.0	-	-	5.0	-	5.5		V <sub>PP</sub> = +100V V <sub>NN</sub> = -100V	
		-	4.0	-	-	5.0	-	5.5		V <sub>PP</sub> = +160V V <sub>NN</sub> = -40V	
I <sub>DD</sub>	Average V <sub>DD</sub> supply current	-	4.0	-	-	4.0	-	4.0	mA	f <sub>CLK</sub> = 5.0MHz, V <sub>DD</sub> = 5.0V	
I <sub>DDQ</sub>	Quiescent V <sub>DD</sub> supply current	-	10	-	-	10	-	10	μA	All logic inputs are static	
I <sub>SOR</sub>	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V <sub>OUT</sub> = V <sub>DD</sub> -0.7V	
I <sub>SINK</sub>	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V <sub>OUT</sub> = 0.7V	
C <sub>IN</sub>	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

\* See Test Circuits on page 5

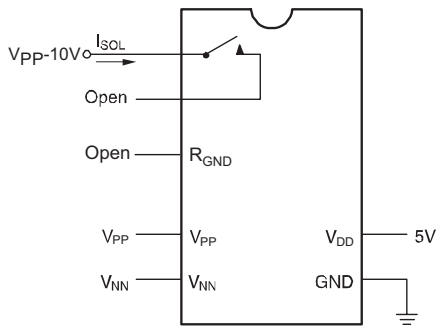
**AC Electrical Characteristics**

(over recommended operating conditions,  $V_{DD} = 5.0V$ ,  $t_R = t_F \leq 5.0ns$ , 50% duty cycle,  $C_{LOAD} = 20pF$ , unless otherwise noted)

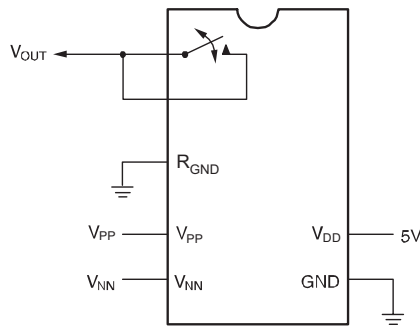
Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
$t_{SD}$	Set up time before $\overline{LE}$ rises	25	-	25	-	-	25	-	ns	---
$t_{WLE}$	Time width of $\overline{LE}$	56	-	-	56	-	56	-	ns	$V_{DD} = 3.0V$
		12	-	-	12	-	12	-		$V_{DD} = 5.0V$
$t_{DO}$	Clock delay time to data out	50	100	50	78	100	50	100	ns	$V_{DD} = 3.0V$
		15	40	15	30	40	15	40		$V_{DD} = 5.0V$
$t_{WCL}$	Time width of CL	55	-	55	-	-	55	-	ns	---
$t_{SU}$	Set up time data to clock	21	-	-	21	-	21	-	ns	$V_{DD} = 3.0V$
		7	-	-	7	-	7	-		$V_{DD} = 5.0V$
$t_H$	Hold time data from clock	2	-	2	-	-	2	-	ns	$V_{DD} = 3.0$ or $5.0V$
$f_{CLK}$	Clock frequency	-	8	-	-	8	-	8	MHz	$V_{DD} = 3.0V$
		-	20	-	-	20	-	20		$V_{DD} = 5.0V$
$t_R, t_F$	Clock rise and fall times	-	50	-	-	50	-	50	ns	----
$T_{ON}$	Turn ON time*	-	5.0	-	-	5.0	-	5.0	$\mu s$	$V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10K\Omega$
$T_{OFF}$	Turn OFF time*	-	5.0	-	-	5.0	-	5.0	$\mu s$	$V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10K\Omega$
dv/dt	Maximum $V_{SIG}$ slew rate	-	20	-	-	20	-	20	v/ns	$V_{PP} = +40V, V_{NN} = -160V$
		-	20	-	-	20	-	20		$V_{PP} = +100V, V_{NN} = -100V$
		-	20	-	-	20	-	20		$V_{PP} = +160V, V_{NN} = -40V$
$K_O$	Off isolation*	-30	-	-30	-33	-	-30	-	dB	$f = 5.0MHz, 1K\Omega/15pF$ load
		-58	-	-58	-	-	-58	-		$f = 5.0MHz, 50\Omega$ load
$K_{CR}$	Switch crosstalk*	-60	-	-60	-70	-	-60	-	dB	$f = 5.0MHz, 50\Omega$ load
$I_{ID}$	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, $f = 1.0MHz$
$C_{SG(ON)}$	On capacitance SW to GND	25	50	25	38	50	25	50	pF	0V, $f = 1.0MHz$
$+V_{SPK}$	Output voltage spike*	-	-	-	-	150	-	-	mV	$V_{PP} = +40V, V_{NN} = -160V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	150	-	-		$V_{PP} = +100V, V_{NN} = -100V, R_{LOAD} = 50\Omega$
$+V_{SPK}$		-	-	-	-	150	-	-		$V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	150	-	-		$V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50\Omega$
$+V_{SPK}$		-	-	-	-	150	-	-		$V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	150	-	-		$V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50\Omega$
QC	Charge injection*	-	-	-	820	-	-	-	pC	$V_{PP} = +40V, V_{NN} = -160V, V_{SIG} = 0V$
		-	-	-	600	-	-	-		$V_{PP} = +100V, V_{NN} = -100V, V_{SIG} = 0V$
		-	-	-	350	-	-	-		$V_{PP} = +160V, V_{NN} = -40V, V_{SIG} = 0V$

\* See Test Circuits on page 5

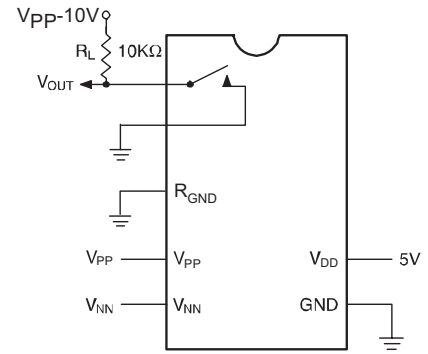
HV2701 Test Circuits



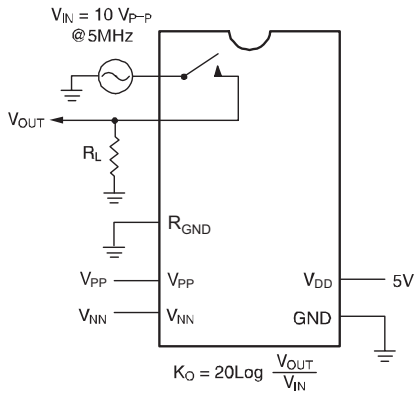
Switch Off Leakage per Switch



DC Offset Switch ON/OFF

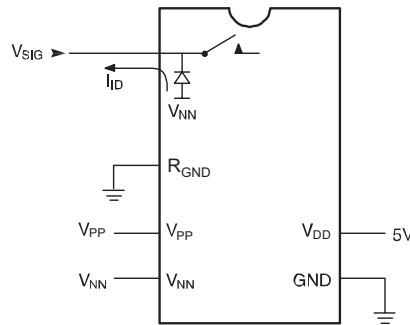


TURN (TON/TOFF) ON/OFF TIME

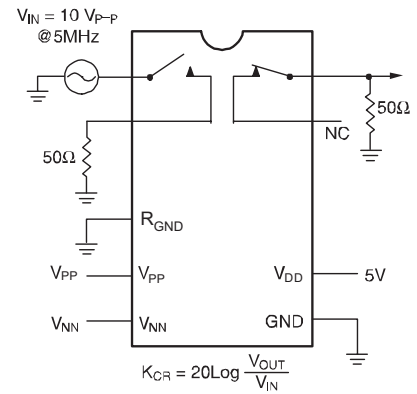


OFF Isolation

$$K_O = 20 \text{Log} \frac{V_{OUT}}{V_{IN}}$$

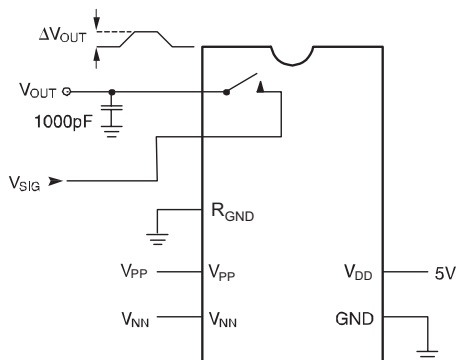


Output Switch Isolation Diode Current

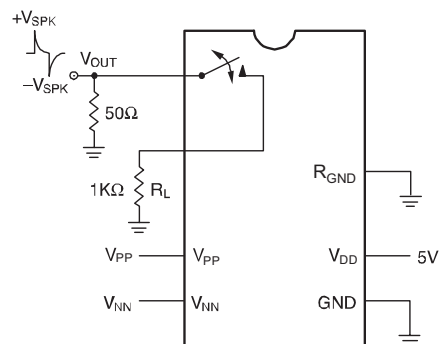


Switch Crosstalk

$$K_{CR} = 20 \text{Log} \frac{V_{OUT}}{V_{IN}}$$



Charge Injection  
 $Q = 1000\text{pF} \times \Delta V_{OUT}$



Output Voltage Spike

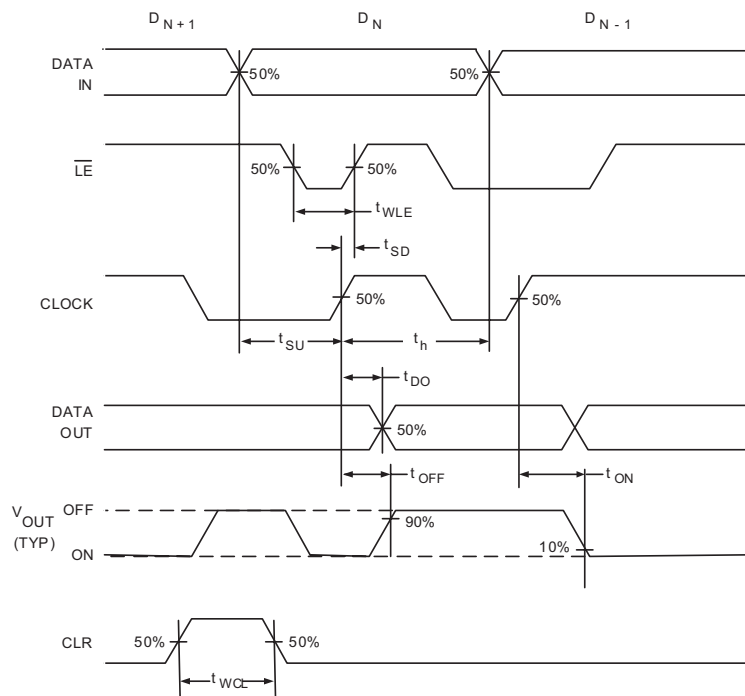
Logic Function Table

D0	D1	...	D7	D8	...	D15	$\overline{LE}$	CL	SW0	SW1	...	SW7	SW8	...	SW15
L	-		-	-		-	L	L	OFF	-		-	-		-
H	-		-	-		-	L	L	ON	-		-	-		-
-	L		-	-		-	L	L	-	OFF		-	-		-
-	H		-	-		-	L	L	-	ON		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		L	-		-	L	L	-	-		OFF	-		-
-	-		H	-		-	L	L	-	-		ON	-		-
-	-	...	-	L	...	-	L	L	-	-	...	-	OFF	...	-
-	-		-	H		-	L	L	-	-		-	ON		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		L	L	L	-	-		-	-		OFF
-	-		-	-		H	L	L	-	-		-	-		ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE					
X	X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF					

Notes:

1. The 16 switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. All 16 switches go to a state retaining their latched condition at the rising edge of  $\overline{LE}$ . When  $\overline{LE}$  is low the shift registers data flow through the latch.
4.  $D_{OUT}$  is high when data in the shift register 15 is high.
5. Shift registers clocking has no effect on the switch states if  $\overline{LE}$  is high.
6. The CL clear input overrides all other inputs.

Logic Timing Waveforms



**Pin Configuration  
48-Lead LQFP (FG)**

Pin #	Function
1	NC
2	NC
3	SW4B
4	SW4A
5	SW3B
6	SW3A
7	SW2B
8	SW2A
9	SW1B
10	SW1A
11	SW0B
12	SW0A

Pin #	Function
13	VNN
14	NC
15	VPP
16	NC
17	GND
18	VDD
19	DIN
20	CLK
21	$\overline{LE}$
22	CLR
23	DOUT
24	RGND

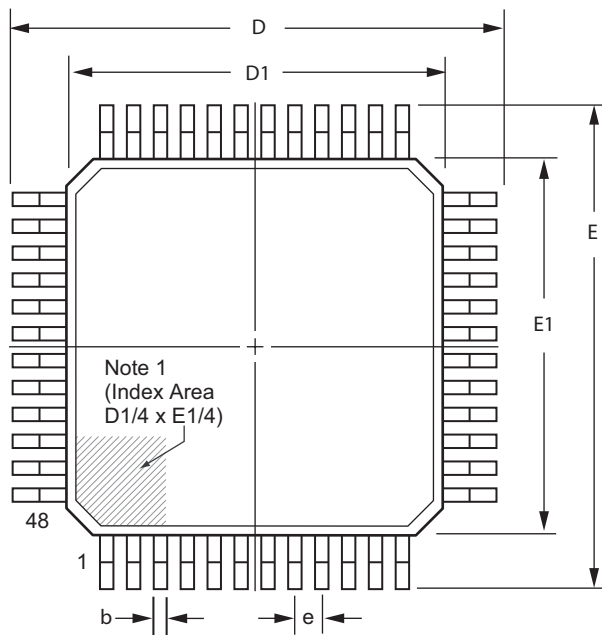
Pin #	Function
25	SW15B
26	SW15A
27	SW14B
28	SW14A
29	SW13B
30	SW13A
31	SW12B
32	SW12A
33	SW11B
34	SW11A
35	NC
36	NC

Pin #	Function
37	SW10B
38	SW10A
39	SW9B
40	SW9A
41	SW8B
42	SW8A
43	SW7B
44	SW7A
45	SW6B
46	SW6A
47	SW5B
48	SW5A

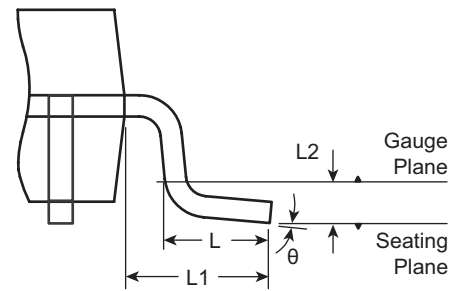
NC = No Internal Connection

# 48-Lead LQFP Package Outline (FG)

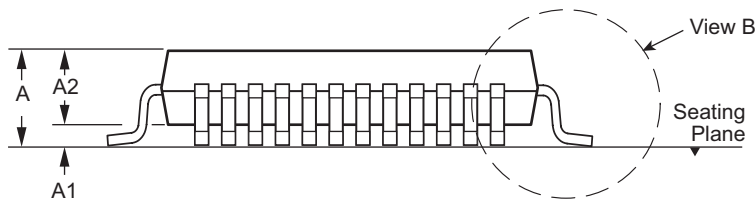
7x7mm body, 1.4mm height (min), 0.50mm pitch



**Top View**



**View B**



**Side View**

**Note 1:**

A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol	A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	$\theta$
Dimension (mm)	MIN	1.40	0.05	1.35	0.17	8.80	6.80	8.80	6.80	0.50 BSC	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00				3.5°
	MAX	1.60	0.15	1.45	0.27	9.20	7.20	9.20	7.20				7°

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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