TOSHIBA Power MOS FET Module Silicon P Channel MOS Type (Four L^2-π-MOSV in One)

MP4208

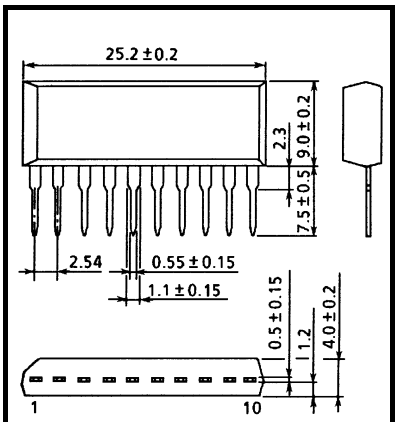
Industrial Applications

High Power High Speed Switching Applications

Hammer Drive, Pulse Motor Drive and Inductive Load Switching

- −4 V gate drive available
- Small package by full molding (SIP 10 pin)
- High drain power dissipation (4-device operation)
  : P_T = 4 W (Ta = 25°C)
- Low drain-source ON resistance: $R_{DS\ (ON)}$ = 0.2 Ω (typ.)
- Low leakage current: I_{GSS} = ±10 μA (max) (V_{GS} = ±16 V)
  I_{DSS} = −100 μA (max) (V_{DS} = −60 V)
- Enhancement-mode: V_{th} = −0.8 to −2.0 V (I_D = −1 mA)

Unit: mm



1, 10	SOURCE
2, 4, 6, 8	GATE
3, 5, 7, 9	DRAIN

JEDEC	—
JEITA	—
TOSHIBA	2-25A1D

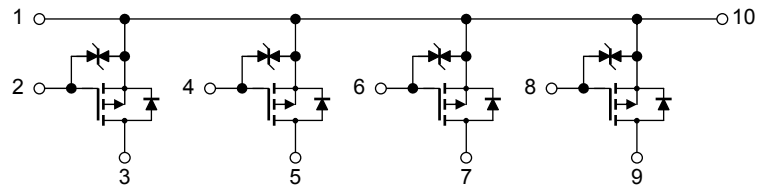
Weight: 2.1 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

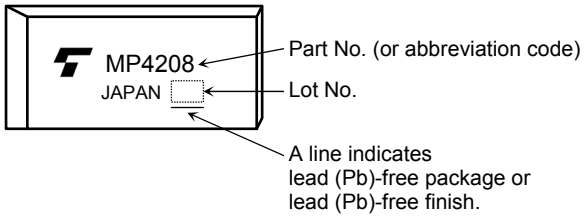
Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	−60	V
Gate-source voltage	V_{GSS}	±20	V
Drain current	I_D	−5	A
Peak drain current	I_{DP}	−10	A
Drain power dissipation (1-device operation, Ta = 25°C)	P_D	2.0	W
Drain power dissipation (4-device operation, Ta = 25°C)	P_{DT}	4.0	W
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Array Configuration



Marking

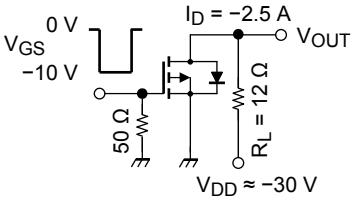


Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance from channel to ambient (4-device operation, Ta = 25°C)	$\Sigma R_{th\ (ch\text{-}a)}$	31.3	°C/W
Maximum lead temperature for soldering purposes (3.2 mm from case for 10 s)	T_L	260	°C

This transistor is an electrostatic-sensitive device. Please handle withccaution.

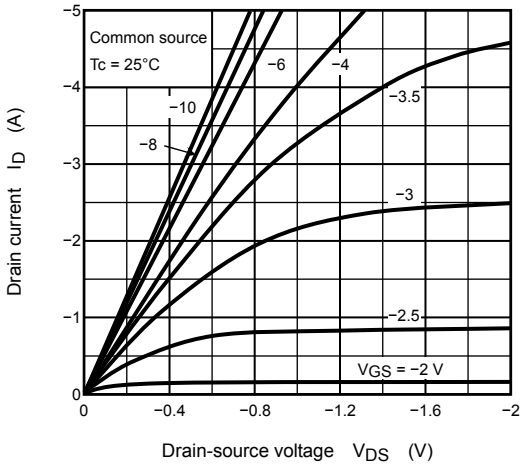
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-off current		I_{DSS}	V_{DS} = −60 V, V_{GS} = 0 V	—	—	−100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−60	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −1 mA	−0.8	—	−2.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −2.5 A	1	3	—	S
Drain-source ON resistance		$R_{DS\ (ON)}$	I_D = −2.5 A, V_{GS} = −4 V	—	0.3	0.5	Ω
		$R_{DS\ (ON)}$	I_D = −2.5 A, V_{GS} = −10 V	—	0.2	0.3	
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	630	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	95	—	pF
Output capacitance		C_{oss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	290	—	pF
Switching time	Rise time	t_r		—	25	—	ns
	Turn-on time	t_{on}		—	45	—	
	Fall time	t_f		—	55	—	
	Turn-off time	t_{off}	V_{IN}: t_r, t_f < 5 ns, duty ≤ 1%, t_w = 10 μs	—	200	—	
Total gate charge (gate-source plus gate-drain)		Q_g	I_D = −5 A, V_{GS} = −10 V, V_{DD} ≈ 48 V	—	22	—	nC
Gate-source charge		Q_{gs}		—	16	—	nC
Gate-drain (“miller”) charge		Q_{gd}		—	6	—	nC

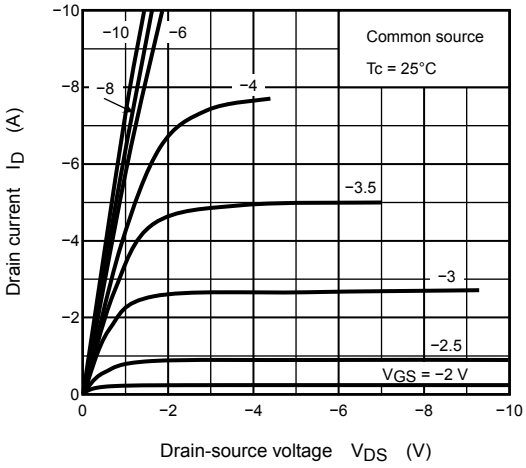
Source-Drain Diode Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	I_{DR}	—	—	—	−5	A
Peak drain reverse current	I_{DRP}	—	—	—	−10	A
Diode forward voltage	V_{DSF}	I_{DR} = −5 A, V_{GS} = 0 V	—	1.0	2.0	V
Reverse recovery time	t_{rr}	I_{DR} = −5 A, V_{GS} = 0 V	—	80	—	ns
Reverse recovery charge	Q_{rr}	dI_{DR}/dt = −50 A/μs	—	0.1	—	μC

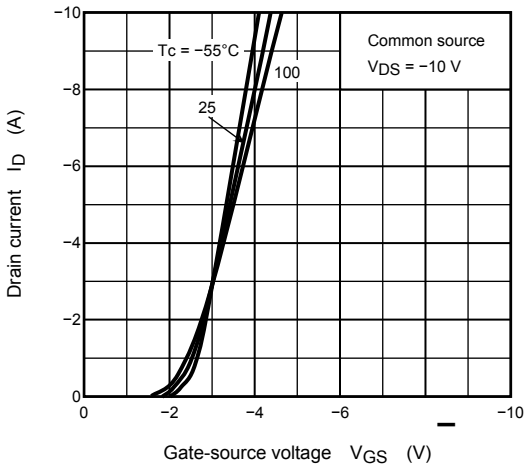
$I_D - V_{DS}$



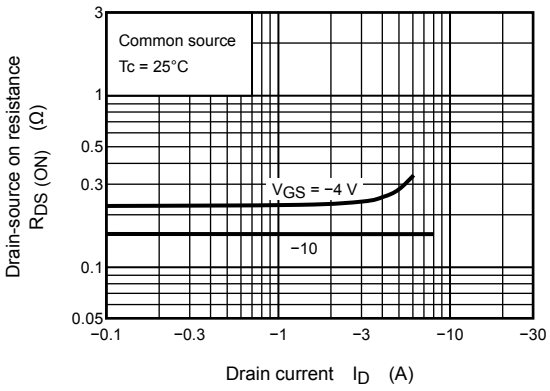
$I_D - V_{DS}$



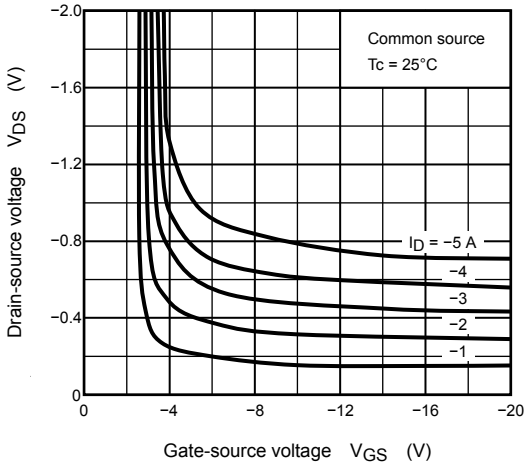
$I_D - V_{GS}$



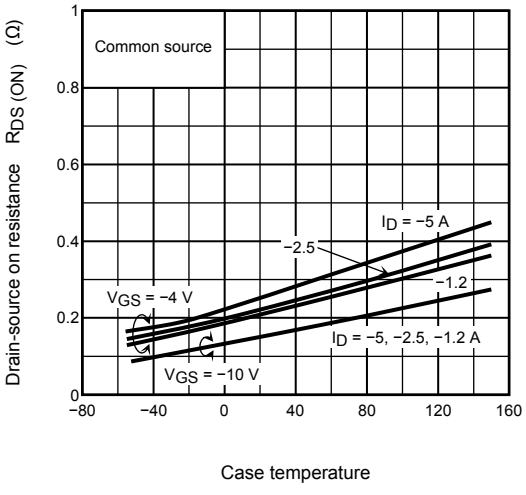
$R_{DS\ (ON)} - I_D$



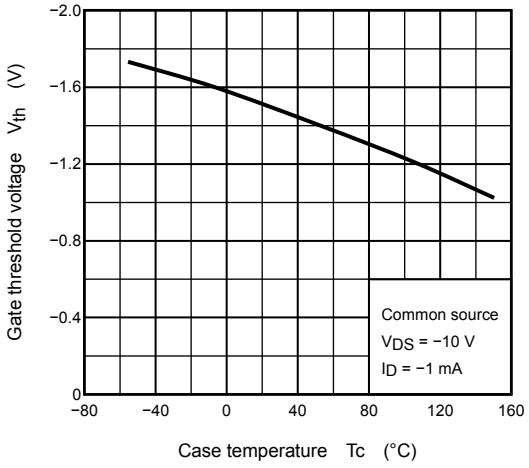
$V_{DS} - V_{GS}$



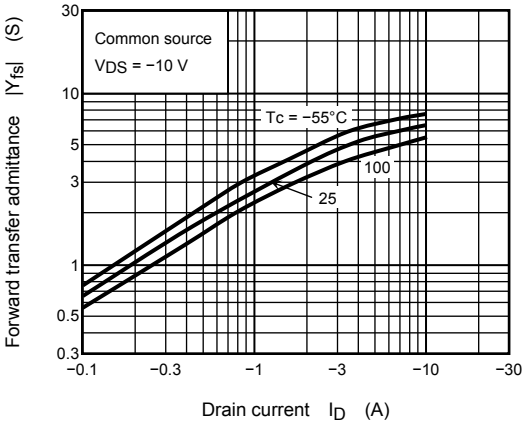
$R_{DS\ (ON)} - Tc$



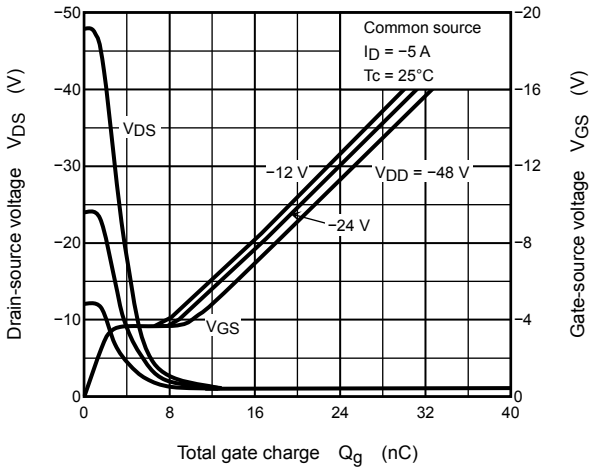
V_{th} – Tc



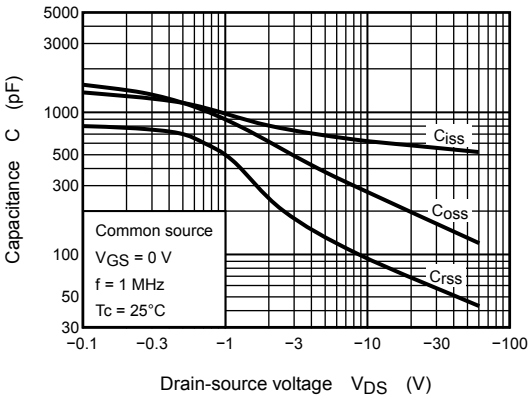
$|Y_{fs}|$ – I_D



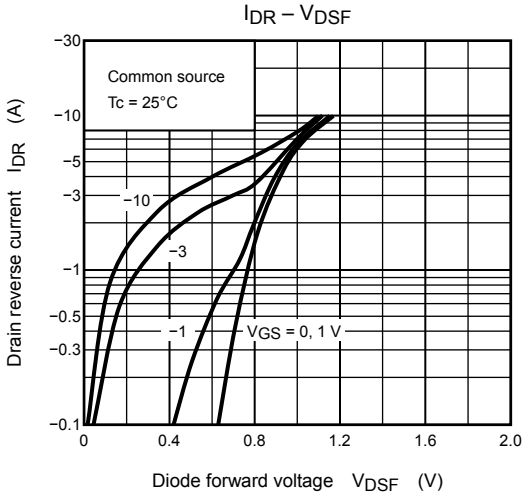
Dynamic Input/Output Characteristics



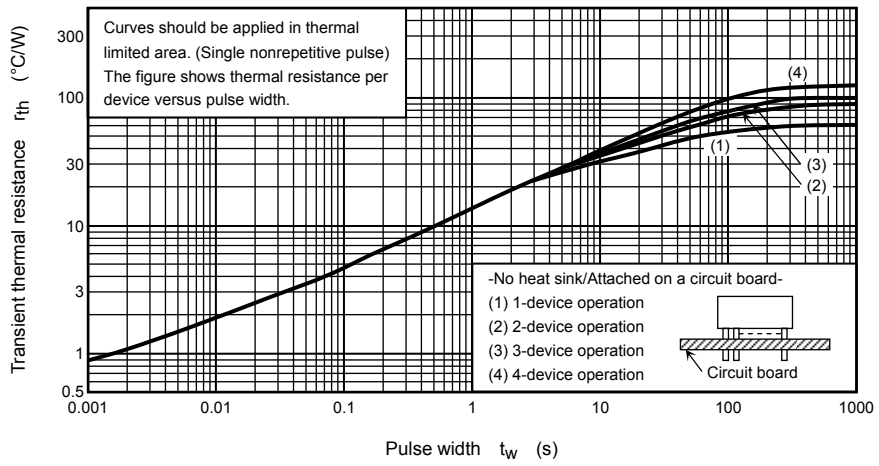
Capacitance – V_{DS}



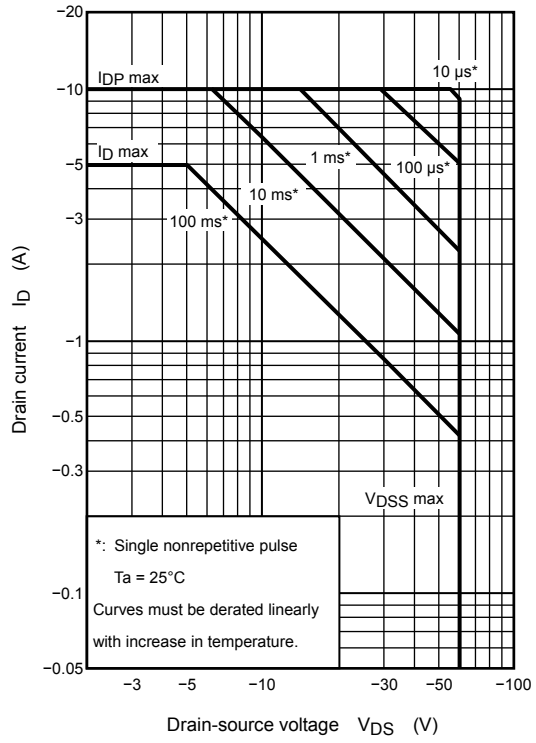
I_{DR} – V_{DSF}



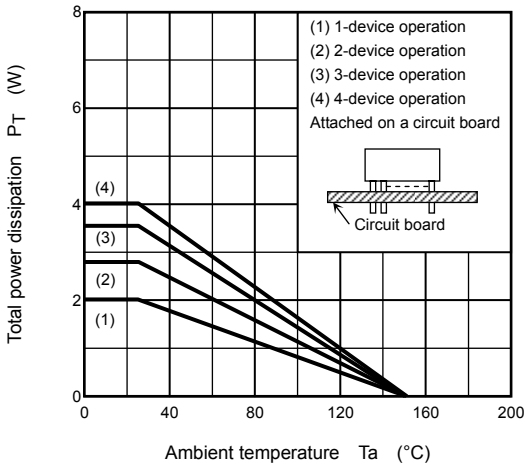
$r_{th} - t_w$



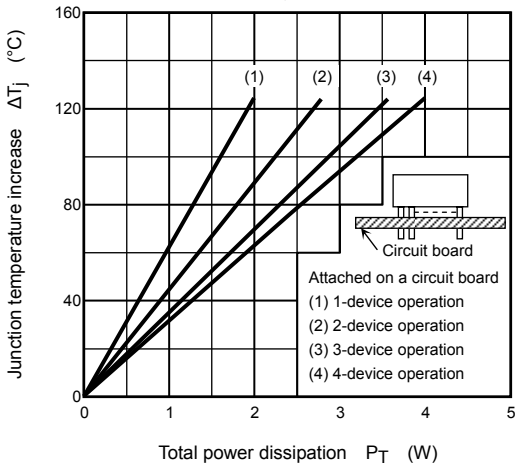
Safe Operating Area



$P_T - Ta$



$\Delta T_j - P_T$



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