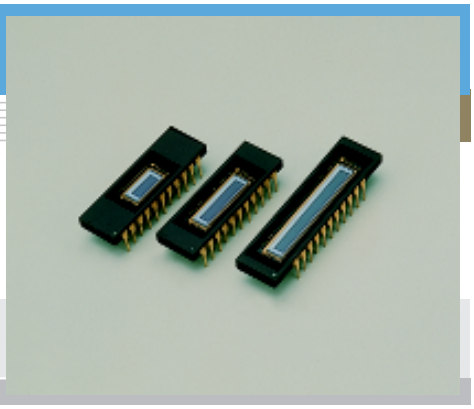
NMOS linear image sensor
S8380/S8381 series

NMOS linear image sensors with high IR sensitivity



S8380/S8381 series are designed to have higher sensitivity in the infrared and soft X-ray regions when compared to standard NMOS linear image sensors. The peak sensitivity wavelength is in the near IR region (λp=750 nm).
The photodiodes of S8380 series have a height of 2.5 mm and are arrayed in a row at a spacing of 50 µm. The photodiodes of S8381 series also have a height of 2.5 mm but are arrayed at a spacing of 25 µm. The photodiodes are available in 3 different pixel quantities for each series, 128 (S8380-128Q), 256 (S8380-256Q, S8381-256Q) and 512 (S8380-512Q, S8381-512Q) and 1024 (S8381-1024Q). Quartz glass is the standard window material.

Features

- High sensitivity in the IR and soft X-ray regions
- Wide active area
  Pixel pitch: 50 µm (S8380 series)
  25 µm (S8381 series)
  Pixel height: 2.5 mm
- High UV sensitivity with good stability
- Low dark current and high saturation charge allow a long integration time and a wide dynamic range at room temperature
- Excellent output linearity and sensitivity spatial uniformity
- Lower power consumption: 1 mW Max.
- Start pulse and clock pulses are CMOS logic compatible

Applications

- Multichannel spectrophotometry
- Image readout system

Figure 1 Equivalent circuit

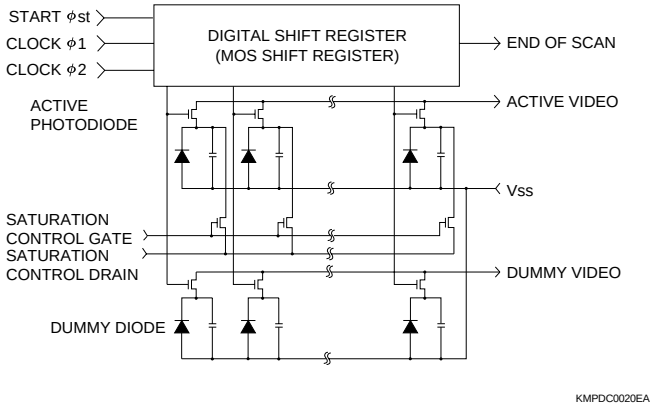
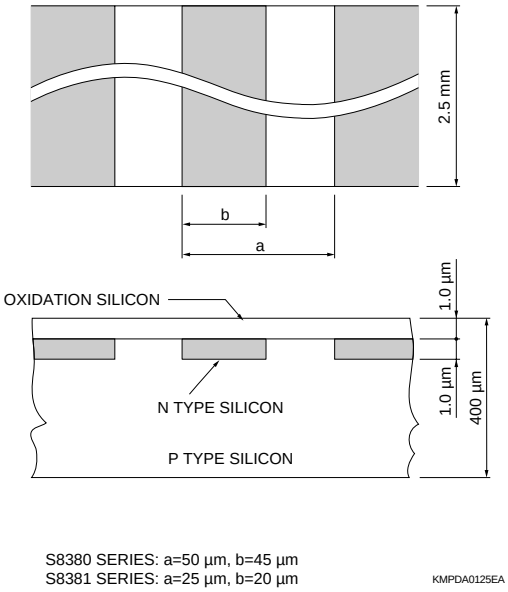


Figure 2 Active area structure



■ Absolute maximum ratings

Parameter	Symbol	Value	Unit
Input pulse (φ1, φ2, φst) voltage	Vφ	15	V
Power consumption *1	P	1	mW
Operating temperature *2	Topr	-40 to +65	°C
Storage temperature	Tstg	-40 to +85	°C

*1: Vφ=5.0 V
*2: No condensation

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■ Shape specifications

Parameter	S8380-128Q	S8380-256Q	S8380-512Q	S8381-256Q	S8381-512Q	S8381-1024Q	Unit
Number of pixels	128	256	512	256	512	1024	-
Package length	31.75		40.6	31.75		40.6	mm
Number of pin	22			22			-
Window material *3	Quartz			Quartz			-
Weight	3.0		3.5	3.0		3.5	g

*3: Fiber optic plate is available.

■ Specifications (Ta=25 °C)

Parameter	Symbol	S8380 series			S8381 series			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Pixel pitch	-	-	50	-	-	25	-	μm
Pixel height	-	-	2.5	-	-	2.5	-	mm
Spectral response range (10 % of peak)	λ	200 to 1000			200 to 1000			nm
Peak sensitivity wavelength	λp	-	750	-	-	750	-	nm
Photodiode dark current *4	ID	-	0.2	0.6	-	0.1	0.3	pA
Photodiode capacitance *4	Cph	-	20	-	-	10	-	pF
Saturation exposure *4, *5	Esat	-	90	-	-	90	-	$mlx \cdot s$
Saturation output charge *4	Qsat	-	50	-	-	25	-	pC
Photo response non-uniformity *6	PRNU	-	-	±3	-	-	±3	%

*4: Vb=2.0 V, Vφ=5.0 V
*5: 2856 K, tungsten lamp
*6: 50 % of saturation, excluding the start pixel and last pixel

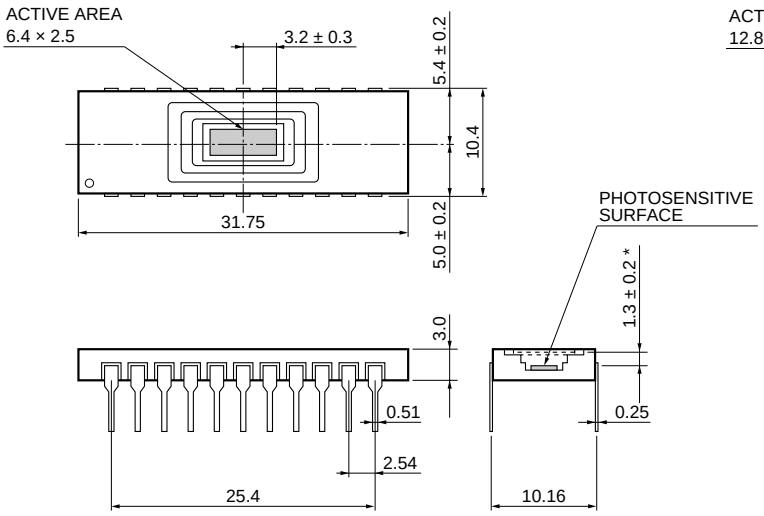
■ Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Condition	S8380 series			S8381 series			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock pulse (φ1, φ2) voltage	High	Vφ1, Vφ2 (H)		4.5	5	10	4.5	5	10	V
	Low	Vφ1, Vφ2 (L)		0	-	0.4	0	-	0.4	V
Start pulse (φst) voltage	High	Vφs (H)		4.5	Vφ1	10	4.5	Vφ1	10	V
	Low	Vφs (L)		0	-	0.4	0	-	0.4	V
Video bias voltage *7		Vb		1.5	Vφ - 3.0	Vφ - 2.5	1.5	Vφ - 3.0	Vφ - 2.5	V
Saturation control gate voltage		Vscg		-	0	-	-	0	-	V
Saturation control drain voltage		Vscd		-	Vb	-	-	Vb	-	V
Clock pulse (φ1, φ2) rise / fall time *8		trφ1, trφ2 tfφ1, tfφ2		-	20	-	-	20	-	ns
Clock pulse (φ1, φ2) pulse width		tpwφ1, tpwφ2		200	-	-	200	-	-	ns
Start pulse (φst) rise / fall time		trφs, tfφs		-	20	-	-	20	-	ns
Start pulse (φst) pulse width		tpwφs		200	-	-	200	-	-	ns
Start pulse (φst) and clock pulse (φ2) overlap		tφov		200	-	-	200	-	-	ns
Clock pulse space *8		X1, X2		trf - 20	-	-	trf - 20	-	-	ns
Data rate *9		f		0.1	-	2000	0.1	-	2000	kHz
Video delay time		tvd	50 % of saturation *9, *10	-	80 (-128 Q)	-	-	100 (-256 Q)	-	ns
				-	120 (-256 Q)	-	-	150 (-512 Q)	-	ns
				-	160 (-512 Q)	-	-	200 (-1024 Q)	-	ns
Clock pulse (φ1, φ2) line capacitance		Cφ	5 V bias	-	21 (-128 Q)	-	-	27 (-256 Q)	-	pF
				-	36 (-256 Q)	-	-	50 (-512 Q)	-	pF
				-	67 (-512 Q)	-	-	100 (-1024 Q)	-	pF
Saturation control gate (Vscg) line capacitance		Cscg	5 V bias	-	12 (-128 Q)	-	-	14 (-256 Q)	-	pF
				-	20 (-256 Q)	-	-	24 (-512 Q)	-	pF
				-	35 (-512 Q)	-	-	45 (-1024 Q)	-	pF
Video line capacitance		CV	2 V bias	-	7 (-128 Q)	-	-	10 (-256 Q)	-	pF
				-	11 (-256 Q)	-	-	16 (-512 Q)	-	pF
				-	20 (-512 Q)	-	-	30 (-1024 Q)	-	pF

*7: Vφ is input pulse voltage (refer to figure 8).
*8: trf is the clock pulse rise or fall time. A clock pulse space of "rise time/fall time - 20" ns (nanoseconds) or more should be input if the clock pulse rise or fall time is longer than 20 ns (refer to figure 7).
*9: Vb=2.0 V, Vφ=5.0 V
*10: Measured with C7883 driver circuit.

Figure 3 Dimensional outlines (unit: mm)

S8380-128Q, S8381-256Q



* Optical distance from the outer surface of the quartz window to the chip surface

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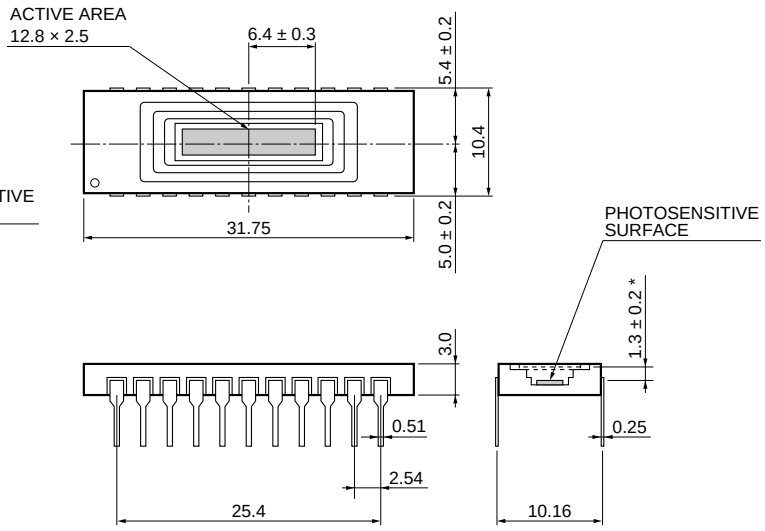
S8380-256Q, S8381-512Q



* Optical distance from the outer surface of the quartz window to the chip surface

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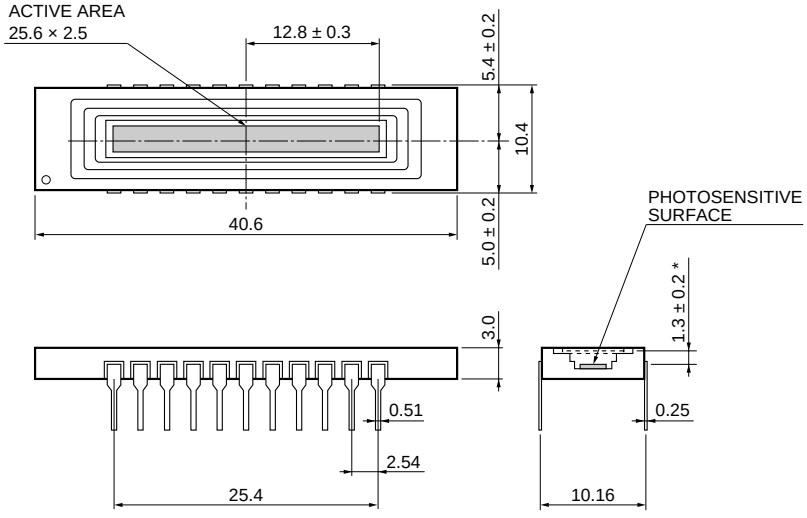
S8380-512Q, S8381-1024Q



* Optical distance from the outer surface of the quartz window to the chip surface

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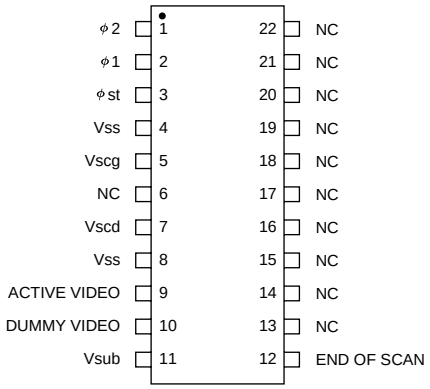
Figure 4 Pin connection



Vss, Vsub and NC should be grounded.

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■ Recommended operating conditions

Terminal	Input or output	Description
ϕ1, ϕ2	Input (CMOS logic compatible)	Pulses for operating the MOS shift register. The video data rate is equal to the clock pulse frequency since the video output signal is obtained synchronously with the rise of ϕ2 pulse.
ϕst	Input (CMOS logic compatible)	Pulse for starting the MOS shift register operation. The time interval between start pulses is equal to the signal accumulation time.
Vss	-	Connected to the anode of each photodiode. This should be grounded.
Vscg	Input	Used for restricting blooming. This should be grounded.
Vscd	Input	Used for restricting blooming. This should be biased at a voltage equal to the video bias voltage.
Active video	Output	Video output signal. Connects to photodiode cathodes when the address is on. A positive voltage should be applied to the video line in order to use photodiodes with a reverse voltage. When the amplitude of ϕ1 and ϕ2 is 5 V, a video bias voltage of 2 V is recommended.
Dummy video	Output	This has the same structure as the active video, but is not connected to photodiodes, so only spike noise is output. This should be biased at a voltage equal to the active video or left as an open-circuit when not needed.
Vsub	-	Connected to the silicon substrate. This should be grounded.
End of scan	Output (CMOS logic compatible)	This should be pulled up at 5 V by using a 10 kΩ resistor. This is a negative going pulse that appears synchronously with the ϕ2 timing right after the last photodiode is addressed.
NC	-	Should be grounded.

Figure 5 Spectral response (typical example)

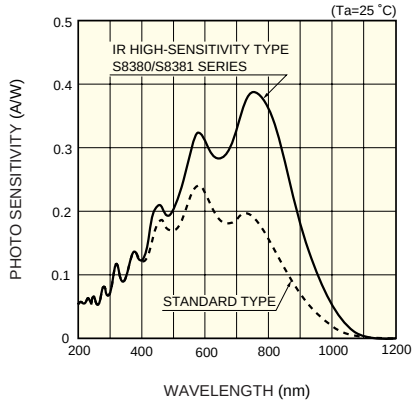


Figure 6 Output charge vs. exposure

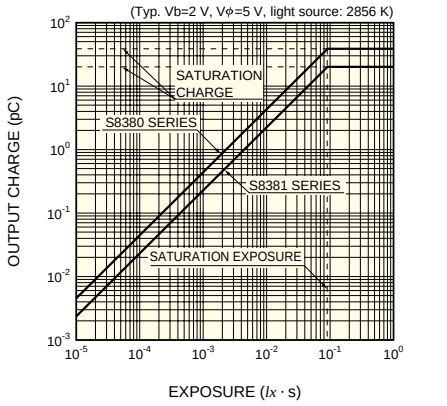


Figure 7 Timing chart for driver circuit

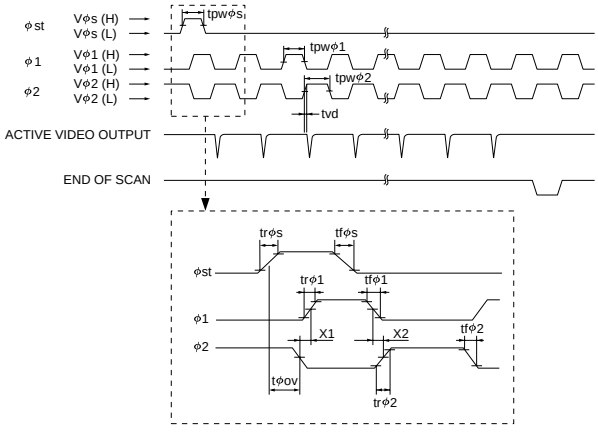
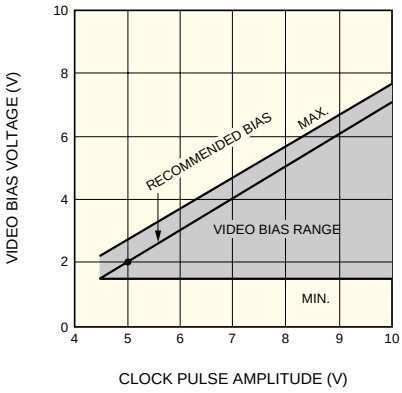


Figure 8 Video bias voltage margin



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