CCD area image sensor
S8665-0909

Four-stage thermoelectric cooled, back-thinned FFT-CCD

S8665-0909 is an FFT-CCD area image sensor featuring low noise and low dark current (MPP mode operation). The output charge can be integrated for long periods of time even at low light levels, allowing a wide dynamic range.
S8665-0909 uses a four-stage thermoelectric cooler that cools the CCD down to -50 ˚C when operated at room temperatures, achieving even lower noise and dark current.

Features

- Four-stage TE-cooled
- Number of active pixels: 512 (H) × 512 (V)
- Pixel size: 24 × 24 µm
- 100 % fill factor
- Wide dynamic range
- Low dark current
- Low readout noise
- MPP operation

Applications

- Astronomy
- Scientific measuring instrument
- UV imaging
- For low-light-level detection requiring

■ Selection guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]
S8665-0909	Four-stage TE-cooled	532 × 520	512 × 512	12.288 × 12.288

■ Specifications

Parameter	Specification
CCD structure	Full frame transfer
Fill factor	100 %
Cooling	Four-stage TE-cooled
Number of pixels	532 (H) × 520 (V)
Number of active pixels	512 (H) × 512 (V)
Pixel size	24 (H) × 24 (V) µm
Active area	12.288 (H) × 12.288 (V) mm
Vertical clock phase	2 phase
Horizontal clock phase	2 phase
Output circuit	One-stage MOSFET source follower
Package	28 pin metal package
Window	AR coated sapphire

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■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	Topr	-50	-	+30	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	V_{OD}	-0.5	-	+25	V
RD voltage	V_{RD}	-0.5	-	+18	V
ISV voltage	V_{ISV}	-0.5	-	+18	V
ISH voltage	V_{ISH}	-0.5	-	+18	V
IGV voltage	V_{IG1V}, V_{IG2V}	-10	-	+15	V
IGH voltage	V_{IG1H}, V_{IG2H}	-10	-	+15	V
SG voltage	V_{SG}	-10	-	+15	V
OG voltage	V_{OG}	-10	-	+15	V
RG voltage	V_{RG}	-10	-	+15	V
TG voltage	V_{TG}	-10	-	+15	V
Vertical clock voltage	V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal clock voltage	V_{P1H}, V_{P2H}	-10	-	+15	V

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{OD}	18	20	22	V
Reset drain voltage		V_{RD}	11.5	12	12.5	V
Output gate voltage		V_{OG}	1	3	5	V
Substrate voltage		V_{SS}	-	0	-	V
Test point (vertical input source)		V_{ISV}	-	V_{RD}	-	V
Test point (horizontal input source)		V_{ISH}	-	V_{RD}	-	V
Test point (vertical input gate)		V_{IG1V}, V_{IG2V}	-8	0	-	V
Test point (horizontal input gate)		V_{IG1H}, V_{IG2H}	-8	0	-	V
Vertical shift register clock voltage	High	V_{P1VH}, V_{P2VH}	4	6	8	V
	Low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage	High	V_{P1HH}, V_{P2HH}	4	6	8	V
	Low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Summing gate voltage	High	V_{SGH}	4	6	8	V
	Low	V_{SGL}	-9	-8	-7	
Reset gate voltage	High	V_{RGH}	4	6	8	V
	Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage	High	V_{TGH}	4	6	8	V
	Low	V_{TGL}	-9	-8	-7	

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	1	MHz
Vertical shift register capacitance	C_{P1V}, C_{P2V}	-	6,400	-	pF
Horizontal shift register capacitance	C_{P1H}, C_{P2H}	-	120	-	pF
Summing gate capacitance	C_{SG}	-	7	-	pF
Reset gate capacitance	C_{RG}	-	7	-	pF
Transfer gate capacitance	C_{TG}	-	150	-	pF
Charge transfer efficiency *1	CTE	0.99995	0.99999	-	-
DC output level *2	Vout	12	15	18	V
Output impedance *2	Zo	-	3	-	kΩ
Power consumption *2 *3	P	-	15	-	mW

*1: Charge transfer efficiency per pixel, measured at half of the full well capacity.
*2: The values depend on the load resistance. (Typical, V_{OD}=20 V, Load resistance=22 kΩ)
*3: Power consumption of the on-chip amplifier.

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

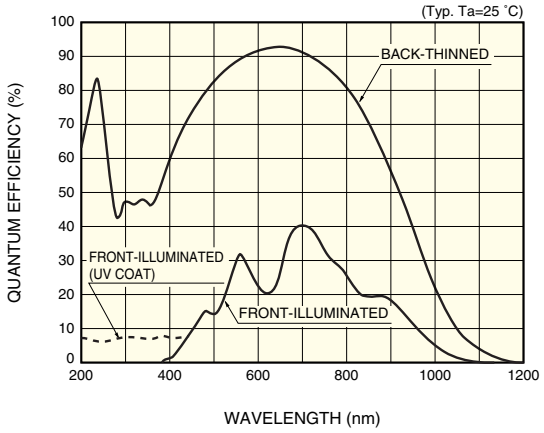
Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat	-	-	Fw × Sv	-	V
Full well capacity	Vertical	Fw	*4	150	300	-	ke⁻
	Horizontal			300	600	-	
CCD node sensitivity		Sv	*5	1.8	2.2	-	μV/e⁻
Dark current (MPP mode)	+25 °C	DS	*6	-	4,000	12,000	e⁻/pixel/s
	0 °C			-	200	600	
	-30 °C			-	3	9	
Readout noise		Nr	*7	-	8	12	e⁻rms
Dynamic range	Line binning	DR	*8	-	75,000	-	-
	Area scanning			-	37,500	-	
Spectral response range		λ	-	-	200 to 1100	-	nm
Photo response non-uniformity		PRNU	*9	-	-	±10	%
Blemish	Point defect	-	*10	-	-	10	-
	Cluster defect		*11	-	-	3	
	Column defect		*12	-	-	0	

*4: Large horizontal full well capacity for line binning operation.
*5: V_{OD}=20 V, load resistance=22 kΩ.
*6: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*7: -40 °C, operating frequency is 80 kHz.
*8: Dynamic range DR=Full well capacity/Readout noise
*9: Measured at half of the full well capacity output.

$$\text{Photo response non-uniformity (PRNU) [\%]} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

*10: White spots > 3 % of full well at 0 °C after Ts=1 s, Black spots > 50 % reduction in response relative to adjacent pixels.
*11: Continuous 2 to 9 point defects.
*12: Continuous ≥ 10 point defects.

■ Spectral response (without window) *13



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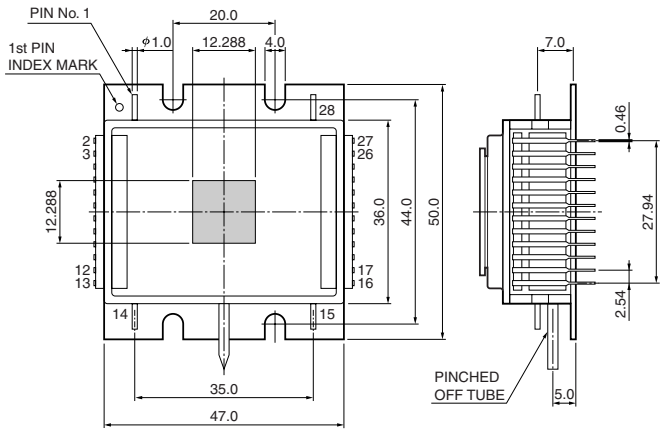
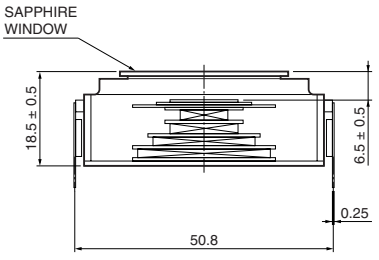
*13: Spectral response with sapphire window is decreased by the transmittance

■ Dimensional outline (unit: mm)





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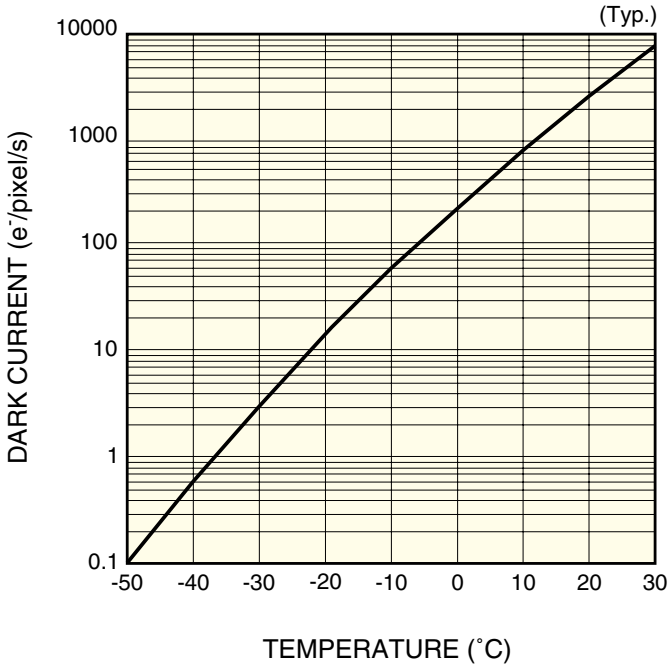
■ Dark current vs. temperature



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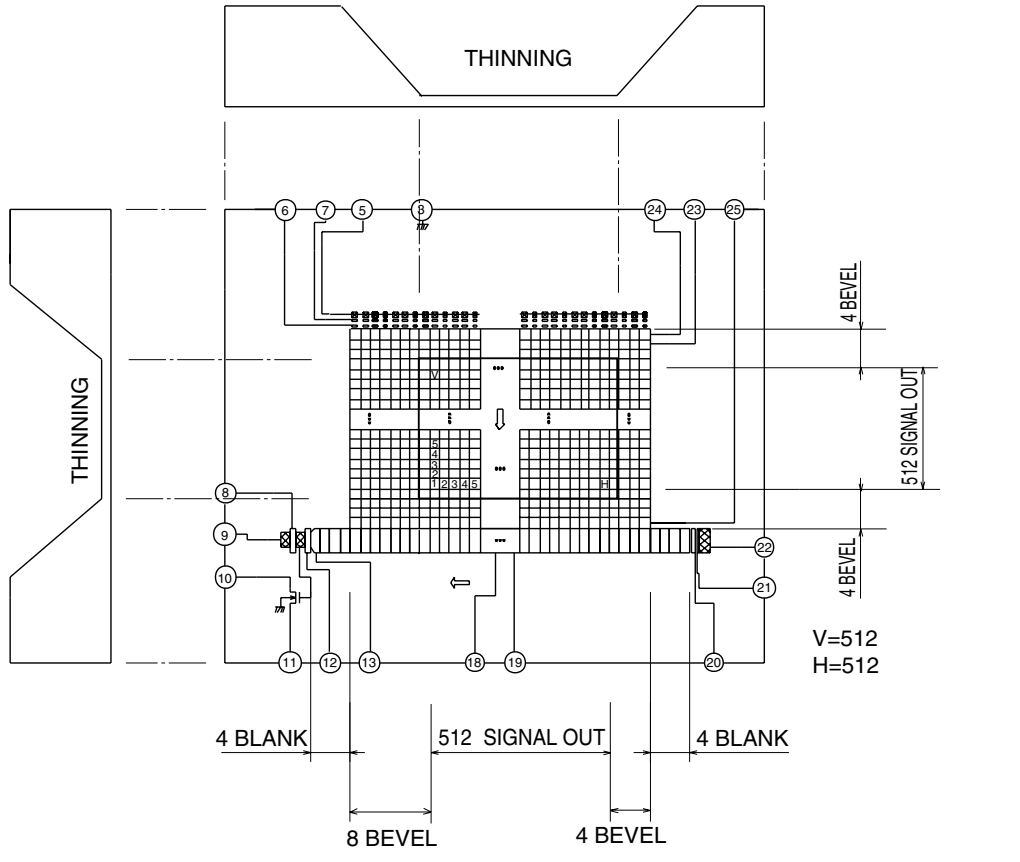
■ Device structure



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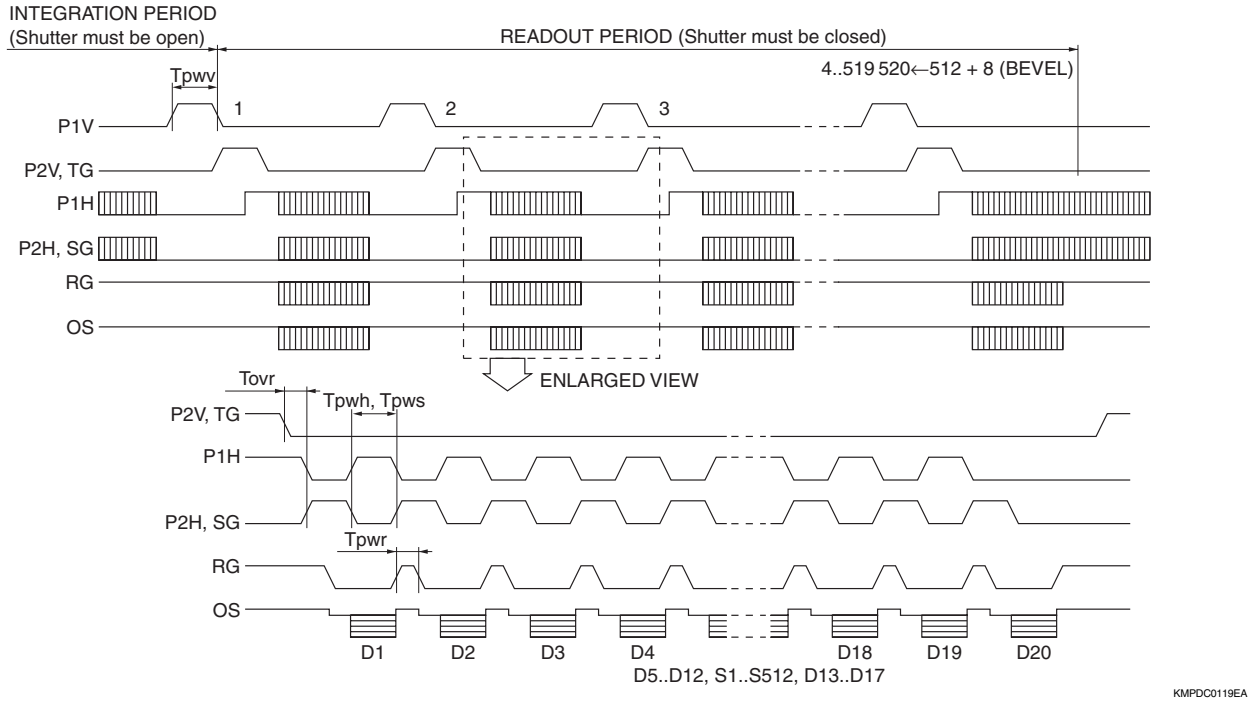
■ PIN connections

Pin No.	Symbol	Description	Remark
1	P-	TE-cooler-	
2	NC		
3	SS	Substrate (GND)	
4	NC		
5	ISV	Test point (vertical input source)	Shorted to RD
6	IG2V	Test point (vertical input gate-2)	Shorted to 0 V
7	IG1V	Test point (vertical input gate-1)	Shorted to 0 V
8	RG	Reset gate	
9	RD	Reset drain	
10	OS	Output transistor source	
11	OD	Output transistor drain	
12	OG	Output gate	
13	SG	Summing gate	Same timing as P2H
14	P+	TE-cooler+	
15	TSH1	Temperature sensor (hot side)	
16	TSC1	Temperature sensor (cool side)	
17	TSC2	Temperature sensor (cool side)	
18	P2H	CCD horizontal register clock-2	
19	P1H	CCD horizontal register clock-1	
20	IG2H	Test point (horizontal input gate-2)	Shorted to 0 V
21	IG1H	Test point (horizontal input gate-1)	Shorted to 0 V
22	ISH	Test point (horizontal input source)	Shorted to RD
23	P2V	CCD vertical register clock-2	
24	P1V	CCD vertical register clock-1	
25	TG	Transfer gate	Same timing as P2V *14
26	NC		
27	NC		
28	TSH2	Temperature sensor (hot side)	

*14: TG is an isolation gate between vertical register and horizontal resister.
In standard operation, the same pulse of P2V should be applied to the TG.

■ Timing chart

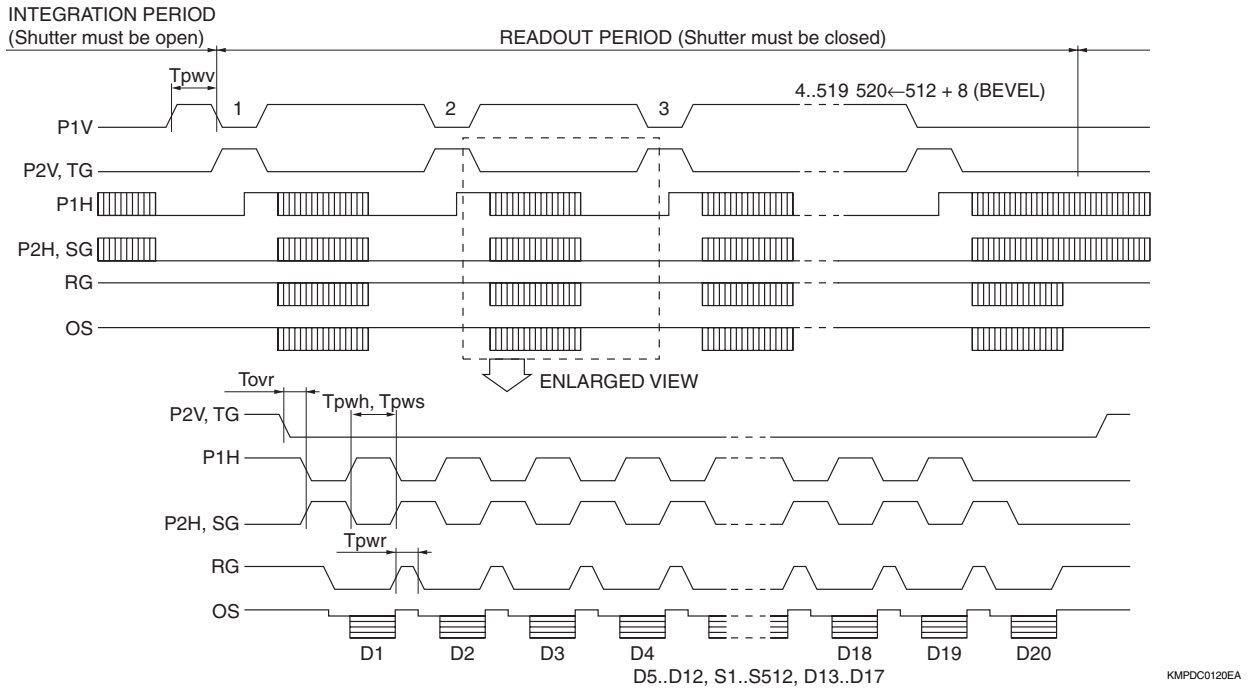
Area scanning 1 (low dark current mode)



Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*15	6	-	-	µs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*15	500	-	-	ns
	Rise and fall time	Tprh, pfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	-	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	Overlap time	Tovr	-	3	-	-	µs

*15: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

Area scanning 2 (large full well mode)



Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width	Tpwv	*16	6	-	-	µs
	Rise and fall time	Tprv, Tpfv		200	-	-	ns
P1H, P2H	Pulse width	Tpwh	*16	500	-	-	ns
	Rise and fall time	Tprh, Tpfh		10	-	-	ns
	Duty ratio	-		-	50	-	%
SG	Pulse width	Tpws	-	500	-	-	ns
	Rise and fall time	Tprs, Tpfs		10	-	-	ns
	Duty ratio	-		-	50	-	%
RG	Pulse width	Tpwr	-	100	-	-	ns
	Rise and fall time	Tprr, Tpfr		5	-	-	ns
TG - P1H	Overlap time	Tovr	-	3	-	-	µs

*16: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

■ Specifications of built-in TE-cooler

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal resistance	Rint	Ta=27 °C	-	1.6	-	Ω
Maximum current *17	Imax	Th *18=27 °C ΔT *19=ΔTmax	-	-	4.4	A
Maximum voltage	Vmax	Th*18=27 °C ΔT=ΔTmax I=Imax	-	-	7.4	V
Maximum heat absorption *20	Qmax	Tc *21=Th *19=27 °C I=Imax	-	-	3.0	W
Maximum temperature at hot side	-		-	-	50	°C
CCD temperature	-	Ta=25 °C	-	-50	-30	°C

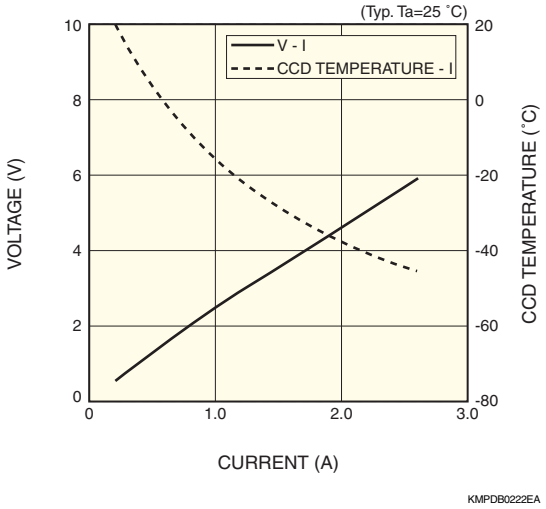
*17: If the current is greater than Imax, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not a damage threshold. To protect the thermoelectric cooler (Peltier element) and maintain stable operation, the supply current should be less than 60 % of this maximum current.

*18: Temperature at hot side of thermoelectric cooler.

*19: ΔT=Th - Tc

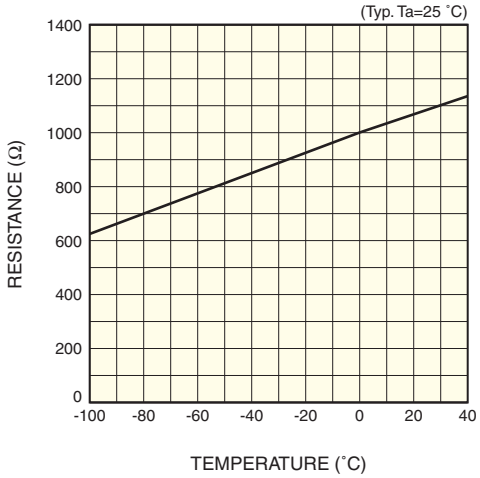
*20: This is a theoretical heat absorption level that offsets the temperature difference in the Peltier element when the maximum current is supplied to the unit.

*21: Temperature at cool side of thermoelectric cooler.



■ Specifications of built-in temperature sensors

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resistance at cool side	Rc	T=0 °C	-	1,000	-	Ω
Temperature coefficient of resistance at cool side	-	-	-	0.00375	-	Ω/Ω
Resistance at hot side	Rh	T=0 °C	-	1,000	-	Ω
Temperature coefficient of resistance at hot side	-	-	-	0.00385	-	Ω/Ω



■ Precaution for use (electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature incline rate

Element cooling/heating temperature incline rate should be set at less than 5 K/min.

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