

STN2NF10

N-channel 100V - 0.23Ω - 2.4A - SOT-223 STripFET™ II Power MOSFET

Features

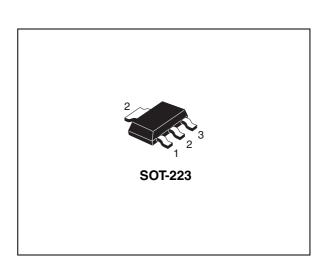
Туре	V _{DSS}	R _{DS(on)}	I _D
STN2NF10	100V	< 0.26Ω	2.4A

Description

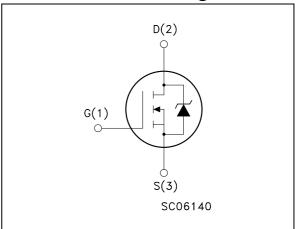
This Power MOSFET is the latest development of STMicroelectronics unique "single feature size" strip-based process. The resulting transistor shows extremely high packing density for low onresistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Application

- Switching application
 - DC-DC converters



Internal schematic diagram



Order code

Part number	Marking	Package	Packaging	
STN2NF10	N2NF10	SOT-223	Tape & reel	

Contents STN2NF10

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STN2NF10 Electrical ratings

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} =0)	100	V
V _{GS}	Gate-source voltage	± 20	V
I _D	Drain current (continuous) at T _C = 25°C	2.4	Α
I _D	Drain current (continuous) at T _C = 100°C	1.5	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	17	Α
	Derating factor	0.026	W/°C
P _{TOT} ⁽²⁾	Total dissipation at T _C = 25°C	3.3	W
E _{AS} (3)	Single pulse avalanche energy	200	mJ
dv/dt (4)	Peak diode recovery voltage slope	30	V/ns
T _j T _{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

- 1. Pulse width limited by safe operating area
- 2. This value is rated according to Rthj-amb, $t \le 10$ sec
- 3. $I_{AS} = 2.4A$, $V_{DD} = 30V$, $Rg=4.7\Omega$, starting Tj = 25°C
- 4. $I_{SD} \le 6A$, $di/dt \le 500A/\mu s$, $V_{DD} = 80\% V_{(BR)DSS}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
Rthj-amb (1) Thermal resistance junction-amb		38	°C/W
Rthj-amb (2)	Thermal resistance junction-amb	62.5	°C/W

- 1. When mounted on 1inch² FR-4 board, 2 oz. Cu, (t < 10sec)
- 2. When mounted on 1inch 2 FR-4 board, 2 oz. Cu, (t >10sec)

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2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter Test conditions		Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	100			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating, Tc=125°C V_{DS} = 30V, Tc=125°C			1 10 1	μΑ μΑ μΑ
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2		4	٧
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10V, I _D = 1.2A		0.23	0.26	Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
9 _{fs}	Forward transconductance	V _{DS} =15V, I _D =1.2A		2.5		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} =25V, f=1MHz, V _{GS} =0		280 45 20		pF pF pF
$egin{array}{c} Q_{ m g} \ Q_{ m gd} \end{array}$	Total gate charge Gate-source charge Gate-drain charge	V_{DD} =80V, I_{D} = 6A V_{GS} =10V (see Figure 15)		10 2.5 4	14	nC nC nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time Rise time	V_{DD} =50V, I_D = 2.4A V_{GS} =10V, R_G =4.7 Ω (see Figure 14)		6 10		ns ns
t _{d(off)}	Turn-off delay time Fall time	V_{DD} =50V, I_{D} = 2.4A V_{GS} =10V, R_{G} =4.7 Ω (see Figure 14)		20 3		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max	Unit
I _{SD}	Source-drain current Source-drain current (pulsed)				2.4 17	A A
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 2.4A, V _{GS} =0			1.2	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I _{SD} = 6A, V _{DD} =10V di/dt=100A/μs,Tj=150°C (see Figure 19)		70 175 5		ns nC A

^{1.} Pulse width limited by safe operating area

^{2.} Pulsed: pulse duration = 300µs, duty cycle 1.5%

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2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance

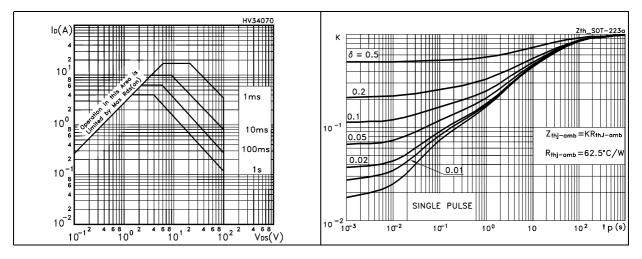


Figure 3. Output characteristics

Figure 4. Transfer characteristics

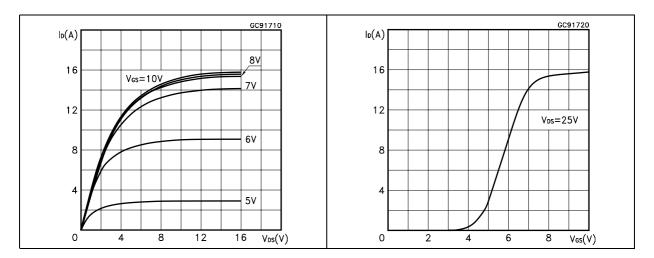
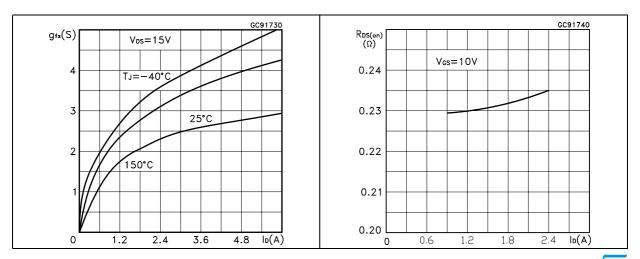


Figure 5. Transconductance

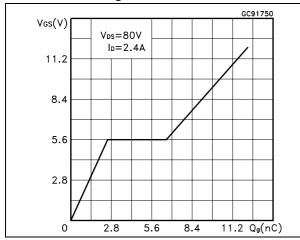
Figure 6. Static drain-source on resistance



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Figure 7. Gate charge vs. gate-source voltage

Figure 8. Capacitance variations



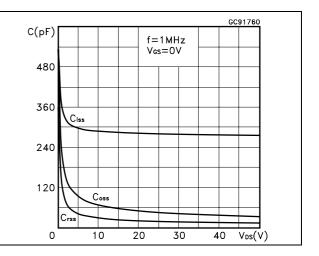
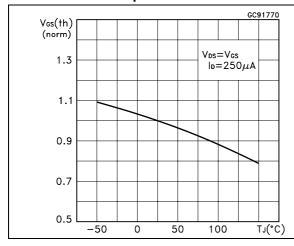


Figure 9. Normalized gate threshold voltage Figure 10. vs. temperature

Figure 10. Normalized on resistance vs. temperature



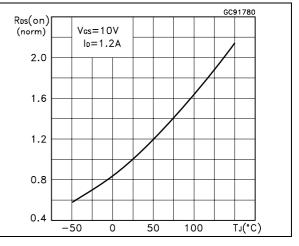
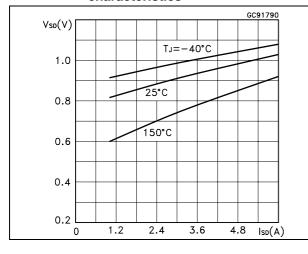
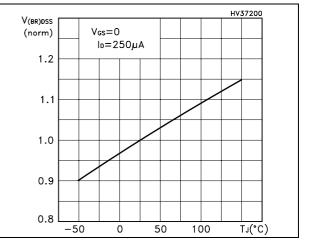


Figure 11. Source-drain diode forward characteristics

Figure 12. Normalized BV_DSS vs. temperature

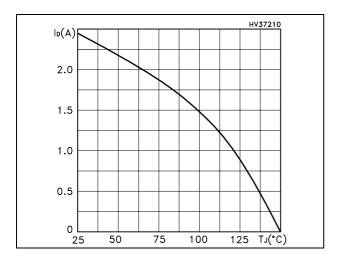




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Figure 13. Max drain current vs. temperature



STN2NF10 Test circuit

3 Test circuit

Figure 14. Switching times test circuit for resistive load

Figure 15. Gate charge test circuit

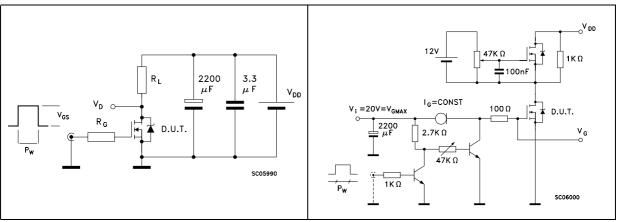


Figure 16. Test circuit for inductive load switching and diode recovery times

Figure 17. Unclamped inductive load test circuit

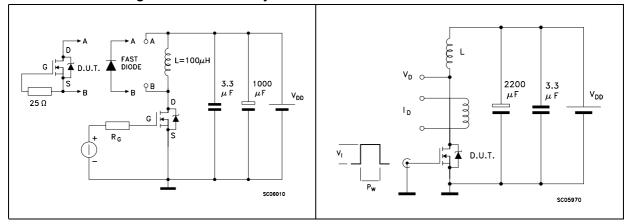
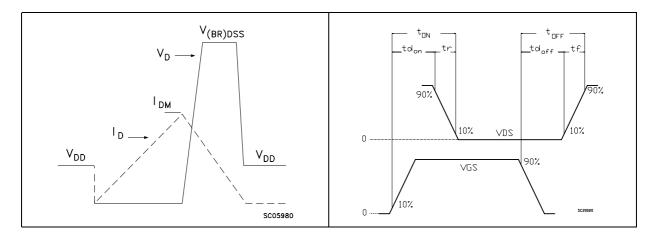


Figure 18. Unclamped inductive waveform

Figure 19. Switching time waveform



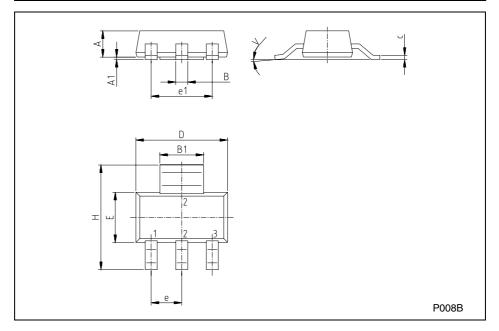
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4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

SOT-223 MECHANICAL DATA

DIM.		mm			inch	
Dini.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
Α			1.80			0.071
В	0.60	0.70	0.80	0.024	0.027	0.031
B1	2.90	3.00	3.10	0.114	0.118	0.122
С	0.24	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
е		2.30			0.090	
e1		4.60			0.181	
E	3.30	3.50	3.70	0.130	0.138	0.146
Н	6.70	7.00	7.30	0.264	0.276	0.287
V			10°			10°
A1		0.02				



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Revision history STN2NF10

5 Revision history

Table 7. Revision history

Date	Revision	Changes
14-Sep-2006	4	The document has been reformatted
29-Mar-2007	5	Figure 1 has been updated
04-Apr-2007	6	New test condition for I _{DSS} on <i>Table 3</i>

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