# N-Channel Enhancement-Mode Vertical DMOS FET

## Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low $C_{ISS}$ and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

## Applications

- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

## General Description

This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

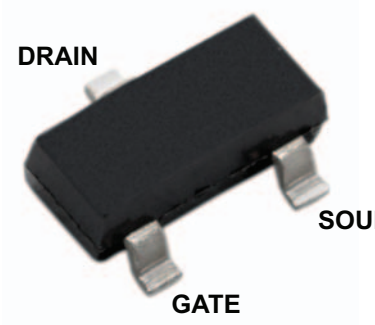
Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

## Ordering Information

| $BV_{DSS}/BV_{DGS}$ (V) | $R_{DS(ON)}$ max (Ω) | $V_{GS(th)}$ max (V) | Package Option |
|---|---|---|---|
| | | | TO-236AB (SOT-23) |
| 240 | 15 | 2.0 | TN2124K1-G |

*-G indicates package is RoHS compliant ('Green')*

## Pin Configuration




**TO-236AB (SOT-23) (K1)**

## Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| Drain-to-source voltage | $BV_{DSS}$ |
| Drain-to-gate voltage | $BV_{DGS}$ |
| Gate-to-source voltage | ±20V |
| Operating and storage temperature | -55°C to +150°C |
| Soldering temperature* | 300°C |

*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

** Distance of 1.6mm from case for 10 seconds.*

## Product Marking


W = Code for week sealed

**TO-236AB (SOT-23) (K1)**

## Thermal Characteristics

| Package | $I_D$ (continuous)(*) (mA) | $I_D$ (pulsed) (mA) | Power Dissipation @$T_A$ = 25°C (W) | $\theta_{jc}$ (°C/W) | $\theta_{ja}$ (°C/W) | $I_{DR}$(*) (mA) | $I_{DRM}$ (mA) |
|---|---|---|---|---|---|---|---|
| TO-236AB (SOT-23) (K1) | 134 | 250 | 0.36 | 200 | 350 | 134 | 250 |

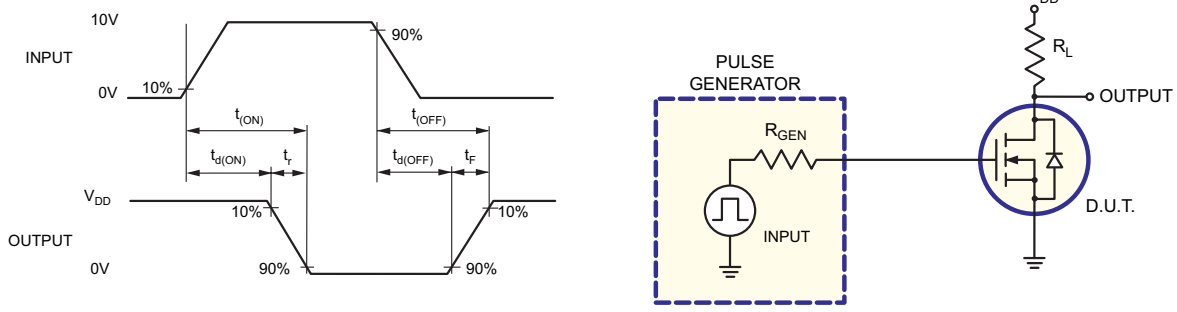
***Notes:***
* $I_D$ *(continuous) is limited by max rated* $T_j$ .

## Electrical Characteristics *(@25°C unless otherwise specified)*

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-source breakdown voltage | 240 | - | - | V | $V_{GS}$ = 0V, $I_D$ = 1.0mA |
| $V_{GS(th)}$ | Gate threshold voltage | 0.8 | - | 2.0 | V | $V_{GS}$ = $V_{DS}$, $I_D$= 1.0mA |
| $\Delta V_{GS(th)}$ | Change in $V_{GS(th)}$ with temperature | - | - | -5.5 | mV/°C | $V_{GS}$ = $V_{DS}$, $I_D$= 1.0mA |
| $I_{GSS}$ | Gate body leakage | - | 0.1 | 100 | nA | $V_{GS}$ = ± 20V, $V_{DS}$ = 0V |
| $I_{DSS}$ | Zero gate voltage drain current | - | - | 1.0 | µA | $V_{GS}$ = 0V, $V_{DS}$ = Max Rating |
| | | - | - | 100 | µA | $V_{GS}$ = 0V, $V_{DS}$ = 0.8 Max Rating, $T_A$ = 125°C |
| $I_{D(ON)}$ | ON-state drain current | 140 | - | - | mA | $V_{GS}$ = 4.5V, $V_{DS}$ = 25V |
| $R_{DS(ON)}$ | Static drain-to-source ON-state resistance | - | - | 30 | Ω | $V_{GS}$ = 3.0V, $I_D$ = 25mA |
| | | - | - | 15 | Ω | $V_{GS}$ = 4.5V, $I_D$ = 120mA |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with temperature | - | 0.7 | 1.0 | %/°C | $V_{GS}$ = 4.5V, $I_D$ = 120mA |
| $G_{FS}$ | Forward transductance | 100 | 170 | - | mmho | $V_{DS}$ = 25V, $I_D$ = 120mA |
| $C_{ISS}$ | Input capacitance | - | 38 | 50 | pF | $V_{GS}$ = 0V, $V_{DS}$ = 25V, f = 1.0MHz |
| $C_{OSS}$ | Common source output capacitance | - | 9.0 | 15 | | |
| $C_{RSS}$ | Reverse transfer capacitance | - | 3.0 | 5.0 | | |
| $t_{d(ON)}$ | Turn-ON delay time | - | 4.0 | 7.0 | ns | $V_{DD}$ = 25V, $I_D$ = 140mA, $R_{GEN}$ = 25Ω |
| $t_r$ | Rise time | - | 2.0 | 5.0 | | |
| $t_{d(OFF)}$ | Turn-OFF delay time | - | 7.0 | 10 | | |
| $t_f$ | Fall time | - | 9.0 | 12 | | |
| $V_{SD}$ | Diode forward voltage drop | - | - | 1.8 | V | $V_{GS}$ = 0V, $I_{SD}$ = 120mA |
| $t_{rr}$ | Reverse recovery time | - | 400 | - | ns | $V_{GS}$ = 0V, $I_{SD}$ = 120mA |

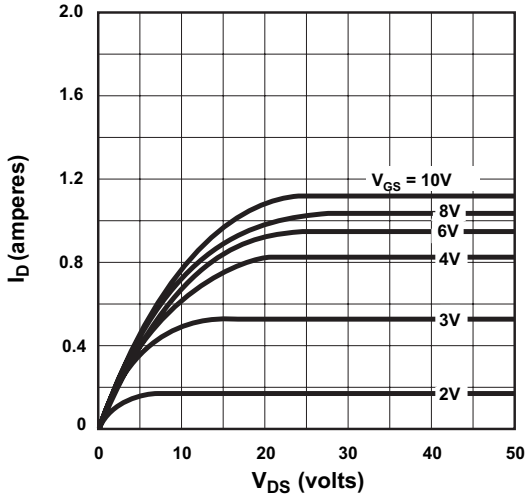
***Notes:***
*(1) All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
*(2) All A.C. parameters sample tested.*

## Switching Waveforms and Test Circuit

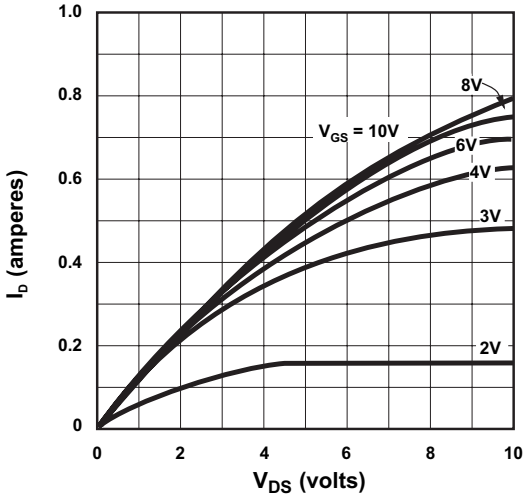


## Typical Performance Curves

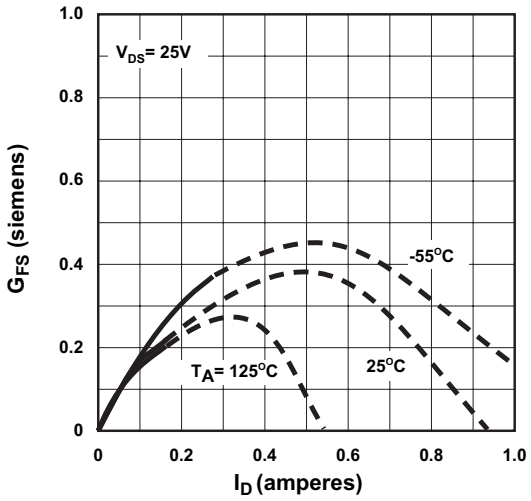
Output Characteristics



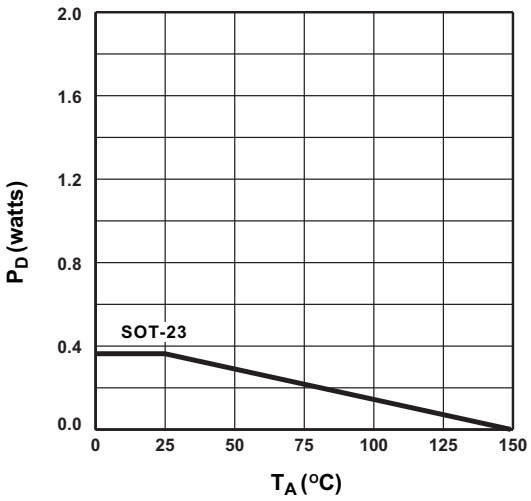

Saturation Characteristics



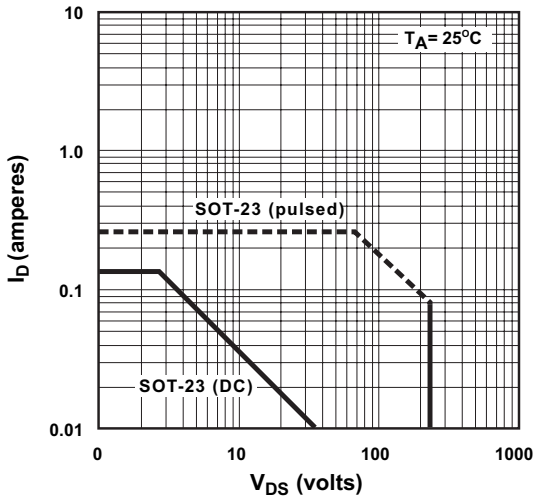

Transconductance vs. Drain Current



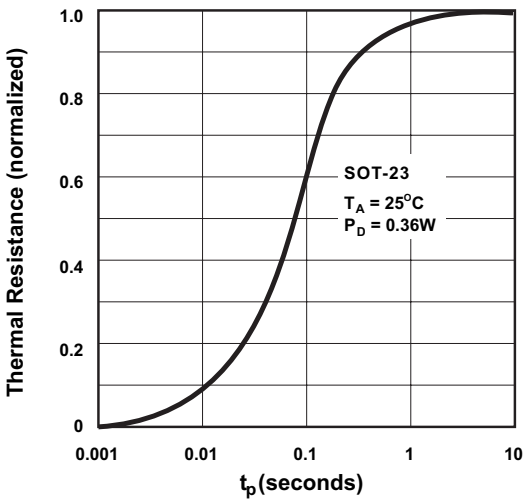

Power Dissipation vs. Temperature




Maximum Rated Safe Operating Area

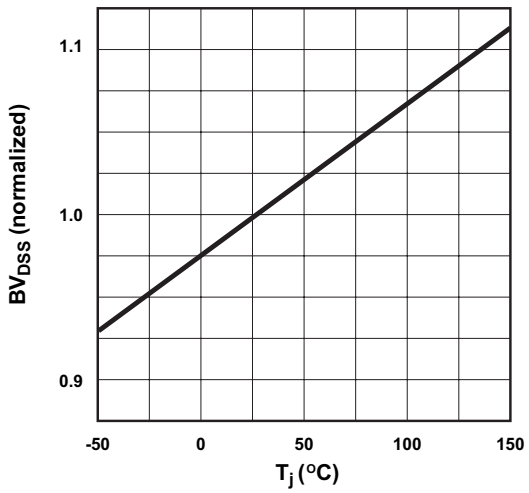



Thermal Response Characteristics

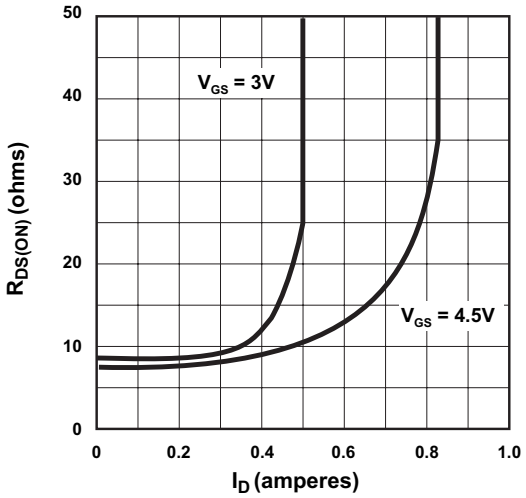


## Typical Performance Curves *(cont.)*

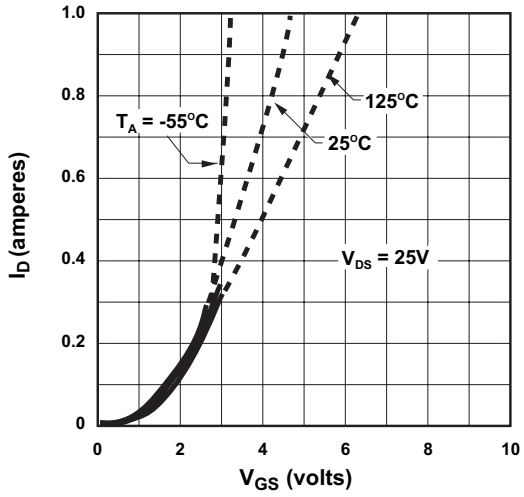
**$BV_{DSS}$ Variation with Temperature**



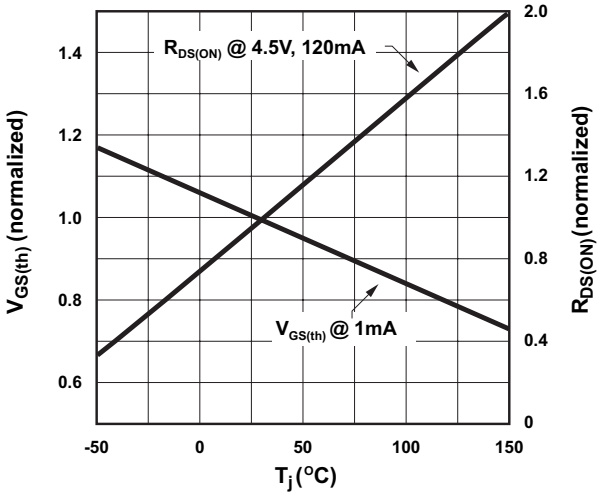

**On-Resistance vs. Drain Current**



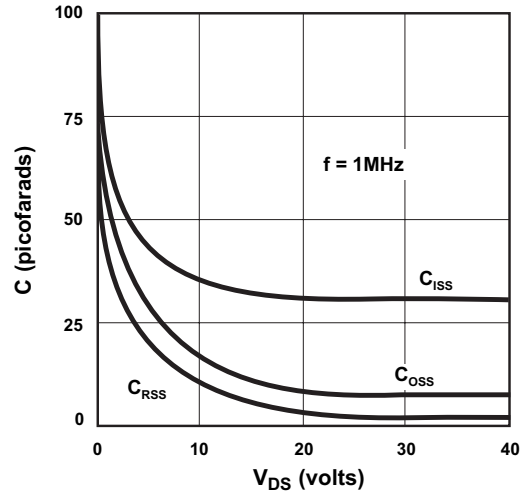

**Transfer Characteristics**



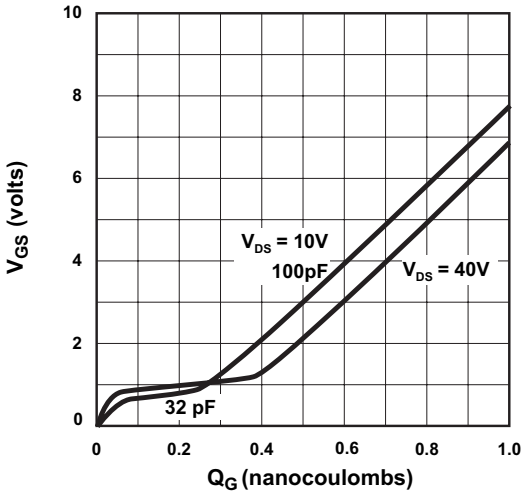

**$V_{TH}$ and $R_{DS}$ Variation with Temperature**




**Capacitance vs. Drain-to-Source Voltage**

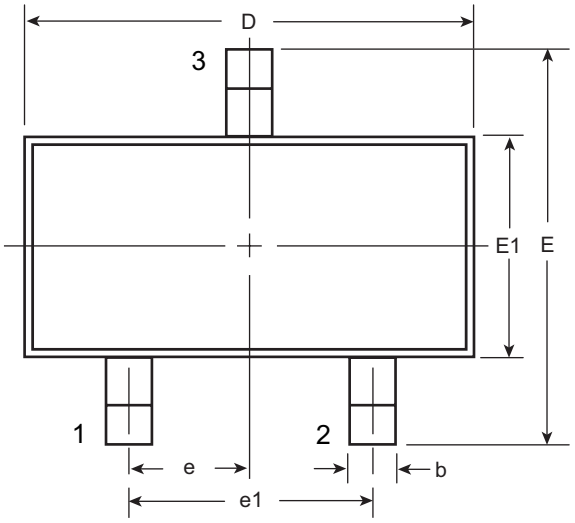



**Gate Drive Dynamic Characteristics**

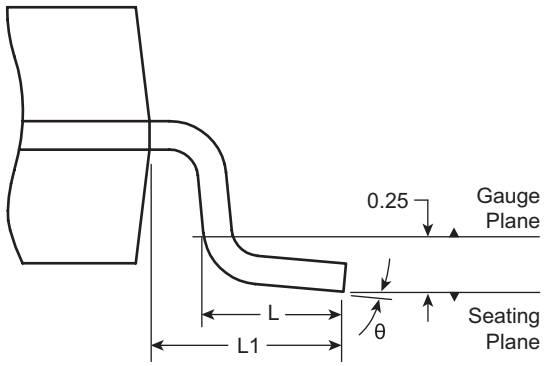


# 3-Lead TO-236AB (SOT-23) Package Outline (K1)

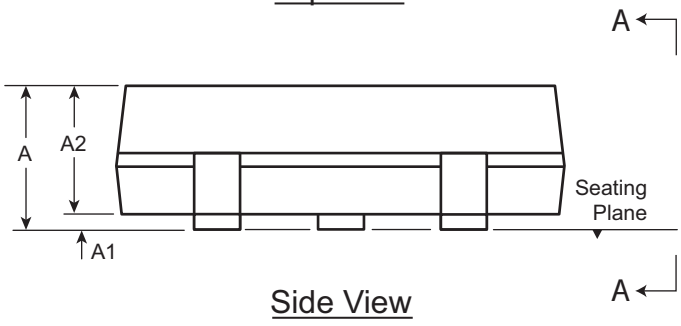
***2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch***



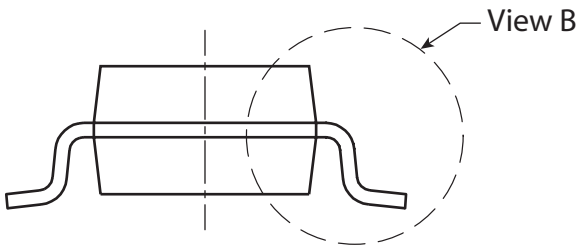

Top View




View B




Side View




View A-A

| Symbol | | A | A1 | A2 | b | D | E | E1 | e | e1 | L | L1 | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (mm) | MIN | 0.89 | 0.01 | 0.88 | 0.30 | 2.80 | 2.10 | 1.20 | 0.95 BSC | 1.90 BSC | 0.40 | 0.54 REF | 0° |
| | NOM | - | - | 0.95 | - | 2.90 | - | 1.30 | | | 0.50 | | - |
| | MAX | 1.12 | 0.10 | 1.02 | 0.50 | 3.04 | 2.64 | 1.40 | | | 0.60 | | 8° |

*JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.*
***Drawings not to scale.***

*(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)*



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