



## P- Channel Enhancement-Mode Vertical DMOS FETs

### Features

- ▶ Low threshold — -2.0V max.
- ▶ High input impedance
- ▶ Low input capacitance
- ▶ Fast switching speeds
- ▶ Low on resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage
- ▶ Complementary N- and P-channel devices

### Applications

- ▶ Logic level interfaces – ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

### General Description

These low threshold enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex’s well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally induced secondary breakdown.

Supertex’s vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

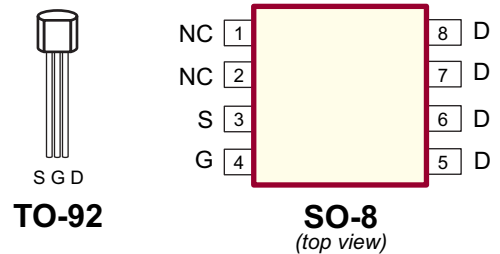
### Absolute Maximum Ratings

Parameter	Value
Drain to source voltage	$BV_{DSS}$
Drain to gate voltage	$BV_{DGS}$
Gate to source voltage	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering temperature <sup>1</sup>	$+300^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

**Note 1.** Distance of 1.6mm from case for 10 seconds.

### Pin Configurations



### Ordering Information

Device	Package Options		$BV_{DSS}/BV_{DGS}$	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)
	SO-8	TO-92				
TP2635	-	TP2635N3	-350V	15Ω	-2.0V	-0.7A
	-	TP2635N3-G				
TP2640	TP2640LG	TP2640N3	-400V	15Ω	-2.0V	-0.7A
	TP2640LG-G	TP2640N3-G				

-G indicates package is RoHS compliant ("Green")

### Thermal Characteristics

Package	I <sub>D</sub> (continuous) <sup>1</sup>	I <sub>D</sub> (pulsed)	Power Dissipation @T <sub>c</sub> = 25°C	θ <sub>jc</sub> (°C/W)	θ <sub>jc</sub> (°C/W)	I <sub>DR</sub> <sup>1</sup>	I <sub>DRM</sub>
SO-8	-210mA	-1.25A	1.3W <sup>2</sup>	24	96 <sup>2</sup>	210mA	-1.25A
TO-92	-180mA	-0.8A	1.0W	125	170	-180mA	-0.8A

**Notes:**

1. I<sub>D</sub> (continuous) is limited by max rated T<sub>f</sub>.
2. Mounted on FR4 board, 25mm x 25mm x 1.57mm

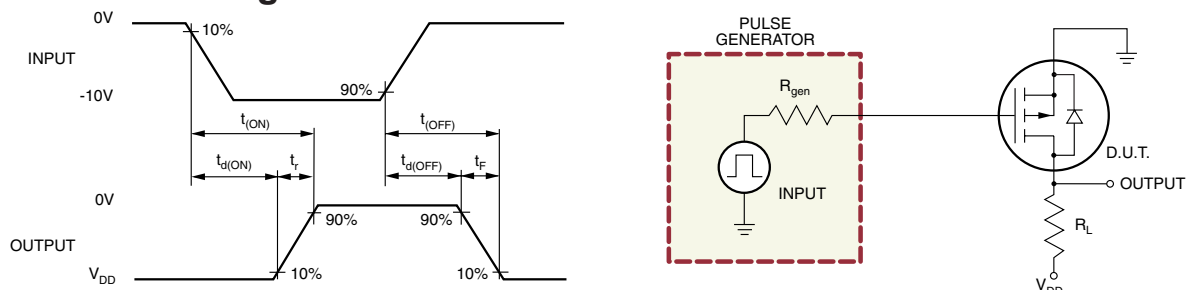
### Electrical Characteristics (T<sub>J</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
BV <sub>DSS</sub>	Drain-to-source break-down voltage	TP2640	-400	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -2.0mA
		TP2635	-350	-	-		
V <sub>GS(th)</sub>	Gate threshold voltage	-0.8	-	-2.0	V	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -1.0mA	
ΔV <sub>GS(th)</sub>	Change in V <sub>GS(th)</sub> with temperature	-	-	5	mV/°C	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -1.0mA	
I <sub>GSS</sub>	Gate body leakage	-	-	-100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V	
I <sub>DSS</sub>	Zero gate voltage drain current	-	-	-1.0	μA	V <sub>DS</sub> = -100V, V <sub>GS</sub> = 0V	
		-	-	-10.0	μA	V <sub>DS</sub> = Max rating, V <sub>GS</sub> = 0V	
		-	-	-1.0	mA	V <sub>DS</sub> = 0.8 Max Rating, V <sub>GS</sub> = 0V, T <sub>A</sub> = 125°C	
I <sub>D(ON)</sub>	ON-state drain current	0.7	-	-	A	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -25V	
R <sub>DS(ON)</sub>	Static drain-to-source ON-state resistance	-	12	15	Ω	V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -200mA	
		-	11	15		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -150mA	
		-	11	15		V <sub>GS</sub> = -10V, I <sub>D</sub> = -300mA	
ΔR <sub>DS(ON)</sub>	Change in R <sub>DS(ON)</sub> with temperature	-	-	0.75	%/°C	V <sub>GS</sub> = -10V, I <sub>D</sub> = -300mA	
G <sub>FS</sub>	Forward transconductance	200	-	-	mΩ	V <sub>DS</sub> = -25V, I <sub>D</sub> = -300mA	
C <sub>ISS</sub>	Input capacitance	-	-	300	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -25V, f = 1MHz	
C <sub>OSS</sub>	Common source output capacitance	-	-	50			
C <sub>RSS</sub>	Reverse transfer capacitance	-	-	12			
t <sub>d(ON)</sub>	Turn-ON delay time	-	-	10	ns	V <sub>DD</sub> = 25V, I <sub>D</sub> = 2.0A, R <sub>GEN</sub> = 25Ω	
t <sub>r</sub>	Rise time	-	-	15			
t <sub>d(OFF)</sub>	Turn-OFF delay time	-	-	60			
t <sub>f</sub>	Fall time	-	-	40			
V <sub>SD</sub>	Diode forward voltage drop	-	-	-1.8	V	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 200mA	
t <sub>rr</sub>	Reverse recovery time	-	300	-	ns	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 1.0A	

**Notes:**

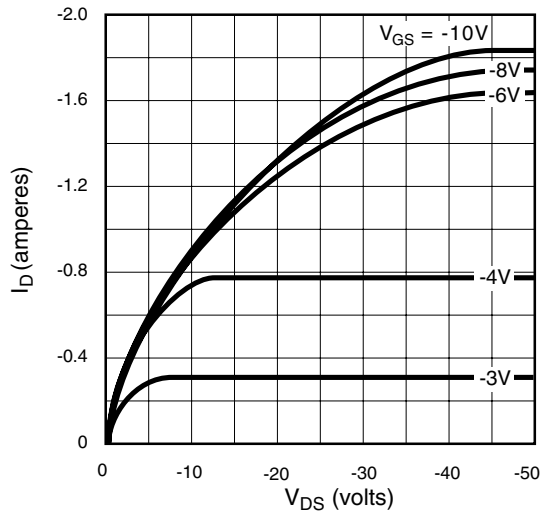
1. All D.C. parameters 100% tested at 25C unless otherwise stated. (Pulse test: 300s pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

### N- Channel Switching Waveforms and Test Circuit

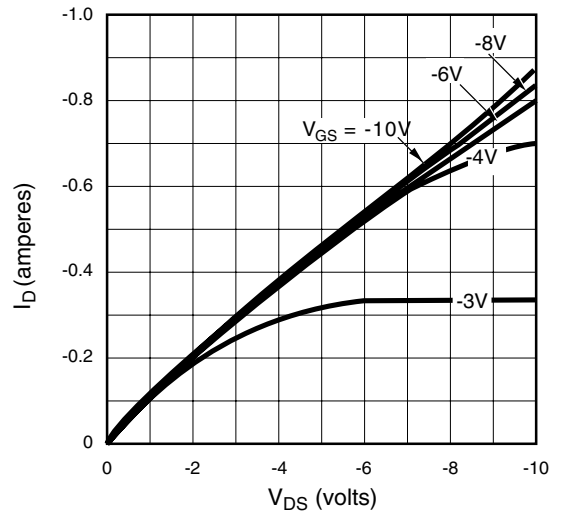


# Typical Performance Curves

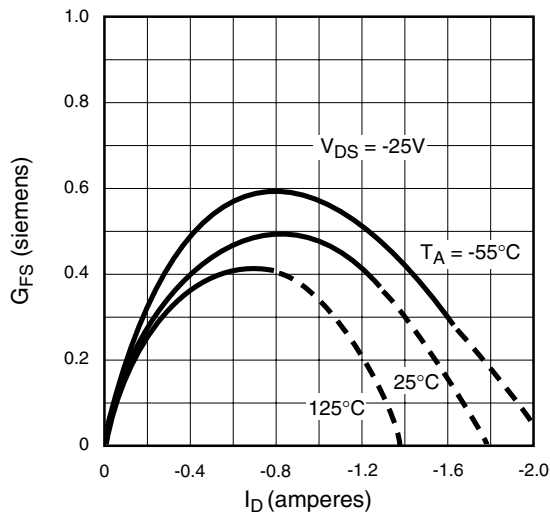
Output Characteristics



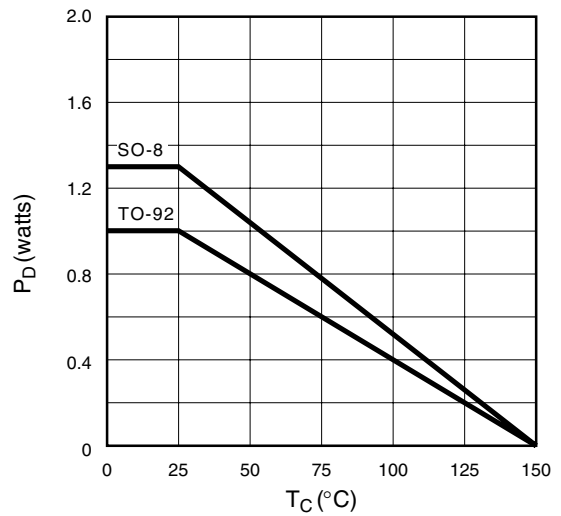
Saturation Characteristics



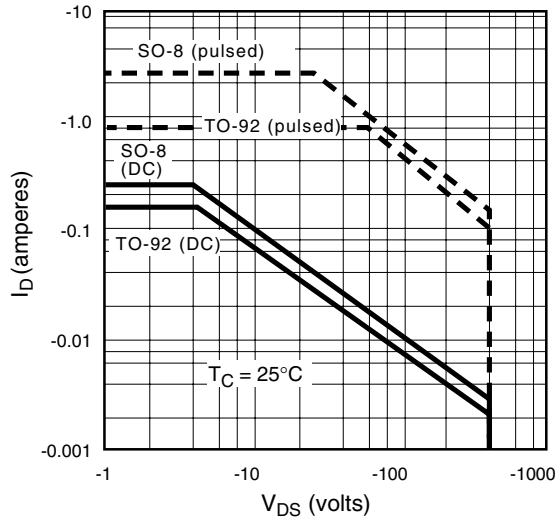
Transconductance vs. Drain Current



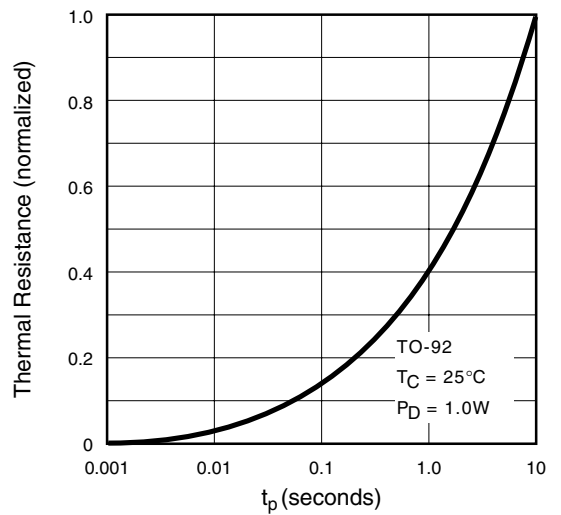
Power Dissipation vs. Temperature



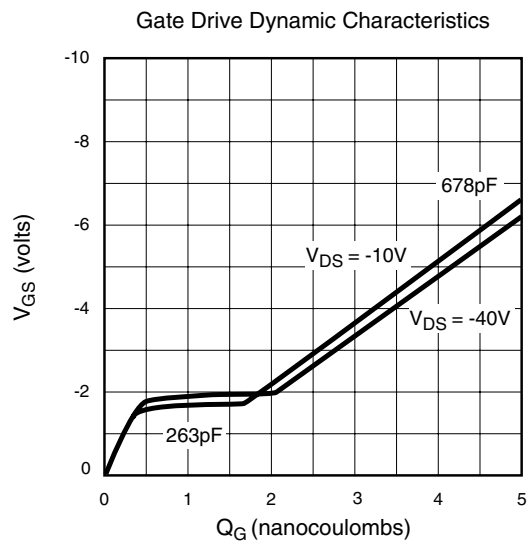
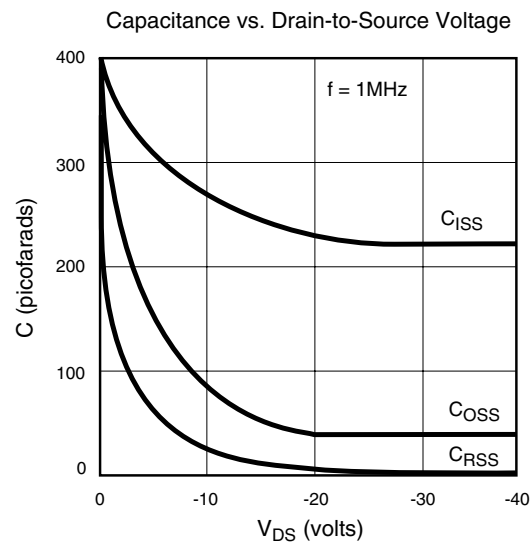
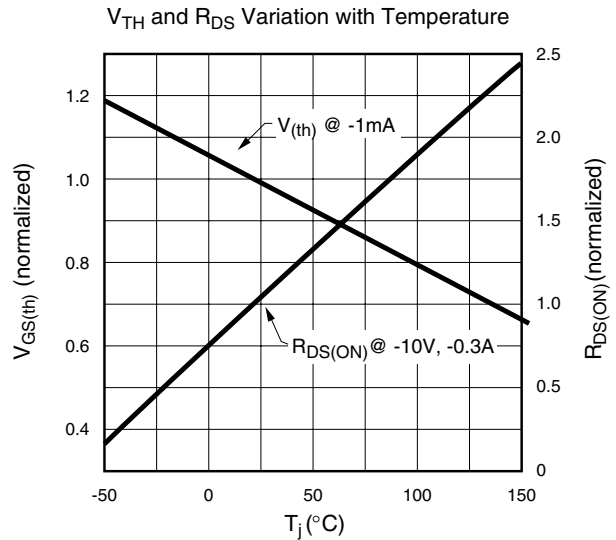
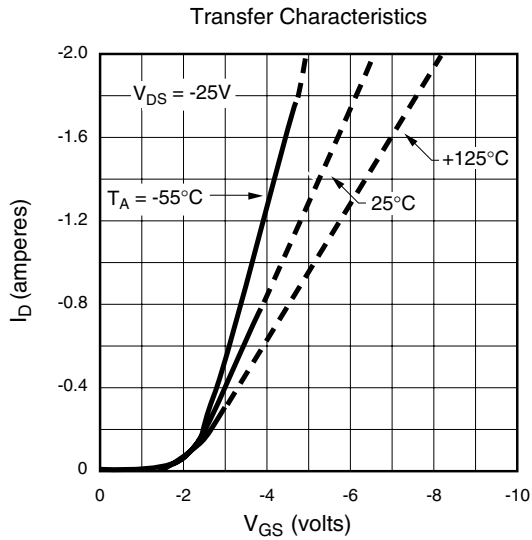
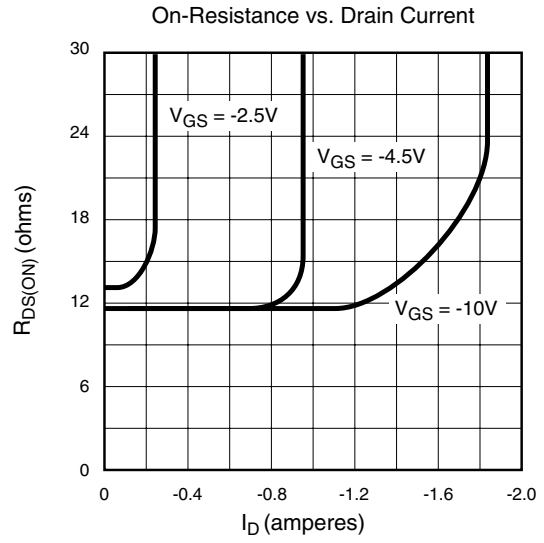
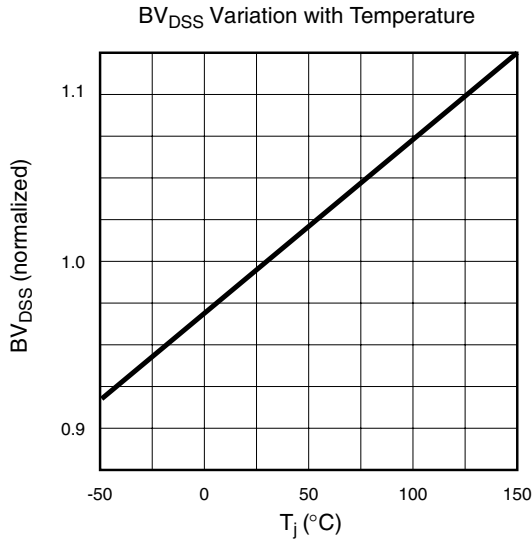
Maximum Rated Safe Operating Area



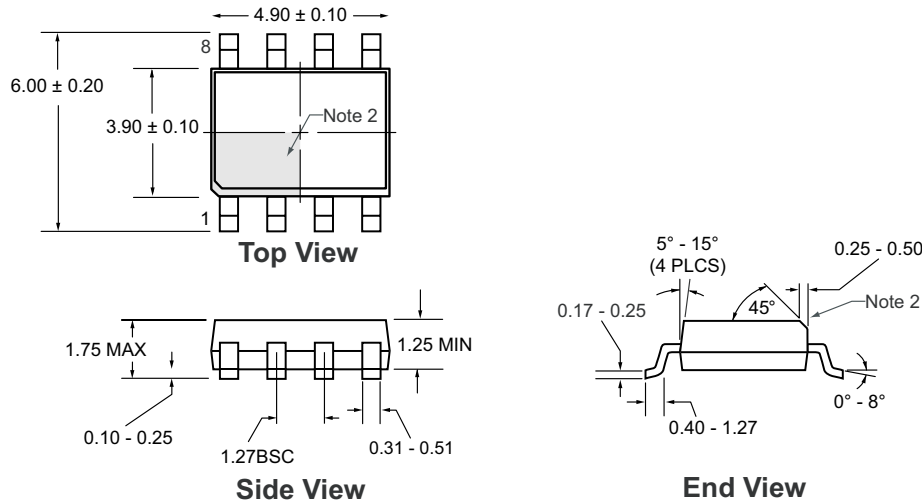
Thermal Response Characteristics



Typical Performance Curves (cont.)



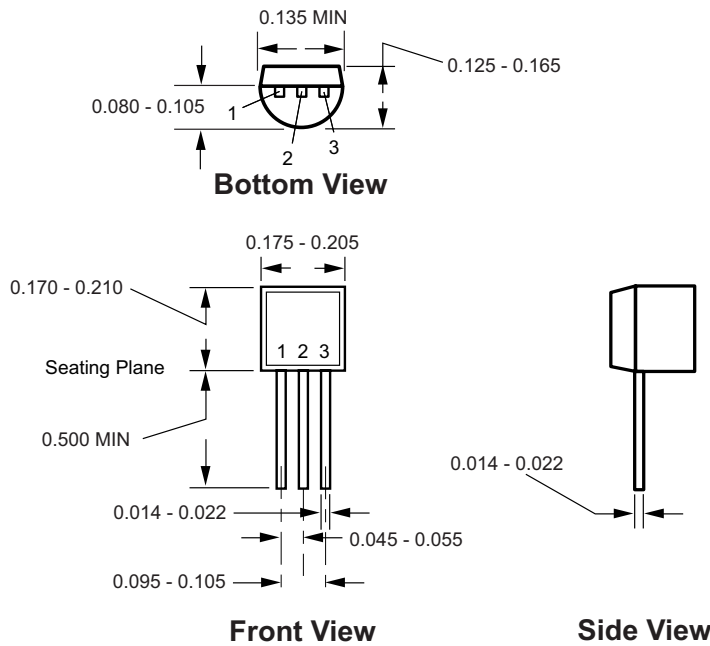
### 8-Lead SOIC Package Outline (LG)



Notes:

1. All dimensions in millimeters. Angles in degrees.
2. If the corner is not chamfered, then a Pin 1 identifier must be located within the area indicated.

### 3-Lead TO-92 Package Outline (N3)



Notes:

All dimensions are in millimeters; all angles in degrees.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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