19-1024; Rev 0; 10/07

DisplayPort to DVI/HDMI Level Shifter

General Description

The MAX9406 high-speed, low-skew, quad differential input to current-mode logic (CML) translator features high-speed signal conversion of the DisplayPort (DP) to High-Definition Multimedia Interface (HDMI™) technology. This device features ultra-low propagation delay of 350ps and channel-to-channel skew of less than 20ps. The MAX9406 supports typical data rates of 2Gbps.

The MAX9406 provides the level shift for HDMI's Display Data Channel (DDC) and hot-plug detection (HPD), which converts the 5V single-ended logic to 3.3V single-ended logic.

The MAX9406 operates from a 3V to 3.6V core supply and is specified over the -40°C to +85°C extended temperature range. This device is available in 48-pin, 7mm x 7mm thin QFN and 32-pin, 5mm x 5mm thin QFN packages.

Applications

Level Conversion for DP to HDMI

Data and Clock Driver and Buffer

Backplane Data and Clock Distribution

Base Stations

ATE

HDMI is a trademark of HDMI Licensing, LCC.

Features

- **500mV Differential HDMI Output at 2Gbps Data Rate**
- **350ps Propagation Delay**
- **20ps Channel-to-Channel Skew at 2Gbps**
- **Low Jitters: DJ = 11ps$_{P-P}$ and RJ = 0.5ps$_{RMS}$**
- **Bidirectional Level Shifter of 5V to 3.3V for DDC Pins**
- **Level Shifter of 5V to 3.3V for I/Os**
- **Integrated 50Ω Input Terminations and Biasing**
- **-40°C to +85°C Operating Temperature Range**

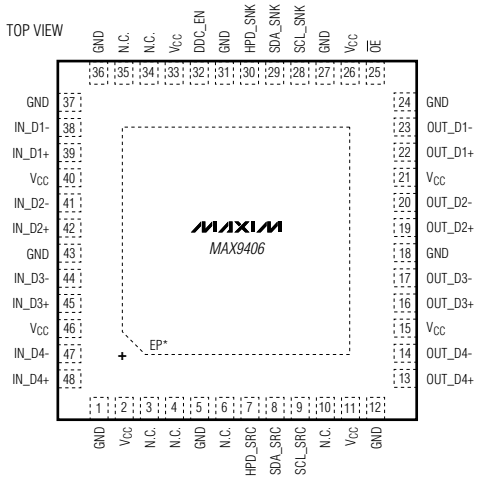
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9406ETJ+	-40°C to +85°C	32 Thin QFN-EP* (5mm x 5mm x 0.8mm)	T3255-4
MAX9406ETM+	-40°C to +85°C	48 Thin QFN-EP* (7mm x 7mm x 0.8mm)	T4877-6

+Denotes a lead-free package.

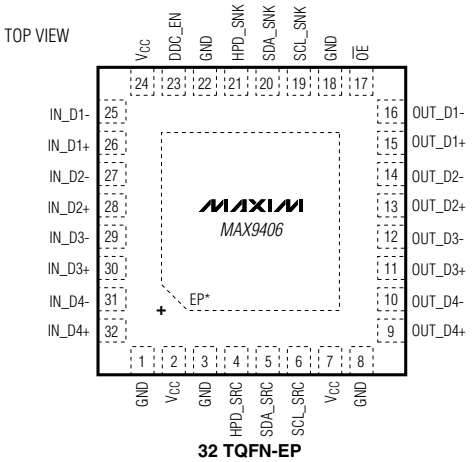
**EP = Exposed paddle.*

Pin Configurations



48 TQFN-EP
7mm × 7mm

*EP EXPOSED PADDLE. CONNECT EP TO GND.



32 TQFN-EP
5mm × 5mm

*EP EXPOSED PADDLE. CONNECT EP TO GND.

DisplayPort to DVI/HDMI Level Shifter

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4V
All Pins to GND.....-0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration (all outputs).....Continuous
Continuous Power Dissipation (T_A = +70°C)
32-Pin Thin QFN (derate 21.3mW/°C above +70°C) .1702mW
48-Pin Thin QFN (derate 27.8mW/°C above +70°C) .2222mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
32-Pin Thin QFN.....+1.7°C/W
48-Pin Thin QFN.....+0.8°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
32-Pin Thin QFN.....+29°C/W
48-Pin Thin QFN.....+25°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
IN_D_ and OUT_D_ to GND.....±1.5kV
Lead Temperature (soldering, 10s).....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to *Application Note 4083* at www.maxim-ic.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{OE}$ INPUT						
Input High Level	V_{IH1}		2.4			V
Input Low Level	V_{IL1}				0.5	V
Input Current	I_{IN-EN}	V_{IN} = 0 to V_{CC}		24		µA
DDC_EN INPUT						
Input High Level	V_{IH1}		2.4			V
Input Low Level	V_{IL1}				0.5	V
Input Current	I_{IN-DDC}	V_{IN} = 0 to V_{CC}		100		µA
HPD INPUT AND OUTPUT						
Input High Level	V_{IH2}		2.4		5.3	V
Input Low Level	V_{IL2}				0.8	V
Input Current	I_{IN2}	V_{IN} = 0 to V_{CC}		80		µA
HPD_SNK Pulldown Resistance	R_{HPD}		40	60		kΩ
Output High Level	$V_{OH-HPDB}$		2.5		V_{CC}	V
Output Low Level	$V_{OL-HPDB}$		0	0.18	0.4	V
DIFFERENTIAL INPUTS (IN_)						
Differential Input High Threshold	V_{IDH}	$V_{ID} = V_{IN+} - V_{IN-}$			50	mV
Differential Input Low Threshold	V_{IDL}	$V_{ID} = V_{IN+} - V_{IN-}$	-50			mV
Common Input Voltage	V_{COM}	V_{COD} = DC Avg [(V_{IN+} + V_{IN-}) / 2]	0	1.43	2	V
Common-Mode AC Tolerance	$V_{CM\_AC\_P-P}$	$V_{CM\_AC\_P-P} = (V_{IN+} + V_{IN-}) / 2 - V_{COD}$			100	mV
Differential Input Termination	R_{IN}		40		60	Ω

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL OUTPUTS (OUT_)						
Single-Ended Output Swing	V_{OSW}	With a 50Ω load to V_{CC} at both pins	450		600	mV
Single-Ended Output High	V_{OH3}	With a 50Ω load to V_{CC} at both pins	V_{CC} - 10mV		V_{CC} + 10mV	mV
Single-Ended Output Low	V_{OL3}	With a 50Ω load to V_{CC} at both pins	V_{CC} - 600mV		V_{CC} - 400mV	V
Single-Ended Output Current in High-Z	I_{OFF}		-10		+10	µA
Output Short-Circuit Current	I_{OS}	Output pins connected to V_{CC} or GND	-20		+20	mA
POWER CONSUMPTION						
Supply Current	I_{CC}	Includes 4 channels CML termination supply current, $\overline{OE}$ = 0		77	90	mA
	I_{PD}	$\overline{OE}$ = 1		5		

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3V to 3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL SIGNAL						
Maximum Data Rate	r_D		1.85			Gbps
Differential Propagation Delay	t_{PD}			350	500	ps
Channel-to-Channel Skew	t_{SK}			20	50	ps
Output Rise/Fall Time	$t_{R/F}$		180		515	ps
Added Random Jitter	t_{RJ}	1GHz clock input		0.5	1	ps_{RMS}
Added Deterministic Jitter	t_{DJ}	r_D = 2Gbps, 2^{23} - 1 PRBS pattern		11	30	ps_{P-P}
SINGLE-ENDED SIGNAL						
CLK Frequency	f_{SCK}	Supports I^2C fast mode			400	kHz
HPD_SRC Rise/Fall Time	$t_{RF-HPDB}$		1		20	ns
HPD Propagation Delay	t_{HPD}				200	ns

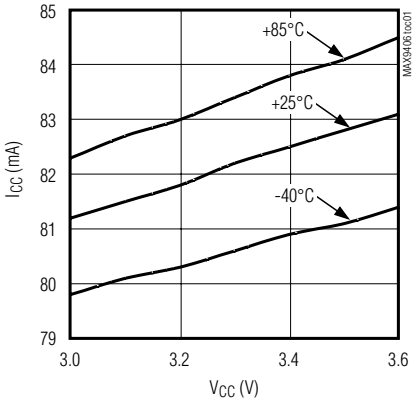
Note 2: AC parameters are guaranteed by design and characterization.

DisplayPort to DVI/HDMI Level Shifter

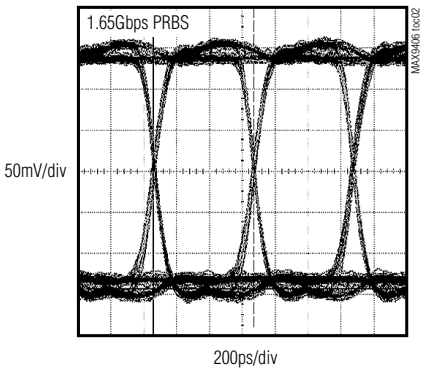
Typical Operating Characteristics

(V_{CC} = 3.3V, outputs terminated with 50Ω, T_A = +25°C, unless otherwise noted.)

SUPPLY CURRENT vs. SUPPLY VOLTAGE



EYE DIAGRAM

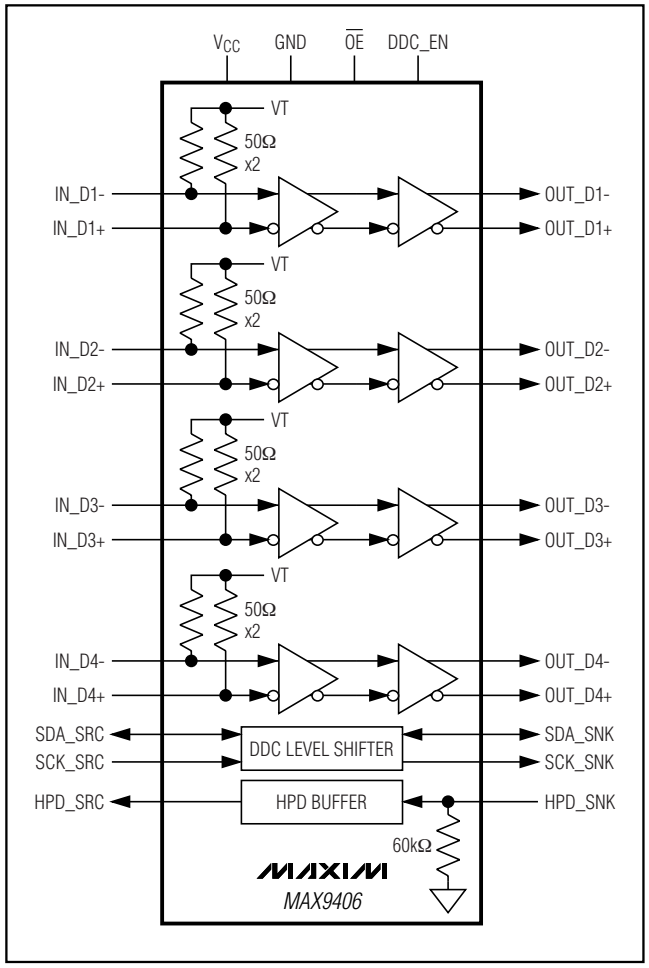


Pin Description

PIN		NAME	FUNCTION
32-PIN TQFN	48-PIN TQFN		
1, 3, 8, 18, 22	1, 5, 12, 18, 24, 27, 31, 36, 37,43	GND	Ground
2, 7, 24	2, 11, 15, 21, 26, 33, 40, 46	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with 0.1µF and 0.01µF capacitors as close to the supply pins as possible.
—	3, 4, 6, 10, 34, 35	N.C.	No Connection. Not internally connected; leave unconnected.
4	7	HPD_SRC	Hot-Plug Detection at 3.3V Logic
5	8	SDA_SRC	Serial Data Line. I^2C data line at 3.3V logic.
6	9	SCL_SRC	Serial Clock Line. I^2C clock line at 3.3V logic.
9	13	OUT_D4+	Differential Output Port 4+
10	14	OUT_D4-	Differential Output Port 4-
11	16	OUT_D3+	Differential Output Port 3+
12	17	OUT_D3-	Differential Output Port 3-
13	19	OUT_D2+	Differential Output Port 2+
14	20	OUT_D2-	Differential Output Port 2-
15	22	OUT_D1+	Differential Output Port 1+
16	23	OUT_D1-	Differential Output Port 1-
17	25	$\overline{OE}$	Output Enable. Drive $\overline{OE}$ low to enable the outputs. Drive $\overline{OE}$ high to disable the outputs.
19	28	SCL_SNK	Serial Data Line. I^2C data line at 5V logic.
20	29	SDA_SNK	Serial Clock Line. I^2C clock line at 5V logic.
21	30	HPD_SNK	Hot-Plug Detection at +5V Logic
23	32	DDC_EN	DDC Link Enable
25	38	IN_D1-	Differential Input Port 1-
26	39	IN_D1+	Differential Input Port 1+
27	41	IN_D2-	Differential Input Port 2-
28	42	IN_D2+	Differential Input Port 2+
29	44	IN_D3-	Differential Input Port 3-
30	45	IN_D3+	Differential Input Port 3+
31	47	IN_D4-	Differential Input Port 4-
32	48	IN_D4+	Differential Input Port 4+
—	—	EP	Exposed Paddle. Connect EP to ground.

DisplayPort to DVI/HDMI Level Shifter

Functional Diagram



Detailed Description

The MAX9406 high-speed, low-skew, quad differential input to CML translator is designed for high-speed signal conversion of the DP to HDMI technology. This device features ultra-low propagation delay of 350ps and channel-to-channel skew of less than 20ps. The MAX9406 supports typical data rates of 2Gbps.

The MAX9406 provides the level shift for HDMI's DDC and HPD, which converts the 5V single-ended logic to 3.3V single-ended logic.

High-Speed Signal Enables

$\overline{OE}$ controls the power through the entire length of the four high-speed signal paths. Setting $\overline{OE}$ low enables all of the high-speed signal paths. Setting $\overline{OE}$ high disables all high-speed links and disconnects the internal biasing supply and brings the device to the low-power state. In the low-power state, however, the DDC and HPD ports are still functioning.

Display Data Channel (DDC)

The MAX9406 allows the translation between 5V and 3V of the lower speed DDC lines. Whenever one side is pulled to GND, the other side follows and vice versa. DDC_EN controls the gating to the DDC link. Setting DDC_EN high enables data to pass through the DDC, while setting DDC_EN low disables the DDC link.

Hot-Plug Detection (HPD)

The MAX9406 translates the HPD 5V logic into 3V logic.

Applications Information

DVI/HDMI Driver

The MAX9406 can be used as the driver for the HDMI signal on the motherboard. The MAX9406 CML output provides a > 400mV differential HDMI output and supports 3.3V pullup at the differential outputs. The level shifter boosts the differential signal from the graphics chip to the HDMI connector, located on the edge of the motherboard.

High-Speed Signal Line Enable/Disable

The MAX9406 allows use of the DDC lines independent of the state of the high-speed signal lines and the $\overline{OE}$ pin. This allows communication through DDC without any high-speed signals.

Output Termination

Terminate CML outputs through 50Ω to V_{CC} or use an equivalent Thevinin termination. Terminate both outputs and use identical terminations on each for the lowest output-to-output skew.

Power-Supply Bypassing

Adequate power-supply bypassing is necessary to maximize the performance and noise immunity. Bypass V_{CC} to GND with high-frequency surface-mount 0.01µF ceramic capacitors as close to the device as possible. Use multiple bypass vias for connection to minimize inductance.

Printed-Circuit Board (PCB) Traces

Input and output trace characteristics affect the performance of the MAX9406. Connect each of the inputs and outputs to a 50Ω characteristic impedance trace. Avoid discontinuities in differential impedance and maximize common-mode noise immunity by maintaining the distance between differential traces, avoiding sharp corners. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Minimize skew by matching the electrical length of the traces.

Exposed Paddle

The thin QFN packages used for the MAX9406 have exposed paddles on the bottom. Connect the exposed paddle to ground using a landing pad large enough to accommodate the entire exposed paddle. Add vias from the exposed paddle's land area to a copper polygon on the other side of the PCB to provide lower thermal impedance from the MAX9406 to the ambient air.

Chip Information

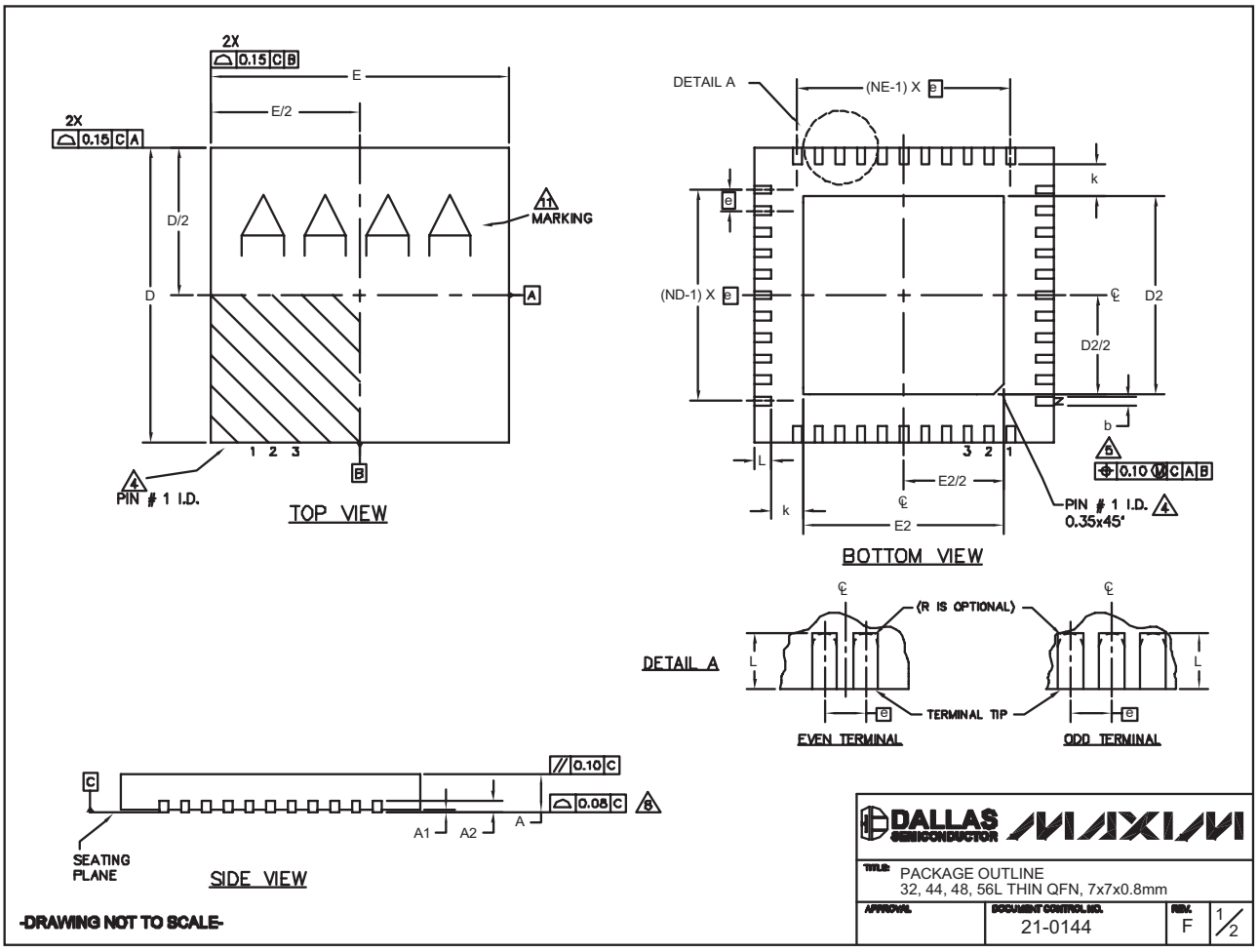
PROCESS: BiPolar

DisplayPort to DVI/HDMI Level Shifter

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

32, 44, 48L QFN.EPS



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG	32L 7x7			44L 7x7			48L 7x7			CUSTOM PKG. (T4877-1) 48L 7x7			56L 7x7		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
E	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10	6.90	7.00	7.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.45	0.55	0.65	0.30	0.40	0.50
N	32			44			48			44			56		
ND	8			11			12			10			14		
NE	8			11			12			12			14		

EXPOSED PAD VARIATIONS								
PKG. CODES	DEPOPULATED LEADS	D2			E2			JEDEC MO220 REV. C
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3277-2	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T3277-3	–	4.55	4.70	4.85	4.55	4.70	4.85	–
T4477-2	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4477-3	–	4.55	4.70	4.85	4.55	4.70	4.85	WKKD-1
T4877-1**	13,24,37,48	4.20	4.30	4.40	4.20	4.30	4.40	–
T4877-3	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877-4	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-5	–	2.40	2.50	2.60	2.40	2.50	2.60	–
T4877-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877-7	–	4.95	5.10	5.25	4.95	5.10	5.25	–
T4877M-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877M-6	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T4877MN-8	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-1	–	5.40	5.50	5.60	5.40	5.50	5.60	–
T5677-2	–	5.40	5.50	5.60	5.40	5.50	5.60	–

** NOTE: T4877-1 IS A CUSTOM 48L PKG. WITH 4 LEADS DEPOPULATED. TOTAL NUMBER OF LEADS ARE 44.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 EXCEPT THE EXPOSED PAD DIMENSIONS OF T4877-1/-3/-4/-5/-6 & T5677-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
32, 44, 48, 56L THIN QFN, 7x7x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0144	F	2/2

DisplayPort to DVI/HDMI Level Shifter

Package Information (continued)

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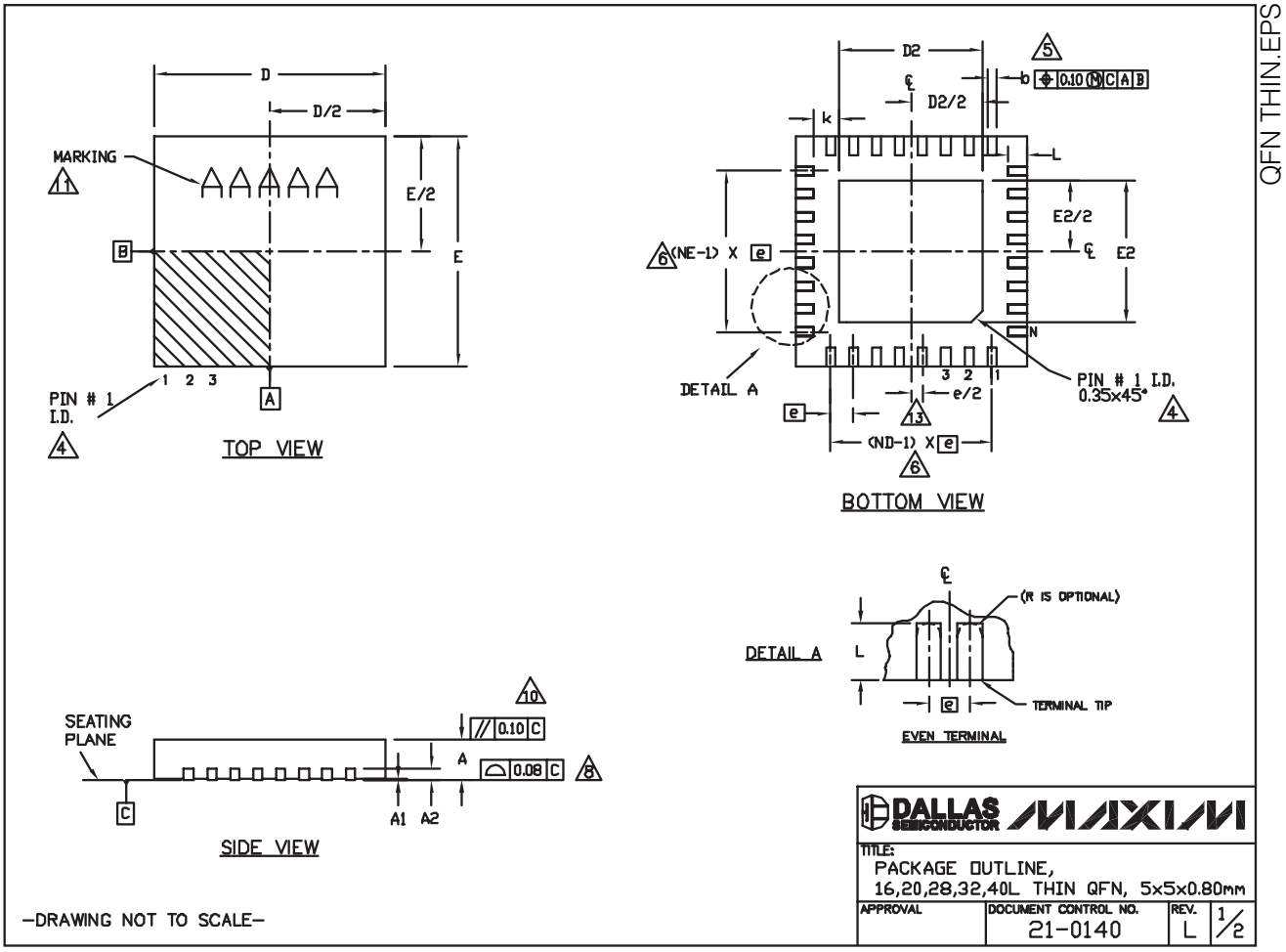

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

—DRAWING NOT TO SCALE—

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.80mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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