TOSHIBA BiCMOS Integrated Circuit Silicon Monolithic

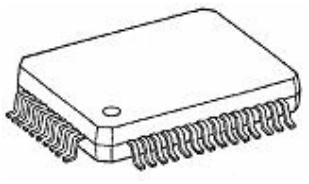
TB1305FG,TB1308FG

Component SW, Sync Separation and H/V Frequency Counter IC for TVs

The TB1305FG and TB1308FG include a component SW block, a prefilter for AD conversion, sync separation and H/V format detectors for TV component video signals.

The TB1305FG and TB1308FG contribute to reduction in the proportion of PCB occupied by LCR filters and to the simplification of designs on analog interfaces.

The TB1305FG and TB1308FG are equipped with an I^2CBUS interface through which various functions can be controlled.



P-QFP48-1014-0.80

Weight: 0.83 g (typ.)

Features

COMPONENT BLOCK

- Component video input: TB1305FG 2 channels, TB1308FG 3 channels; RGB available
- Component video output
- Gain switching: 0dB / +6dB
- Bandwidth filter: prefilter for ADC; 4.2 to 31MHz variable)

SYNC SEPARATION BLOCK

- Supports 525/60i/60p, 625/50i/50p, 750/50p/60p, 1125/50i/60i/50p/60p, 1250/50i, VGA@60, SVGA@60, XGA@60, SXGA@60, UXGA@60
- HD/VD input: 2 channels; positive and negative input acceptable
- HD/VD output: positive and negative output selectable
- Masking pseudo-sync for copyguard signal

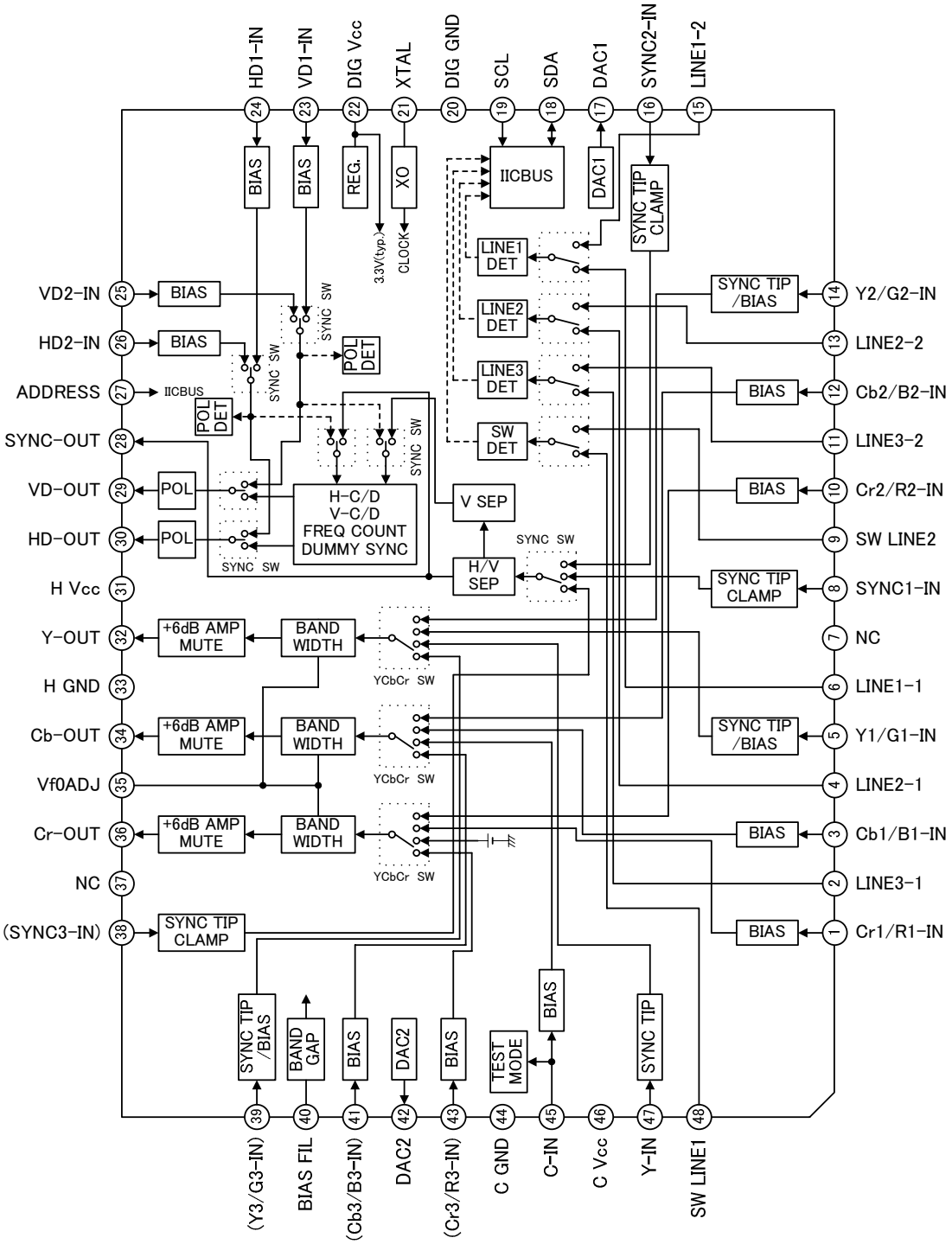
OTHERS

- Line detector for D-pin (2 channels)
- Horizontal and vertical frequency counter
- Format detection circuit for input signal
- Automatic sync process switching mode

Lineup

Part No.	Number of component video inputs
TB1305FG	2
TB1308FG	3

Block Diagram



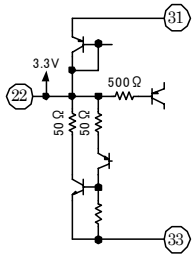
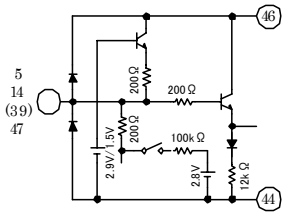
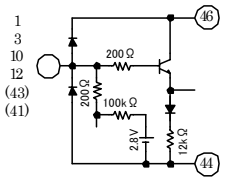
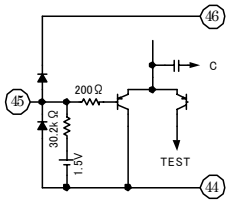
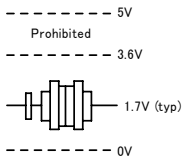
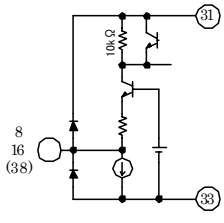
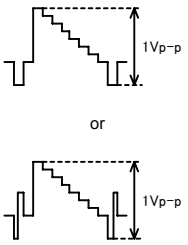
NOTE: Pins 38, 39, 41 and 43 are available for the TB1308FG only. The pins are NC for the TB1305FG.

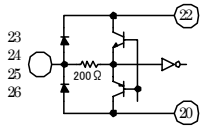
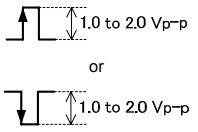
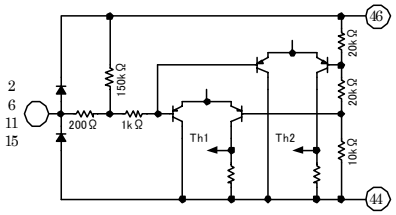
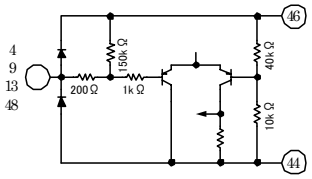
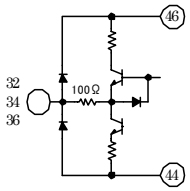
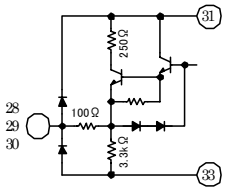
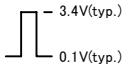
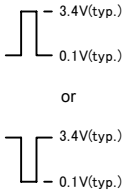
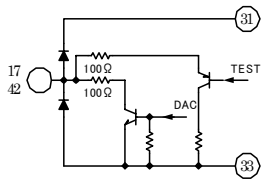
The TB1305FG and TB1308FG do not support weak signals, ghost signals or other non-standard signals.

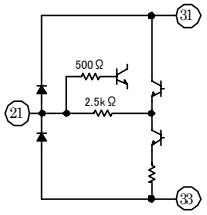
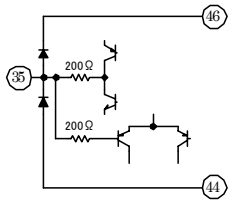
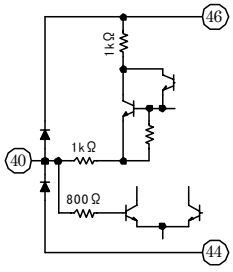
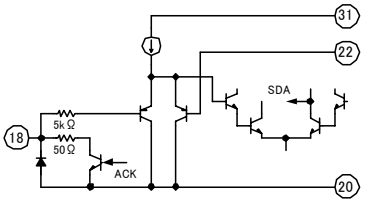
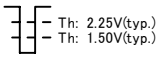
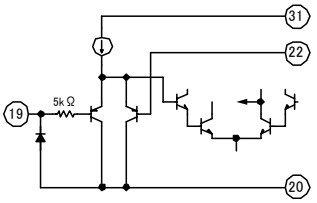
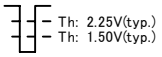
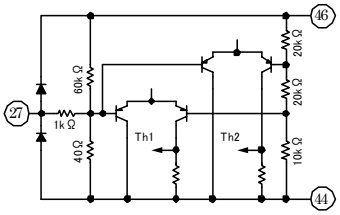
Some functional blocks, circuits or constants may be omitted or simplified in the block diagram for explanatory purposes.

Pin Functions

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
22	DIG V_{CC}	V_{CC} pin for the logical circuits. Supply power through a resistor from pin 31 like the Application Circuit. This pin voltage is clipped to 3.3 V (typ.) by the internal regulator.		3.3 V (typ.)
20	DIG GND	GND pin for the logical circuits.	—	—
31	H V_{CC}	V_{CC} pin for the sync circuits. Connect 5.0 V (typ.)	—	5.0 V (typ.)
33	H GND	GND pin for the sync circuits.	—	—
46	C V_{CC}	V_{CC} pin for the video circuits. Connect 5.0 V (typ.)	—	5.0 V (typ.)
44	C GND	GND pin for the video circuits.	—	—
5 14 39	Y1/G1-IN Y2/G2-IN Y3/G3-IN	Y or G input pin. Input the signal via a clamp capacitor. The clamp system is selectable by CLAMP register. NOTE: Pin 39 is not available for the TB1305FG. It is an NC pin.		Sync tip level: 2.1 V (typ.) Bias level: 2.7 V (typ.) RGB/YCbCr/YPbPr signal amplitude: 0.7 Vp-p (without sync)
47	Y-IN	Y or CVBS input pin. Input the Y or CVBS signal in NTSC, PAL or SECAM from an AV-SW via a clamp capacitor. The clamp system is selectable by CLAMP register.		Sync tip level: 2.1 V (typ.) Bias level: 2.7 V (typ.) Y/CVBS signal's amplitude: 1.0 Vp-p (with sync)
1 3 10 12 43 41	Cr1/R1-IN Cb1/B1-IN Cr2/R2-IN Cb2/B2-IN Cr3/R3-IN Cb3/B3-IN	Cb/Cr, Pb/Pr or B/R input pin. Input the signal via a capacitor. NOTE: Pins 41 and 43 are not available for the TB1305FG. They are NC pins.		2.7 V bias (typ.) RGB/YCbCr/YPbPr signal amplitude: 0.7 Vp-p (without sync)
45	C-IN	Chroma signal input pin. Input C signal from AV-SW via a capacitor. When this pin's voltage is High, TEST mode for shipping is active. The pin voltage must be less than 3.6 V during operating.		1.7 V bias (typ.) 
8 16 38	SYNC1-IN SYNC2-IN SYNC3-IN	Composite SYNC input pin to separate into H- and V-SYNC. Input the signal via a resister and a clamp capacitor. NOTE: Pin 38 is not available for the TB1305FG. It is an NC pin.		Sync tip level: 1.75 V (typ.) 

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
24 26	HD1-IN HD2-IN	HD input pin. Input a separated horizontal sync signal (1.0 to 2.0 Vp-p) via a resister and a coupling capacitor. The polarity of the input signal is detected and its leading edge becomes a timing trigger.		1.45 V bias (typ.) 
23 25	VD1-IN VD2-IN	VD input pin. Input a separated vertical sync signal (1.0 to 2.0 Vp-p) via a resister and a coupling capacitor. The polarity of the input signal is detected and its leading edge becomes a timing trigger.		
6 15	LINE1-1 LINE1-2	LINE1 (number of lines) detection pin. Connect LINE1 of D-pin.		DC
2 11	LINE3-1 LINE3-2	LINE3 (aspect ratio) detection pin. Connect LINE3 of D-pin.		DC
4 13	LINE2-1 LINE2-2	LINE2 (i/p) detection pin. Connect LINE2 of D-pin.		DC
48 9	SW LINE1 SW LINE2	SW LINE detection pin. Connect SW LINE of D-pin.		DC
32	Y-OUT	Y, G or CVBS signal output pin.		AC: 0 dB or +6 dB (typ.)
34	Cb-OUT	Cb, Pb, B or C signal output pin.		
36	Cr-OUT	Cr, Pr or R signal output pin.		
28	SYNC-OUT	Separated composite sync output pin.		
29 30	VD-OUT HD-OUT	HD or VD output pin. The polarity of the output is selectable by HV-POL register. The tailing edge of the VD-OUT has a jitter. Use the leading edge only.		
17 42	DAC1 DAC2	1-bit DAC output pin. Open-collector pin.		DC

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
21	XTAL	Crystal connection pin. Connect a 3.579545 MHz crystal for NTSC demodulation to generate internal clocks.		—
35	Vf0ADJ	A filter pin to adjust bandwidth filter characteristics.		—
40	BIAS FIL	A filter pin for internal bias circuits.		—
18	SDA	SDA pin for I^2CBUS.		 H to L: 1.50 V (typ.) L to H: 2.25 V (typ.)
19	SCL	SCL pin for I^2CBUS.		 H to L: 1.50 V (typ.) L to H: 2.25 V (typ.)
27	ADDRESS	Slave address switching pin. Connect to 5 V Vcc or GND. Or leave this pin open.		5 V Vcc: DC_H/DD_H Open: DA_H/DB_H GND: $D8_H/D9_H$
7 37	NC	These pins are not used. Connect to GND. NOTE: Pins 38, 39, 41 and 43 of the TB1305FG are not used . Connect them to GND.	—	—

BUS Control Map

Write Mode Slave address: $D8_H$ / DA_H / DC_H

SA	D7	D6	D5	D4	D3	D2	D1	D0	PRESET
00	MUTE	FILPASS	HD WIDTH	DAC2	DAC1	YCbCr SW		GAIN	00000000
01	f0 SW	BANDWIDTH							00000000
02	fc HALF	SYNC SW			HV FREQ				00000000
03	HV-SEP	VGA-SEP	1(PS MASK)	A SYNC	S MODE	CLAMP	HV-POL	VD PHS	00000000

NOTE: Set PS MASK = 1 (ON) for except “Sync on G” input.
Remark: SA = Sub-Address.

Read Mode Slave address: $D9_H$ / DB_H / DD_H

	D7	D6	D5	D4	D3	D2	D1	D0
0	LINE1		LINE2	LINE3		SW LINE1	SW LINE2	*
1	HD-POL	VD-POL	H FORMAT				V FORMAT	
2	H FM2	V FM2	H IN	V IN	V-SYNC-W	*	VERSION	
3	*	V FREQ DET						
4	H FREQ DET							

*: Undefined

Bus Control Functions

Write Mode

Register Name	Function	Preset Value
MUTE	Swtches mute mode. 0: NORMAL 1: Video mute	NORMAL (0)
FILPASS	Switches the bandwidth limit filter. 0: ON (by-pass) 1: OFF	ON (0)
HD WIDTH	Switches the width of HD-OUT. 0: WIDE 1: NARROW Remark: HD WIDTH = 1 (NARROW) is recommended for the 1125/50p/60p format owing to crosstalk from HD-OUT to video signals so that spike noises on video signals will occur.	WIDE (0)
DAC1,2	1-bit DAC switching Output voltages of DAC1 (pin 17) and DAC2 (pin 42) are controlled. DAC1/2 are open-collector pins. 0: LOW (ON) 1: HIGH (OPEN)	LOW (0)
YCbCr SW	Switches the component video input and line input 00: Y1 / Cb1 / Cr1 / LINE1, 2, 3-1 (pins 1, 2, 3, 4, 5, 6) 01: Y2 / Cb2 / Cr2 / LINE1, 2, 3-2 (pins 10, 11, 12, 13, 14, 15) 10: Y / C (pins 45, 47. Cr-out is muted.) 11: Y3 / Cb3 / Cr3 (pins 39, 41, 43) NOTE: The data (11) is not available for the TB1305FG.	Y1 / Cb1 / Cr1 (00)
GAIN	Switches the output gain. Gain of YCbCr output (pins 32, 34, 36) is controlled. 0: 0 dB 1: +6 dB Remark: GAIN = 0 (0 dB) is recommended for the 1125/50p/60p format since this offers superior frequency characteristics to those of +6 dB mode.	0 dB (0)
f0 SW	Switches the f0 of bandwidth limit filter 0: HIGH 1: LOW	HIGH (0)
BANDWIDTH	Switches the f0 of bandwidth limit filter 0000000: MIN (low) 1111111: MAX (high)	MIN (0000000)
fc HALF	Switches the frequency of bandwidth limit filters for Cb/Cr The cutoff frequency of bandwidth limit filters for Cb/Cr is 1/2 to Y. 0: OFF (same for 3 outputs) 1: ON (1/2 fc for Cb/Cr)	OFF (0)

<table>
<tr><th>Register Name</th><th>Function</th><th>Preset Value</th></tr>
<tr><td>SYNC SW</td><td>Switches sync input.
Sync input to HD/VD-OUT and to SYNC-OUT is selected.
<table>
<tr><th></th><th>HD OUT (pin 30)</th><th>VD OUT (pin 29)</th><th>SYNC OUT (pin 28)</th></tr>
<tr><td>000</td><td colspan="3">SYNC1 (pin 8)</td></tr>
<tr><td>001</td><td colspan="3">SYNC2 (pin 16)</td></tr>
<tr><td>010</td><td colspan="3">SYNC3 (pin 38: TB1308FG only)</td></tr>
<tr><td>011</td><td colspan="3">Not available</td></tr>
<tr><td>100</td><td>HD1 (pin 24)</td><td>VD1 (pin 23)</td><td>SYNC1 (pin 8)</td></tr>
<tr><td>101</td><td>HD2 (pin 26)</td><td>VD2 (pin 25)</td><td>SYNC2 (pin 16)</td></tr>
<tr><td>110</td><td>HD1 (pin 24)</td><td>VD1 (pin 23)</td><td>SYNC3
(pin 38 : TB1308FG only)</td></tr>
<tr><td>111</td><td>HD2 (pin 26)</td><td>VD2 (pin 25)</td><td>SYNC3
(pin 38: TB1308FG only)</td></tr>
</table>
NOTE: SYNC3 of the data 010, 110, 111 is not available for the TB1305FG.</td><td>SYNC1
(000)</td></tr>
<tr><td>HV FREQ</td><td>Input format setting
Set the horizontal and vertical mode according to the format that is input.
0000: 15.625 kHz, 50 Hz (625i) 0001: 15.75 kHz, 60 Hz (525i)
0010: 31.25 kHz, 50 Hz (625p) 0011: 31.5 kHz, 60 Hz (525p, VGA@60Hz)
0100: 28.125 kHz, 50 Hz (1125/50i)0101: 33.75 kHz, 60 Hz (1125/60i)
0110: 37.5 kHz, 50 Hz (750/50p) 0111: 45 kHz, 60 Hz (750/60p, XGA@60Hz)
1000: 31.25 kHz, 50 Hz (1250i)
1001: 37.9 kHz, 60 Hz (SVGA@60Hz)
1010: 64 kHz, 60 Hz (1125/60p, SXGA@60Hz)
1011: 75 kHz, 60 Hz (UXGA@60Hz)
1100: 56.25 kHz, 50 Hz (1125/50p)
1101 ~ 1111: Not available</td><td>15.625 kHz, 50 Hz
(0000)</td></tr>
<tr><td>HV-SEP</td><td>Switches the separation level.
The H/V sync separation level to SYNC-IN (pins 8, 16, 38) is switched.
0: LOW 1: HIGH
Remark: The separation level is changed according to the ratio of negative sync width per H period and the connected resistance.</td><td>LOW
(0)</td></tr>
<tr><td>VGA-SEP</td><td>Switches the separation level.
The H/V sync separation level to SYNC-IN (pins 8, 16, 38) is switched for PC signals.
0: Normal (component video) 1: VGA
Remark: The separation level is changed according to the ratio of negative sync width per H period and the connected resistance.</td><td>Normal
(0)</td></tr>
<tr><td>PS MASK</td><td>Switches the mask mode for pseudo-sync.
Pseudo-syncs in lines are removed.
0: OFF (V-BLK period only) 1: ON (all lines)
NOTE: Set PS MASK = 1 (ON) for except “Sync on G”.</td><td>OFF
(0)</td></tr>
</table>

Register Name	Function	Preset Value
A-SYNC	Automatic sync processing mode. Sync processing mode is changed in accordance with the results obtained by the internal format detection circuits. Format detection is performed for a SYNC or HD/VD signal selected by SYNC SW. The result of detection is returned to H, V FORMAT and H, V FM2. The HV FREQ setting is invalid when this mode is active. 0: OFF (manual switching mode by HV FREQ setting) 1: ON	OFF (0)
S MODE	Switches sync output mode. This function sets the dummy HD/VD output mode when there is no input. The frequency of the dummy HD/VD output depends on the HV FREQ setting (when A-SYNC = OFF) or H, V FORMAT (when A-SYNC = ON). H, V IN shows whether there is no input or not. 0: OFF (No HD and free-run VD output (approx. 44 Hz), when there is no input. However, in 1250i mode, no HD and no VD output, when there is no input.) 1: ON (Dummy HD/VD output when there is no input)	OFF (00)
CLAMP	Switches Y clamping mode. This function sets the clamping mode for pins 5, 14, 39. 0: SYNC TIP CLAMP 1: BIAS	SYNC TIP (0)
HV-POL	Switches the polarity of the HD/VD output. This function sets the polarity of HD/VD OUT (pins 29, 30). 0: Positive 1: Negative	Positive (0)
VD PHS	Switches the phase of dummy VD output. VD PHS compensates for delay time so that the dummy VD-OUT phase is the same as that form the separated V-sync. 0: No delay 1: 0.2 H delay (0.15 H delay for 1125/50p)	No-delay (0)

Read Mode

Register Name	Function
LINE1	LINE1 detection for D-pin (for the number of lines) 00: 525 (480) 01: 750 (720) 10: ---- 11: 1125 (1080) Detects the voltage of LINE1 selected by YCbCr SW. 11 is returned when the pin is not connected.
LINE2	LINE2 detection for D-pin (for i/p) 0: Interlace 1: Progressive Detects the voltage of LINE2 selected by YCbCr SW. 1 is returned when the pin is not connected.
LINE3	LINE3 detection for D-pin (for aspect ratio) 00: 4:3 01: 4:3 letter box 10: ---- 11: 16:9 Detects the voltage of LINE3 selected by YCbCr SW. 11 is returned when the pin is not connected.
SW LINE1	SW LINE1 (pin 48) detection for D-pin 0: Connected 1: Not connected
SW LINE2	SW LINE1 (pin 9) detection for D-pin 0: Connected 1: Not connected
HD-POL	Polarity detection to HD-IN 0: Positive 1: Negative Detects the width from the HD-IN pin to determine whether it is negative or not. When the High level of the input HD-IN is wider than approx 14 μs, HD-POL shows 1.

Register Name	Function
VD-POL	Polarity detection to VD-IN 0: Positive 1: Negative Detects the width from the VD-IN pin to determine whether it is negative or not. When the High level of the input VD-IN is wider than approx 4.5 ms, VD-POL shows 1.
H FORMAT	Horizontal format detection 0000: 15.625/15.75kHz 0001: 28.125kHz 0010: 31.25/31.5kHz 0011: 33.75kHz 0100: 37.5/37.9kHz 0101: 45/48kHz 0110: 64kHz/67.5kHz 0111: 75kHz 1000 56.25kHz 1001 ~ 1111: Undefined Detects a horizontal format (horizontal frequency). NOTE1: Format detection errors such as the following can occur when suppressed syncs are input. See NOTE3 in the function description on Automatic sync processing mode, too. 525i input → 525p detected, 625i input → 625p detected, 1125i input → 1125p detected 525p/625p input → No V-sync detected NOTE2: When 525i, 625i, 1125/50i or 1125/60i signal is input, H FORMAT data can be incorrect caused by the pseudo-syncs for copy guard or the equalizing pulses.
V FORMAT	Vertical format detection 00: 50 Hz 01: 60 Hz 10 ~ 11: Undefined Detects a vertical format (horizontal frequency) according to V FREQ DET data.
H FM2	Horizontal format detection 2 0: Known 1: Unknown Detects whether an input is in one of the defined formats or not. This is based on H FORMAT data. NOTE: H FM2 may indicate Unknown, when 525p input with pseudo sync signal for copy guard is input.
V FM2	Vertical format detection 2 0: Known 1: Unknown Detects whether an input is in one of the defined formats or not. This is based on V FORMAT data.
H IN	Input detection to horizontal syncs 0: No signal 1: Signal
V IN	Input detection to vertical syncs 0: No signal 1: Signal
V-SYNC-W	V-SYNC width detection 0: Wide 1: Narrow Detects V-SYNC width for detecting 1250i format. Under A-SYNC = 1 (ON), V-SYNC-W shows 1, when the VD width from the VD-IN pin is narrower than approx 69 μs, or when the V-SYNC width from the SYNC-IN pin is narrower than approx 27 μs.
VERSION	IC version identification 00: TB1305FG 01: TB1308FG 10: ---- 11: ----
V FREQ DET	Counts the vertical frequency of an input selected by SYNC SW. 0000000: Over 3.5kHz 1001111: 44Hz or less 1010000～1111111: No signal How to calculate a vertical frequency (Y): Convert data read from V FREQ DET into decimal value and call it X. $\underline{\text{Vertical frequency (Y)}} = 1 \div (X \times 2.8607 \times 10^{-4})$ [Hz] The error range of X is −1 to +1.
H FREQ DET	Counts the horizontal frequency of an input selected by SYNC SW. 00000000: No signal 11111111: Over 85kHz How to calculate a horizontal frequency (Y): Convert data read from H FREQ DET into decimal value and call it X. $\underline{\text{Horizontal frequency (Y)}} = 1 \div (0.003 \div X)$ [Hz] The error range of X is −1 to +1.

Note 1: In determining the decision algorithms (detection range, detection times and so on) for H/V frequency detection, it is necessary to take into account both previously mentioned cautions and other factors such as signal conditions and I^2CBUS data transmission in the course of prototype TV set evaluation.

Note 2: The READ BUS flags indicate that a certain signal is detected at a given moment. However, the detection result will not be very reliable if only one flag is checked. To obtain accuracy, it is recommended that a judgment will be made on the basis of confirming several times and verifying agreement among the majority of flags read in a sequence and/or at the same time.

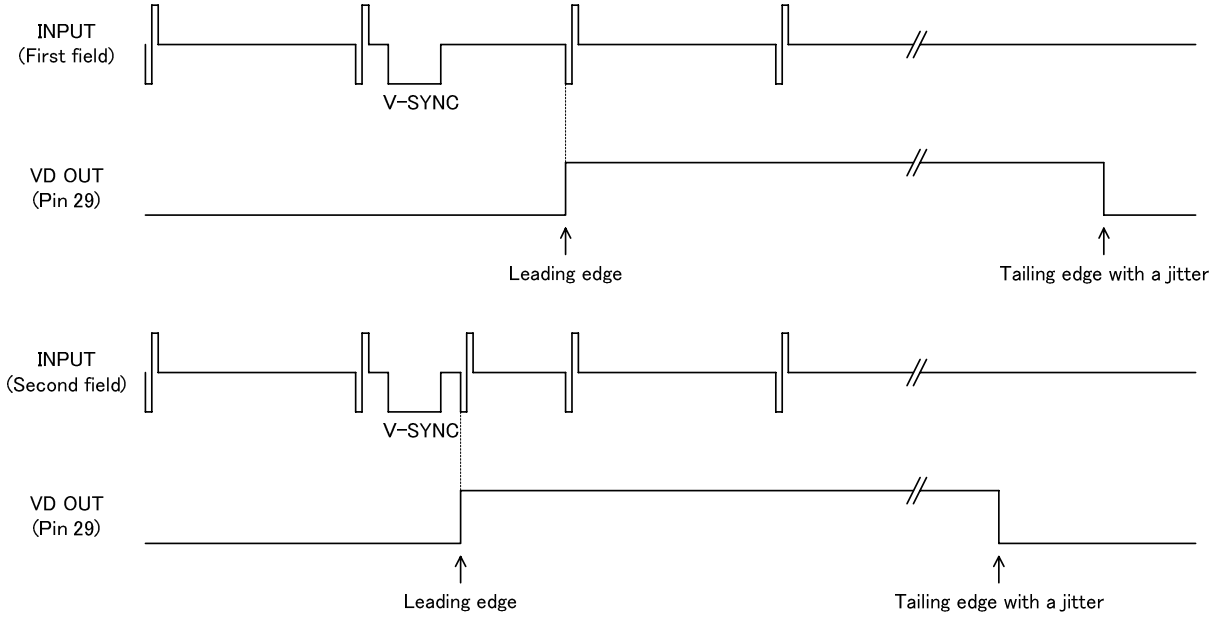
Function Descriptions

Vertical sync separation for 1250i/50

When HV FREQ = 1000, the vertical sync separation for 1250i/50 is accomplished through the use of a special circuit. The phase of the VD-out (pin 29) depends on the H-SYNC timing shown in the figure below. There is no VD-out when there is no H-SYNC input.

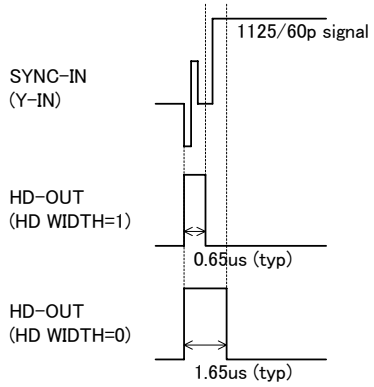
In the manual sync processing mode (A-SYNC = OFF), use READ BUS functions, V-SYNC-W and H, V FORMAT (or H, V FREQ DET) to detect 1250i/50.

NOTE: The VD-OUT's tailing edge has a jitter. Use the leading edge only.



HD width

HD-OUT width is selectable by HD WIDTH, as below. HD WIDTH = 1 (NARROW) is recommended for the 1125/50p/60p format owing to crosstalk from HD-OUT to video signals so that spike noises on video signals will occur.



Automatic sync processing mode (A-SYNC)

Counted horizontal and vertical frequency data to input signal are returned to READ BUS functions, H, V FREQ DET. Also, the detected format is returned to H, V FORMAT and H, FM2 when the H/V frequencies are in internal defined ranges. Input detection results, which indicate whether there is an input or not, for H, V-SYNC or HD, VD are returned to H, V IN. In automatic sync processing mode (when A-SYNC = ON), the TB1305FG and TB1308FG operate as indicated in the following table according to these READ data.

INPUT CONDITION	H, V FORMAT status	H, V FM2 status	H, V IN status	HD, VD outputs
Standard format	The format as input	Known	Signal	The separated sync as input
Non-standard format	The status indicates not the current condition but the last detected format.	Unknown	Signal	The separated sync as input
No input	The status indicates not the current condition but the last detected format.	Known: The status indicates not the current condition but the last detected format.	No signal	Dummy HD and VD, of which the frequency depends on the H, V FORMAT status

NOTE 3: The following format detection errors can occur when suppressed syncs are input.

525i input → 525p detected, 625i input→ 625p detected, 1125i input→ 1125p detected

525p/625p inputs → In case of the 525p/625p sync amplitude become bigger from zero to its standard gradually, V-sync of the input is not detected even though the sync amplitude is got back to its standard amplitude.

The V-sync separation performance to the suppressed sync input may be improved when VGA-SEP is set to 1 (VGA), though the H and V separation level are also changed.

NOTE 4: We recommend recognizing a format by H/V FREQ DET rather than one by H/V FORMAT because H FORMAT and H FM2 can indicate an incorrect data for 525i, 625i, 525p, 1125/50i and 1125/60i caused by the pseudo-syncs for copy guard or the equalizing pulses.

NOTE 5: Dummy HD and VD may become unstable while the mode is changing from one format to another.

By the way, in A-SYNC = OFF and S-MODE = ON mode, dummy HD and VD are output according to HV FREQ setting when there is no input.

Manual sync processing mode (A-SYNC = OFF *NOTE6)

HV FREQ = 625p is required to separate H-SYNC and V-SYNC properly. Set HV FREQ = 625p to count H/V-SYNC for Manual sync processing mode.

The following is an example of how to detect H/V frequency when A-SYNC=OFF.

1. Set HV FREQ = 625p(0010) and read data such as H, V FREQ DET.
2. Detect the H/V frequencies by microprocessor or similar means, depending on the data obtained.
3. Set HV FREQ and so on to the detected mode.
4. Continue to monitor the obtained data such as H, V FREQ DET. When any alteration is recognized, set HV FREQ = 625p(0010) and detect again.

Decision algorithms (for detection range, detection times and so on) for H/V frequency detection should be determined taking into account the above-mentioned errors in measuring H/V frequencies and the other factors such as signal conditions and I^2CBUS data transmission in the course of prototype TV set evaluation.

NOTE 6: We recommend recognizing formats for 525i and 625i signals by another device such as a color-decoder, not by this product, because 525i and 625i signals include non-standard signals.

However, if you use this product to recognize formats including the standard 525i and 625i, set “A-SYNC = ON”. Otherwise, H/V FREQ DET and H/V FORMAT may indicate incorrect value and VD-OUT may lock irregularly for 525i and 625i signals. Refer to the “Application circuit 3 (system configuration)”, too.

Sync separation level

The sync separation level is changed according to the ratio of H-sync width to one line and the connected resistance. Typical sync separation levels for each format are as follows. Then, VGA-SEP=1 for VGA to UXGA.

Format	HV-SEP = 0 (LOW)			HV-SEP = 1 (HIGH)		
	R = 1.2 kΩ	R = 1.5 kΩ	R = 1.8 kΩ	R = 1.2 kΩ	R = 1.5 kΩ	R = 1.8 kΩ
625/50i	22	28	33	24	32	37
525/60i	22	28	34	24	31	37
625/50p	22	28	34	25	31	38
525/60p	21	27	32	24	30	36
1125/50i	31	39	45	40	49	54
1125/60i	26	33	39	34	43	50
750/50p	29	37	43	37	46	52
750/60p	24	31	37	32	40	47
1250/50i	25	32	37	32	41	47
1125/50p	36	45	51	45	54	58
1125/60p	31	39	45	39	49	55
VGA/60	15	19	23	16	21	25
SVGA/60	15	18	22	16	20	24
XGA/60	17	22	26	19	24	28
SXGA/60	27	33	39	30	37	43

Unit [%] ; where 286 mVp-p sync for 525/60i and 300 mVp-p sync for others

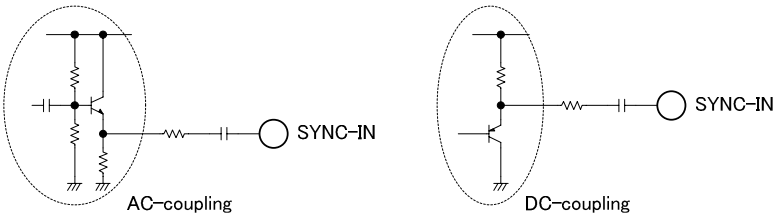
For “Sync on G” signal, HD-OUT is not output during V-sync period because there is no H-sync during V-sync period. Furthermore, for Sync on G of XGA input, HD-OUT disappears during active video period caused by unexpected lock of the internal V-BLK.

The format detection and sync separation performances are changed due to the separation level set by HV-SEP, VGA-SEP setting and/or the connected resistance with SYNC-IN pin. The careful evaluations are required to set the separation level under consideration of expected input conditions such as a suppressed sync input, an input with V-sag and APL (Average Picture Level) fluctuations.

Note on Sync input pin

If the AC-coupling circuit is put before the SYNC-IN pin, the picture on the screen may be not stable. This is because the sync separation circuit is unable to follow the DC level fluctuation caused by APL (Average Picture Level) change in the input signal, and the HD and/or VD output is unable to synchronize the input.

It is recommended to input signals via the DC-coupling buffer if necessary.



For the DC level fluctuation caused by APL change, the sync separation ability may be improved to change the setting of HV-SEP, VGA-SEP and/or changing the resister R. Furthermore, adding a high-resistance around several MΩ between SYNC-IN pin and GND (or Vcc) may improve the sync separation ability.

Adding DC restoration circuit such as a clamp circuit can be also effective for the improvement of DC level fluctuation. Also, refer to Sync separation level descriptions.

Prefilter for AD converter

The filter of the TB1305FG and TB1308FG can be used as a prefilter for AD converter. The cutoff frequency is controllable by I2CBUS functions, FILPASS, f0-SW, BANDWIDTH and fc HALF.

The characteristics for cutoff frequency and delay time are as below.

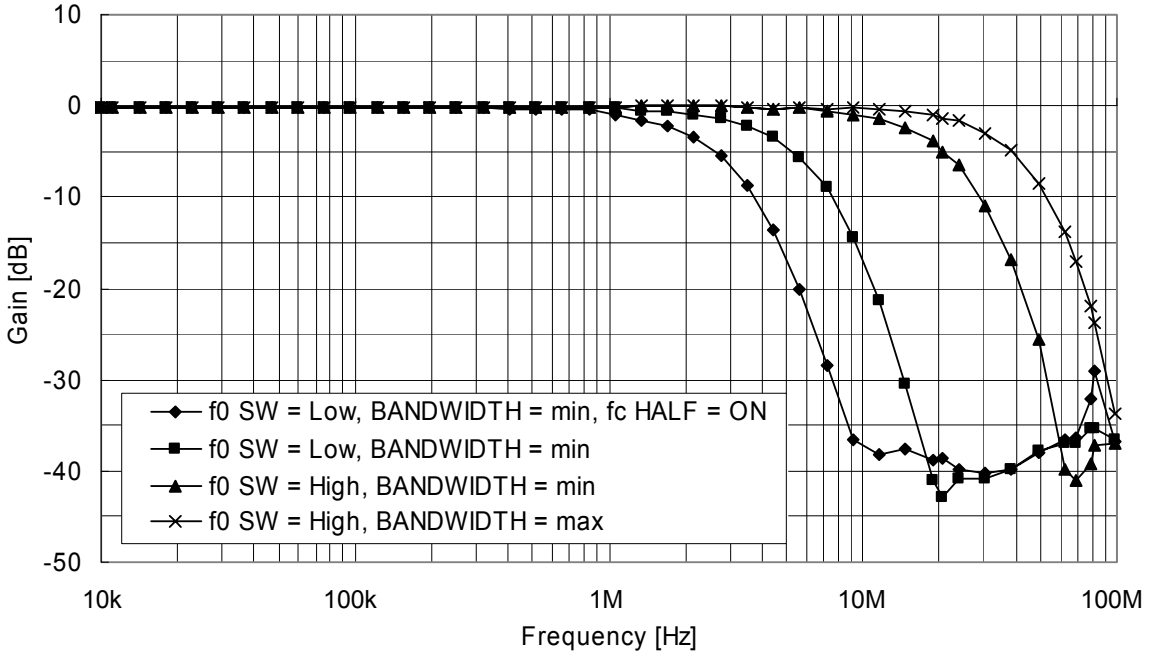


Figure. Typical prefilter frequency characteristics

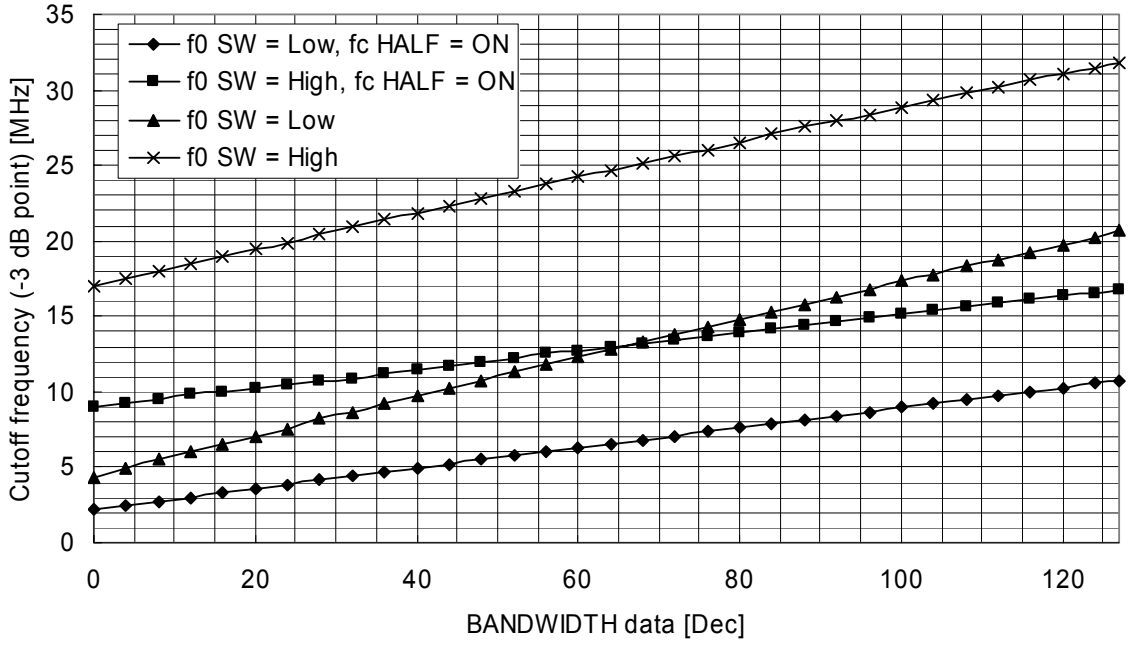


Figure. Typical cutoff frequency (-3 dB point) characteristics of prefilter due to BANDWIDTH data.

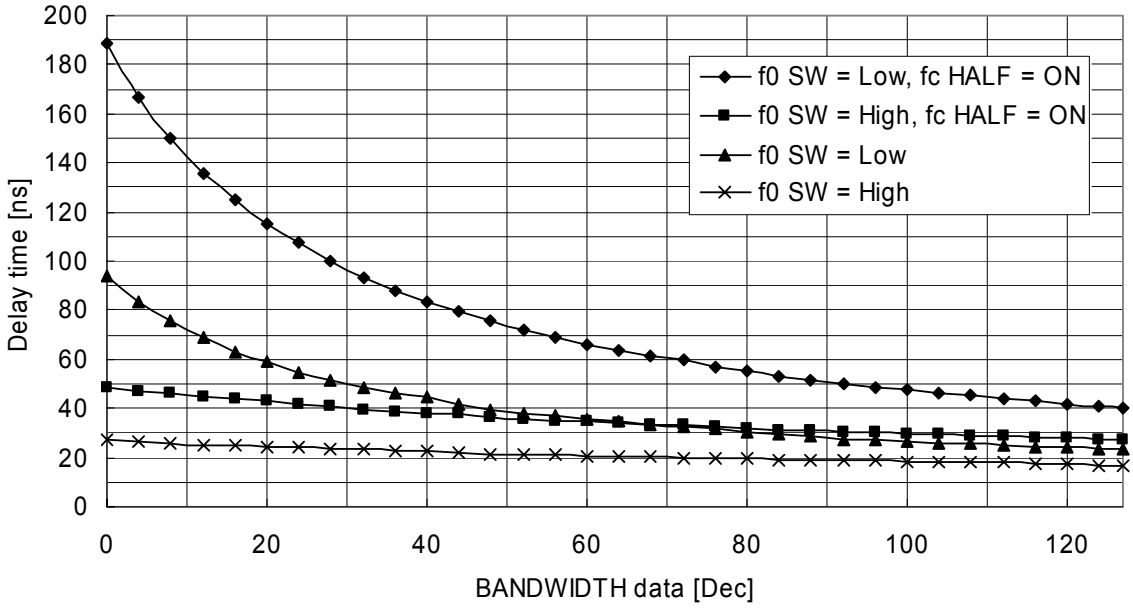


Figure. Typical delay-time (group delay @ 1MHz) characteristics of prefilter due to BANDWIDTH data.

Note on 1125/50p/60p input

When 1125/50p and/or 60p signal are input, GAIN = 0(0dB) and FILPASS = 0(ON) are recommended due to the performance of the slew rate and cutoff frequency of the TB1305FG and TB1308FG circuits. A gain amplifier and/or a prefilter for 1125/50p/60p should be added as external circuits, if necessary.

Note on video output pins

To conduct the video signal from the TB1305FG or TB1308FG to the following circuits, a buffer such as the one in the application circuits is required due to the drive capability of the TB1305FG and TB1308FG being insufficient, especially for high-frequency components.

The DC levels of the video output vary according to I^2CBUS functions, the APL of the input and temperature drift.Therefore, the DC levels should be re-clamped in connected circuits such as AD converters.

Recommended crystal oscillator

When a connected crystal oscillator is used for the XO, the following oscillation specifications are required.

Oscillation frequency (fundamental): 3.579545 MHz (for NTSC decoding)

Frequency tolerance: +/- 50 ppm

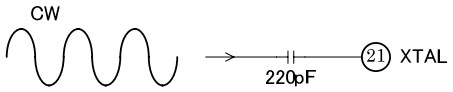
External CW input into crystal oscillator pin

Instead of connecting a crystal oscillator, it is possible to input an external CW (Continual Wave) into pin 21 through a capacitor as below.

The specifications required for CW input are as follows.

Input frequency (fundamental): 3.579545 MHz +/- 50 ppm

Input amplitude: 1.0 Vp-p +/- 0.5 Vp-p



How to deal with unused pins

Unused pins should be dealt with as below. Pins not mentioned below should be connected properly.

Pin No.	Pin Name	Procedure	Pin No.	Pin Name	Procedure
1	Cr1/R1-IN	Procedure 1	25	VD2-IN	Procedure 4
2	LINE3-1	Procedure 2	26	HD2-IN	Procedure 4
3	Cb1/B1-IN	Procedure 1	27	ADDRESS	Procedure 3
4	LINE2-1	Procedure 2	28	SYNC-OUT	Procedure 3
5	Y1/G1-IN	Procedure 1	29	VD-OUT	Procedure 3
6	LINE1-1	Procedure 2	30	HD-OUT	Procedure 3
7	NC	Procedure 2	32	Y-OUT	Procedure 3
8	SYNC1-IN	Procedure 3	34	Cb-OUT	Procedure 3
9	SW LINE2	Procedure 2	36	Cr-OUT	Procedure 3
10	Cr2/R2-IN	Procedure 1	37	NC	Procedure 2
11	LINE3-2	Procedure 2	38	SYNC3-IN	Procedure 3
12	Cb2/B2-IN	Procedure 1	39	Y3/G3-IN	Procedure 1
13	LINE2-2	Procedure 2	41	Cb3/B3-IN	Procedure 1
14	Y2/G2-IN	Procedure 1	42	DAC2	Procedure 3
15	LINE1-2	Procedure 2	43	Cr3/R3-IN	Procedure 1
16	SYNC2-IN	Procedure 3	45	C-IN	Procedure 1
17	DAC1	Procedure 3	47	Y-IN	Procedure 1
23	VD1-IN	Procedure 4	48	SW LINE1	Procedure 2
24	HD1-IN	Procedure 4	—	—	—

Procedure 1: Connect a 1 μF capacitor between this pin and GND.
Procedure 2: Connect to GND.
Procedure 3: Leave open.
Procedure 4: Connect a 10 kΩ resister between this pin and GND.

NOTE: Pins 38, 39, 41 and 43 are NC pins for the TB1305FG. Of these, any unused pins should be dealt with as in “Procedure 2”.

How to Start the I^2CBUS

How to send bus data after power on is described below. Use software to handle the procedure.

1. Turn power on.
2. Transmit all write data.

How to Transmit/Receive via the I^2CBUS

Slave Address: Can Be Changed Using Pin 27.

Pin 27-GND: $D8_H/D9_H$

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	0	0	0/1

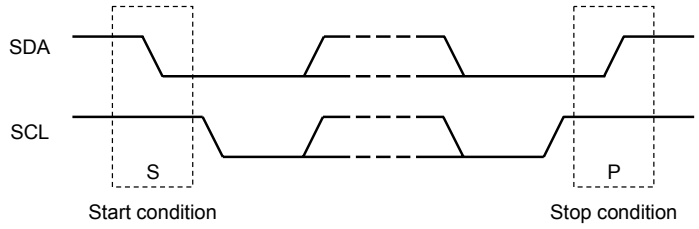
Pin 27-OPEN: DA_H/DB_H

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	0	1	0/1

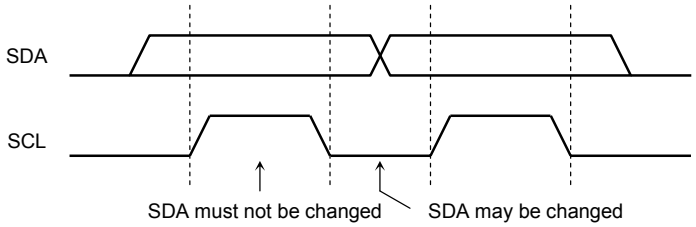
Pin 27-Vcc: DC_H/DD_H

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	1	0	0/1

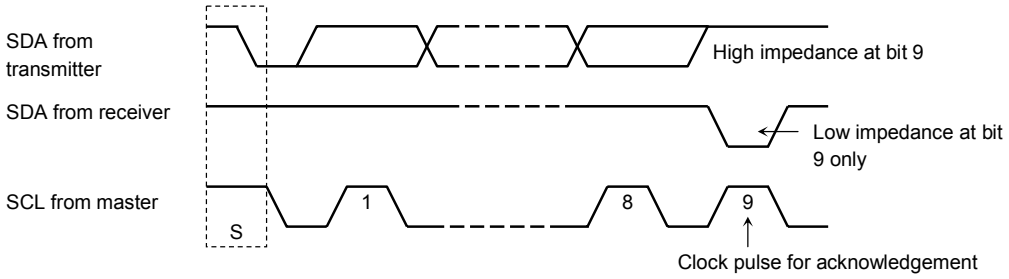
Start and Stop Conditions



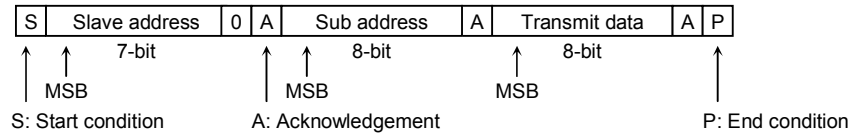
Bit Transmission



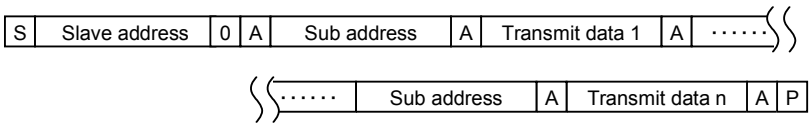
Acknowledgement



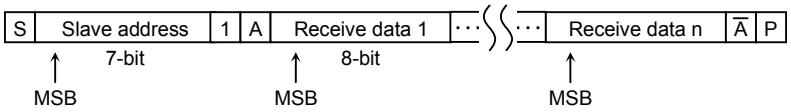
Data Transmit Format 1



Data Transmit Format 2



Data Receive Format



To receive data, the master transmitter changes to a receiver immediately after the first acknowledgement. The slave receiver changes to a transmitter.

The end condition is always created by the master.

Optional Data Transmit Format (Automatic Increment Mode)

In this way, sub-addresses are automatically incremented from the specified sub-address and data are set.

I^2CBUS Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Low level input voltage	V_{IL}	0	–	1.1	V
High level input voltage	V_{IH}	2.8	–	H-Vcc	V
Hysteresis of Schmitt trigger inputs	V_{hys}	–	0.7	–	V
Low level output voltage at 3 mA sink current	V_{OL1}	0	–	0.6	V
Input current each I/O pin with an input voltage between 0.1 VDD and 0.9 VDD	I_i	-10	–	10	μA
Capacitance for each I/O pin	C_i	–	–	10	pF
SCL clock frequency	f_{SCL}	0	–	400	kHz
Hold time START condition	$t_{HD;STA}$	0.6	–	–	μs
Low period of SCL clock	t_{LOW}	1.3	–	–	μs
High period of SCL clock	t_{HIGH}	0.6	–	–	μs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	–	–	μs
Data hold time	$t_{HD;DAT}$	50	–	–	ns
Data set-up time	$t_{SU;DAT}$	100	–	–	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	–	–	μs
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	–	μs

NOTE: This parameter is not tested during production and is provided only as information to assist the design of applications.

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Supply voltage	V_{CCmax}	6.0	V
Input pin voltage	V_{in}	GND − 0.3 ~ Vcc + 0.3	V
Y or Sync input amplitude (pins 5, 8, 14, 16, 38, 39, 47) (Pins 38, 39 are for the TB1308FG only.)	Y_{in}	2.0	Vp-p
Power dissipation	P_D(Note 5)	1136	mW
Power dissipation reduction rate	1/θja	9.1	mW/°C
Operating temperature	T_{opr}	−20 ~ 75	°C
Storage temperature	T_{stg}	−55 ~ 150	°C

Note 5: Refer to the figure below.

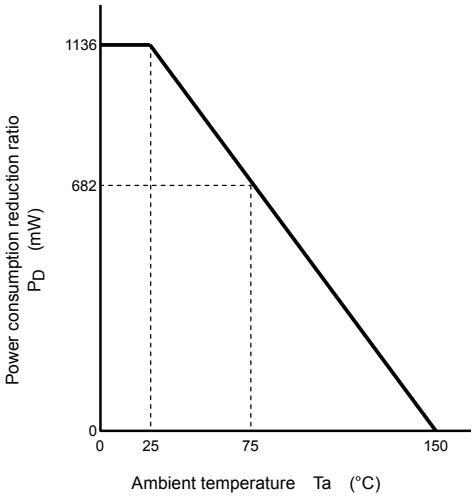


Figure. P_D - Ta Curve

Note 6: Handle pins 7 and 37 of the TB1305FG and TB1308FG with special care. These ICs are sensitive to electrostatic discharge and surge impulse.

Install the product correctly. Otherwise, it may result in break down, damage and/or degradation to the product or equipment.

The absolute maximum ratings of a semiconductor device are a set of specified parameter values that must not be exceeded during operation, even for an instant.

If any of these ratings are exceeded during operation, the electrical characteristics of the device may be irreparably altered, in which case the reliability and lifetime of the device can no longer be guaranteed.

Moreover, operations with exceeded ratings may cause breakdown, damage and/or degradation in other equipment. Applications using the device should be designed so that no maximum rating will ever be exceeded under any operating conditions.

Before using, creating and/or producing designs, refer to and comply with the precautions and conditions set forth in these documents.

Operating conditions

Characteristic		Description		Min.	Typ.	Max.	Unit
Supply voltage (V_{CC})		Pins 31, 46		4.7	5.0	5.3	V
		Pin 22; supply power from H Vcc (pin 31) via a resistor.		3.1	3.3	3.5	
Y signal input amplitude		Pins 5, 8, 14, 16, 38, 39, 47; with sync		—	1.0	—	V_{p-p}
G signal input amplitude		Pins 8, 16, 38; with sync		—	1.0	—	V_{p-p}
Y signal input frequency		Pins 5, 14, 39		0	—	60	MHz
		Pin 47		0	—	8	
Chroma signal input amplitude		Pin 45		—	0.3	2	V_{p-p}
DC voltage of chroma input pin		Pin 45		—	—	3.6	V
Cb, Cr, Pb, Pr signal input amplitude		Pins 1, 3, 10, 12, 41, 43; 100% color bar signal		—	0.7	—	V_{p-p}
Cb, Cr, Pb, Pr signal input frequency		Pins 1, 3, 10, 12, 41, 43		0	—	60	MHz
R, G, B signal input amplitude		Pins 1, 3, 5, 10, 12, 14, 39, 41, 43; 100% white signal without sync		—	0.7	—	V_{p-p}
R, G, B signal input frequency		Pins 1, 3, 5, 10, 12, 14, 39, 41, 43, 39, 41, 43		0	—	60	MHz
HD, VD signal input amplitude		Pins 23, 24, 25, 26		1.0	—	2.0	V_{p-p}
HD input frequency		Pins 24, 26 for freq counter		0	—	85	kHz
VD input frequency		Pins 23, 25 for freq counter		44	—	3500	Hz
LINE detection input voltage	LINE1,3	Pins 2, 6, 11, 15	H	3.5	5.0	C-Vcc	V
			M	1.4	2.2	2.4	
			L	—	GND	0.6	
	LINE2	Pins 4, 13	H	1.4	2.2	C-Vcc	V
			L	—	GND	0.6	
	SW LINE	Pins 9, 48	H	1.4	5.0	C-Vcc	V
			L	—	GND	0.6	
ADDRESS switching voltage		Pin 27	$88/89_H$	—	GND	0.6	V
			DA/DB_H	Pin open			
			DC/DD_H	3.5	C-Vcc	C-Vcc	
SDA input current		Pin 18		—	—	3	mA

Remark: Supply power to all Vcc pins (pins 22, 31 and 46).

NOTE: Pins 38, 39, 41 and 43, as Y/Cb/Cr/SYNC3-IN, are available for the TB1308FG only. Pins 38, 39, 41 and 43 of the TB1305FG are NC pins.

Electrical Characteristics

(Unless otherwise specified, C and H V_{CC} = 5 V, D V_{CC} = 3.3 V, Ta = 25°C, I^2CBUS data: preset values)

Current Consumption

Pin Name	Symbol	Test Conditions	Min	Typ.	Max	Unit
C V_{CC} (pin 46)	I_{CCC}	—	30.0	38.0	46.0	mA
H V_{CC} (pin 31)	I_{CCH}	—	4.5	6.0	7.5	
D V_{CC} (pin 22)	I_{CCD}	Resistance to 5 V; R = 150 Ω	8.5	10.5	12.5	

Pin Voltage (test condition: no signal input)

Pin No.	Pin Name	Symbol	Test Conditions	Min	Typ.	Max	Unit
1	Cr1/R1-IN	V_1	—	2.6	2.7	2.8	V
2	LINE3-1	V_2	—	4.8	—	—	
3	Cb1/B1-IN	V_3	—	2.6	2.7	2.8	
4	LINE2-1	V_4	—	4.8	—	—	
5	Y1/G1-IN	V_5	—	1.95	2.1	2.25	
6	LINE1-1	V_6	—	4.8	—	—	
8	SYNC1-IN	V_8	—	1.4	1.75	2.1	
9	SW LINE2	V_9	—	4.8	—	—	
10	Cr2/R2-IN	V_{10}	—	2.6	2.7	2.8	
11	LINE3-2	V_{11}	—	4.8	—	—	
12	Cb2/B2-IN	V_{12}	—	2.6	2.7	2.8	
13	LINE2-2	V_{13}	—	4.8	—	—	
14	Y2/G2-IN	V_{14}	—	1.95	2.1	2.25	
15	LINE1-2	V_{15}	—	4.8	—	—	
16	SYNC2-IN	V_{16}	—	1.4	1.75	2.1	
21	XTAL	V_{21}	—	3.7	3.85	4.0	
22	DIG Vcc	V_{22}	Resistance to 5 V; R = 150 Ω	3.2	3.35	3.5	
23	VD1-IN	V_{23}	—	1.2	1.45	1.7	
24	HD1-IN	V_{24}	—	1.2	1.45	1.7	
25	VD2-IN	V_{25}	—	1.2	1.45	1.7	
26	HD2-IN	V_{26}	—	1.2	1.45	1.7	
27	ADDRESS	V_{27}	Pin open	1.8	2.0	2.2	
32	Y-OUT	V_{32}	—	0.3	1.0	1.7	
34	Cb-OUT	V_{34}	—	1.5	1.95	2.4	
35	Vf0ADJ	V_{35}	—	2.2	2.5	2.8	
36	Cr-OUT	V_{36}	—	1.5	1.95	2.4	
38	SYNC3-IN	V_{38}	For the TB1308FG only	1.4	1.75	2.1	
39	Y3/G3-IN	V_{39}	For the TB1308FG only	1.95	2.1	2.25	
40	BIAS FIL	V_{40}	—	1.6	1.8	2.0	
41	Cb3/B3-IN	V_{41}	For the TB1308FG only	2.6	2.7	2.8	
43	Cr3/R3-IN	V_{43}	For the TB1308FG only	2.6	2.7	2.8	
45	C-IN	V_{45}	—	1.6	1.7	1.8	
47	Y-IN	V_{47}	—	1.95	2.1	2.25	
48	SW LINE1	V_{48}	—	4.8	—	—	

Video Block

Characteristic			Symbol	Test Conditions	Min	Typ.	Max	Unit
Input dynamic range	Sync-tip clamp mode		Vdsync	FILPASS = 1, BANDWIDTH = max	1.40	1.65	—	Vp-p
	Bias mode		Vdbias		1.40	1.65	—	
	Chroma input		Vdchrm	Pin 45	1.40	1.65	—	
I/O gain		GAIN = 0	Gfoffg0	FILPASS = 0, input = 0.2Vp-p 10 kHz	-1.0	-0.5	0	dB
		GAIN = 1	Gfoffg6		5.0	5.5	6.0	
		GAIN = 0	Gfong0	FILPASS = 1, f0 SW = 0, BANDWIDTH = min, input = 0.2 Vp-p 10 kHz	-0.5	0	0.5	
		GAIN = 1	Gfong6		5.5	6.0	6.5	
I/O frequency characteristic 1	GAIN = 0		fg0	FILPASS = 0, -3 dB point, NOTE 7	70	90	110	MHz
	GAIN = 1		fg6		60	80	100	
I/O frequency characteristic 2	BANDWIDTH = max		fLmax	FILPASS = 1, GAIN = 0, f0 SW = 1, -3 dB point, NOTE 7	18.4	20.5	22.6	MHz
	BANDWIDTH = cnt		fLcnt		11.4	12.7	14.0	
	BANDWIDTH = min		fLmin		3.7	4.2	4.7	
I/O frequency characteristic 3	BANDWIDTH = max		fHmax	FILPASS = 1, GAIN = 0, f0 SW = 0, -3 dB point, NOTE 7	27.9	31.0	34.1	MHz
	BANDWIDTH = cnt		fHcnt		21.6	24.0	26.4	
	BANDWIDTH = min		fHmin		14.6	16.3	18.0	
I/O frequency characteristic 4	BANDWIDTH = max		fhfLmax	FILPASS = 1, GAIN = 0, f0 SW = 1, fc HALF = 1, -3 dB point, NOTE 7	9.2	10.3	11.4	MHz
	BANDWIDTH = cnt		fhfLcnt		5.7	6.4	7.1	
	BANDWIDTH = min		fhfLmin		1.85	2.1	2.35	
I/O frequency characteristic 5	BANDWIDTH = max		fhfHmax	FILPASS = 1, GAIN = 0, f0 SW = 0, fc HALF = 1, -3 dB point, NOTE 7	13.9	15.5	17.1	MHz
	BANDWIDTH = cnt		fhfHcnt		10.8	12	13.2	
	BANDWIDTH = min		fhfHmin		7.3	8.2	9.1	
Differential 1 of frequency characteristic among 3 outputs	GAIN = 0		fdg0	FILPASS = 0, -3 dB point, NOTE 7	-10	0	10	MHz
	GAIN = 1		fdg6		-10	0	10	
Differential 2 of frequency characteristic among 3 outputs	BANDWIDTH = max		fdHmax	FILPASS = 1, f0 SW = 1, -3 dB point, NOTE 7	-0.90	0	0.90	MHz
	BANDWIDTH = cnt		fdHcnt		-0.54	0	0.54	
	BANDWIDTH = min		fdHmin		-0.18	0	0.18	
Differential 3 of frequency characteristic among 3 outputs	BANDWIDTH = max		fdHmax	FILPASS = 1, f0 SW = 0, -3 dB point, NOTE 7	-1.30	0	1.30	MHz
	BANDWIDTH = cnt		fdHcnt		-1.05	0	1.05	
	BANDWIDTH = min		fdHmin		-0.70	0	0.70	
I/O delay time 1	GAIN = 0		Tdg0	FILPASS = 0, 1 MHz, NOTE 7	—	5	10	ns
	GAIN = 1		Tdg6		—	5	10	
I/O delay time 2	BANDWIDTH = max		TdLmax	FILPASS = 1, GAIN = 0, f0 SW = 1, 1 MHz, NOTE 7	18	23	28	ns
	BANDWIDTH = cnt		TdLcnt		29	34	39	
	BANDWIDTH = min		TdLmin		85	95	105	
I/O delay time 3	BANDWIDTH = max		TdHmax	FILPASS = 1, GAIN = 0, f0 SW = 0, 1 MHz, NOTE 7	10	15	20	ns
	BANDWIDTH = cnt		TdHcnt		15	20	25	
	BANDWIDTH = min		TdHmin		22	27	32	
I/O delay time 4	BANDWIDTH = max		TdhfLmax	FILPASS = 1, GAIN = 0, f0 SW = 1, fc HALF = 1, 1 MHz, NOTE 7	35	40	45	ns
	BANDWIDTH = cnt		TdhfLcnt		58	65	72	
	BANDWIDTH = min		TdhfLmin		170	190	210	

Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
I/O delay time 5	BANDWIDTH = max	TdhfHmax	FILPASS = 1, GAIN = 0, f0 SW = 0, fc HALF = 1, 1 MHz, NOTE 7	22	27	32	ns
	BANDWIDTH = cnt	TdhfHcnt		29	34	39	
	BANDWIDTH = min	TdhfHmin		45	50	55	
Differential 1 of delay time among 3 outputs	GAIN = 0	Tddg0	FILPASS = 0, 1 MHz, NOTE 7	-10	0	10	ns
	GAIN = 1	Tddg6		-10	0	10	
Differential 2 of delay time among 3 outputs	BANDWIDTH = max	TddHmax	FILPASS = 1, f0 SW = 1, 1 MHz, NOTE 7	-10	0	10	ns
	BANDWIDTH = cnt	TddHcnt		-10	0	10	
	BANDWIDTH = min	TddHmin		-10	0	10	
Differential 3 of delay time between Y and Cb/Cr outputs	BANDWIDTH = max	TddHmax	FILPASS = 1, f0 SW = 0, fc HALF = 1, 1 MHz, NOTE 7	0	10	20	ns
	BANDWIDTH = cnt	TddHcnt		10	20	30	
	BANDWIDTH = min	TddHmin		35	45	55	
Differential 4 of delay time between Cb and Cr outputs	BANDWIDTH = max	TddHmax	FILPASS = 1, f0 SW = 0, fc HALF = 1, 1 MHz, NOTE 7	-10	0	10	ns
	BANDWIDTH = cnt	TddHcnt		-10	0	10	
	BANDWIDTH = min	TddHmin		-10	0	10	
Mute mode attenuation		Gmute	30 MHz sin wave input, NOTE 7	—	—	-50	dB
Crosstalk among inputs		Gcrs	30 MHz sin wave input, NOTE 7	—	—	-50	dB

NOTE 7: This parameter is not tested during production and is provided only as information to assist the design of applications.

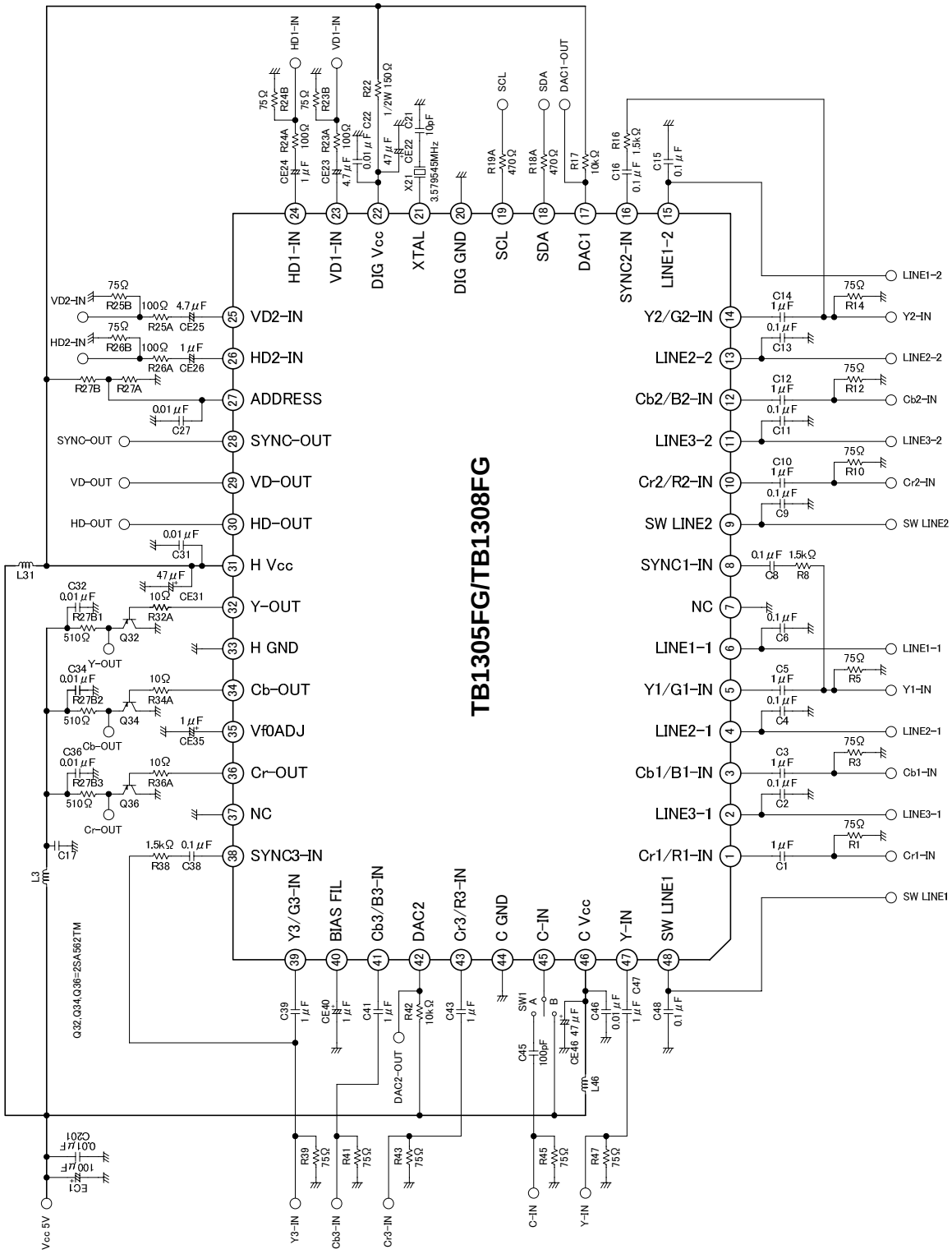
Synchronization Block (Test condition: A-SYNC = 1 (ON))

Characteristic		Symbol	Test Conditions	Min	Typ	Max	Unit
H/V-sync separation level	525/60i	VsepL1	HV-SEP = 0, 286 mVp-p sync, NOTE 7	24	28	32	%
		VsepH1	HV-SEP = 1, 286 mVp-p sync, NOTE 7	27	31	35	
	1125/60i	VsepL2	HV-SEP = 0, 0.3 Vp-p sync, NOTE 7	30	34	38	%
		VsepH2	HV-SEP = 1, 0.3 Vp-p sync, NOTE 7	40	44	48	
	SVGA/60	VsepL3	HV-SEP = 0, VGA-SEP = 1, 0.3 Vp-p sync, NOTE 7	14	18	22	%
		VsepH3	HV-SEP = 1, VGA-SEP = 1, 0.3 Vp-p sync, NOTE 7	16	20	24	
Threshold amplitude for HD input		VthHD	SYNC SW = 100	0.8	—	—	Vp-p
Threshold amplitude for VD input		VthVDn	SYNC SW = 100	0.9	—	—	Vp-p
HD-OUT voltage		VhdH	High level	3.2	3.4	3.5	V
		VhdL	Low level	—	0.1	0.4	
HD-OUT width		Thdw0	HD WIDTH = 0	1.55	1.65	1.75	us
		Thdw1	HD WIDTH = 1	0.55	0.65	0.75	
HD-OUT phase	H sync-in to HD-out	Thdp1	SYNC-SW = 000, 1125/60p input	130	150	170	ns
	HD-in to HD-out	Thdp2	SYNC-SW = 100, NOTE 7	23	28	32	ns

Characteristic			Symbol	Test Conditions	Min	Typ.	Max	Unit
VD-OUT voltage			VvdH	High level	3.2	3.4	3.5	V
			VvdL	Low level	—	0.1	0.4	
VD-OUT width	Sync sep		Tvdws	Separated VD-OUT	—	290	—	us
	1250i ODD		Tvdwodd	When 1250i input	—	285	—	us
	1250i EVEN		Tvdweven		—	270	—	
	Free-run 1		Tvdwfi	Free-run VD-OUT in interlace mode	—	4	—	H
	Free-run 2		Tvdwfp	Free-run VD-OUT in progressive mode	—	8	—	
VD-OUT phase	V sync-in to VD-out		Tvdp1	625/50i input	0.15	0.20	0.26	H
			Tvdp2	525/60i input	0.15	0.20	0.26	
			Tvdp3	625/50p input	0.15	0.20	0.26	
			Tvdp4	525/60p input	0.15	0.20	0.26	
			Tvdp5	1125/50i input	0.15	0.20	0.26	
			Tvdp6	1125/60i input	0.15	0.20	0.26	
			Tvdp7	750/50p input	0.15	0.20	0.26	
			Tvdp8	750/60p input	0.15	0.20	0.26	
			Tvdp9	1125/50p input	0.10	0.15	0.20	
			Tvdp10	1125/60p input	0.15	0.20	0.26	
			Tvdp11	VGA/60 input	0.15	0.20	0.26	
			Tvdp12	SVGA/60 input	0.15	0.20	0.26	
			Tvdp13	XGA input	0.15	0.20	0.26	
			Tvdp14	SXGA input	0.15	0.20	0.26	
			Tvdp15	UXGA input	0.15	0.20	0.26	
	H sync-in to VD-out		Tvdp16	1250/50i input, H sync-in to VD-out	330	340	350	ns
	VD-in to VD-out		Tvdp17	SYNC-SW=100, NOTE 7	23	28	32	ns
Minimum amplitude for suppressed V-sync to separate		HV-SEP = 0	VsupvL	Suppressed H/V-sync input, without picture, NOTE 7	—	—	52	%
		HV-SEP = 1	VsupvH		—	—	48	
SYNC−OUT voltage			VsoH	High level	3.2	3.4	3.5	V
			VsoL	Low level	—	0.1	0.4	

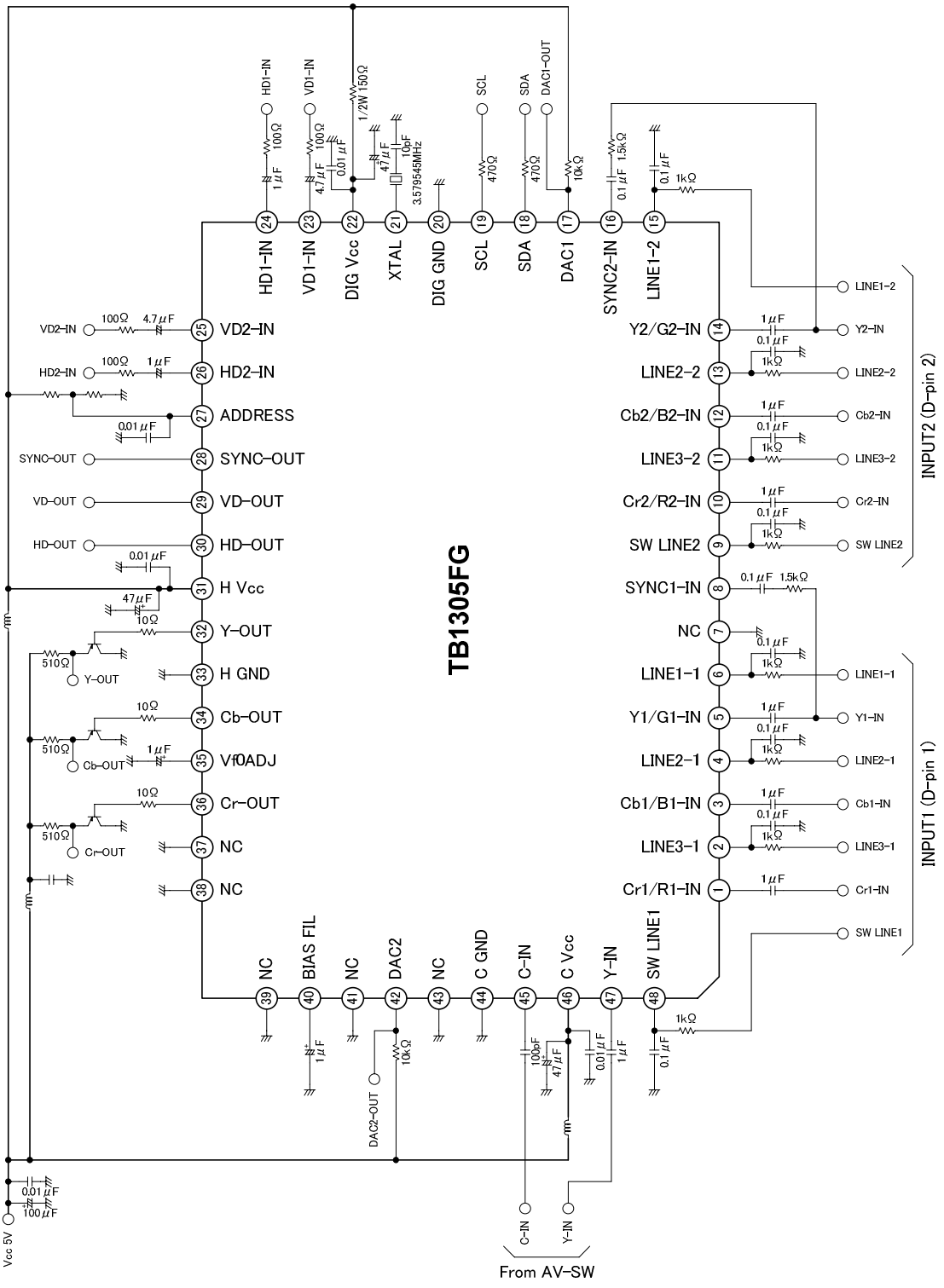
Characteristic		Symbol	Test Conditions	Min	Typ.	Max	Unit
Dummy HD-OUT frequency		fh156	HV FREQ = 0000, S MODE = 1	—	15.564	—	kHz
		fh157	HV FREQ = 0001, S MODE = 1	—	15.701	—	
		fh312	HV FREQ = 0010, S MODE = 1	—	31.401	—	
		fh315	HV FREQ = 0011, S MODE = 1	—	31.401	—	
		fh281	HV FREQ = 0100, S MODE = 1	—	27.966	—	
		fh337	HV FREQ = 0101, S MODE = 1	—	33.771	—	
		fh375	HV FREQ = 0110, S MODE = 1	—	37.288	—	
		fh450	HV FREQ = 0111, S MODE = 1	—	44.746	—	
		fh1250	HV FREQ = 1000, S MODE = 1	—	31.401	—	
		fh379	HV FREQ = 1001, S MODE = 1	—	37.288	—	
		fh640	HV FREQ = 1010, S MODE = 1	—	63.923	—	
		fh750	HV FREQ = 1011, S MODE = 1	—	74.577	—	
		fh562	HV FREQ = 1100, S MODE = 1	—	55.932	—	
Dummy VD-OUT frequency		fv625i	HV FREQ = 0000, S MODE = 1	—	312.5	—	H
		fv525i	HV FREQ = 0001, S MODE = 1	—	262.5	—	
		fv625p	HV FREQ = 0010, S MODE = 1	—	625	—	
		fv525p	HV FREQ = 0011, S MODE = 1	—	525	—	
		fv1125i5	HV FREQ = 0100, S MODE = 1	—	562.5	—	
		fv1125i6	HV FREQ = 0101, S MODE = 1	—	562.5	—	
		fv750p5	HV FREQ = 0110, S MODE = 1	—	750	—	
		fv750p6	HV FREQ = 0111, S MODE = 1	—	750	—	
		fv1250iO	HV FREQ = 1000, S MODE = 1, ODD	—	624.5	—	
		fv1250iE	HV FREQ = 1000, S MODE = 1, EVEN	—	625.5	—	
		fvsvga	HV FREQ = 1001, S MODE = 1	—	628	—	
		fvsxga	HV FREQ = 1010, S MODE = 1	—	1066	—	
		fvuxga	HV FREQ = 1011, S MODE = 1	—	1250	—	
		fv1125p5	HV FREQ = 1100, S MODE = 1	—	1125	—	
VD PHS delay phase	others	Tvdphs1	No input, S MODE = 1, VD PHS = 1	0.15	0.2	0.26	H
	1125/50p	Tvdphs2		0.1	0.15	0.2	
LINE1 detection threshold	L⇔M	Vln1LM	Pin 6, 15	0.8	1.0	1.2	V
	M⇔H	Vln1MH		2.8	3.0	3.2	
LINE2 detection threshold	L⇔H	Vln2LH	Pin 4, 13	0.8	1.0	1.2	
LINE3 detection threshold	L⇔M	Vln3LM	Pin 2, 11	0.8	1.0	1.2	
	M⇔H	Vln3MH		2.8	3.0	3.2	
SW LINE detection threshold	L⇔H	VlnsLH	Pin 9, 48	0.8	1.0	1.2	
Input impedance of LINE input pin		Zline	Pin 2,4,6,9,11,13,15,48, NOTE 7	120	150	—	kΩ
DAC1,2 output voltage		VdacH	High level	4.8	5.0	—	V
		VdacL	Low level	—	0.2	0.4	
Test mode threshold voltage		Vontest	Pin 45, turned-on voltage for test mode	3.6	—	—	V

Test circuit



Components in the test circuits are only used to obtain and confirm the device characteristics. These components and circuits do not warrant to prevent the application equipment from malfunction or failure.

Application circuit 1 (TB1305FG: typical values)



Input video signals, which are driven with low impedance.

The application circuits shown in this document are examples provided for reference purposes only. Thorough evaluation is required in the mass production design phase.
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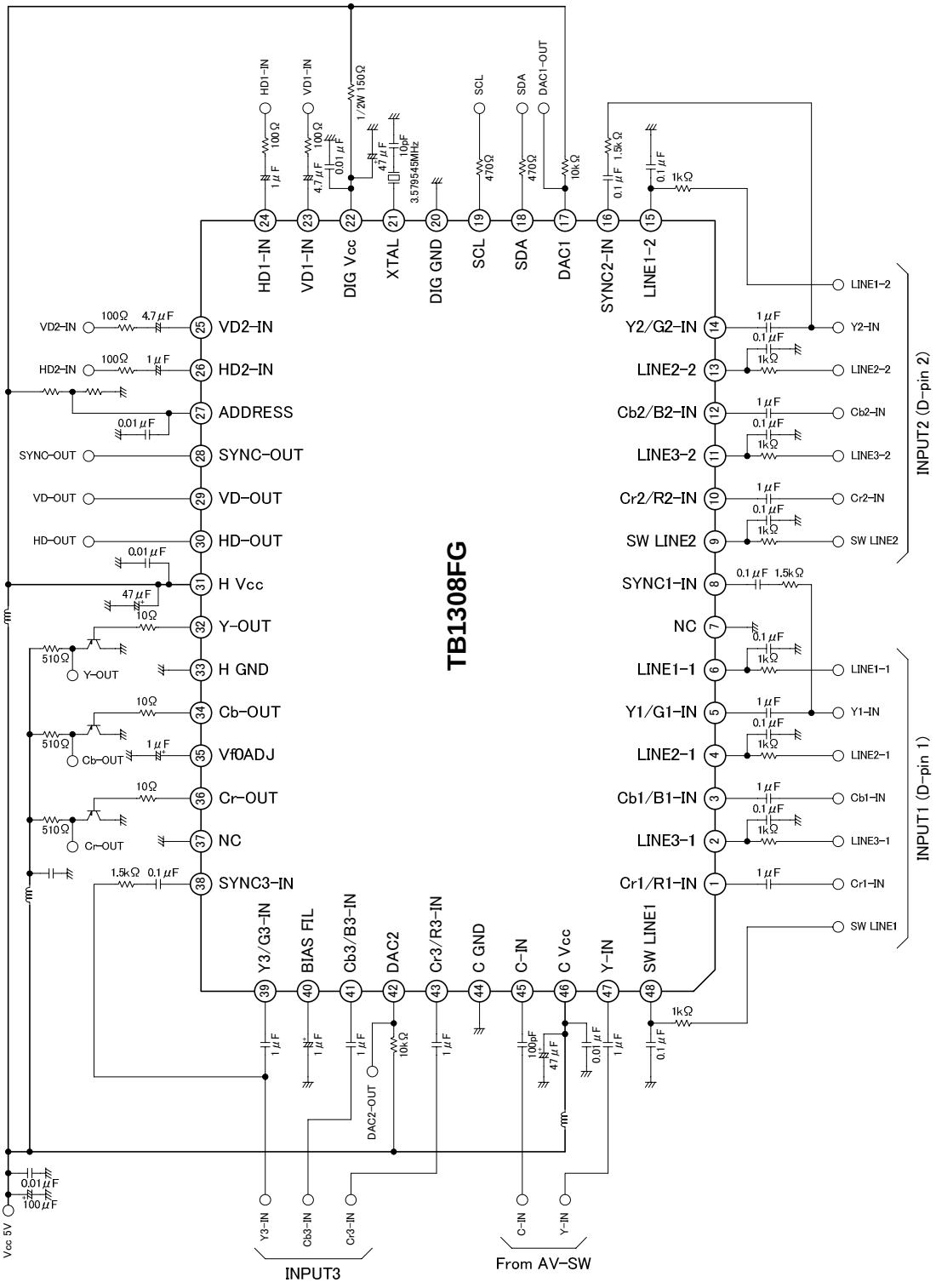
Application circuit 2 (TB1308FG: typical values)



Input video signals, which are driven with low impedance.

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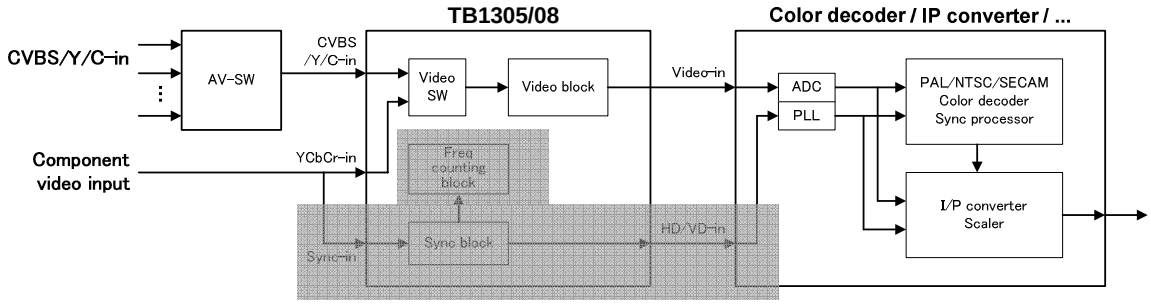
Application circuit 3 (system configuration)

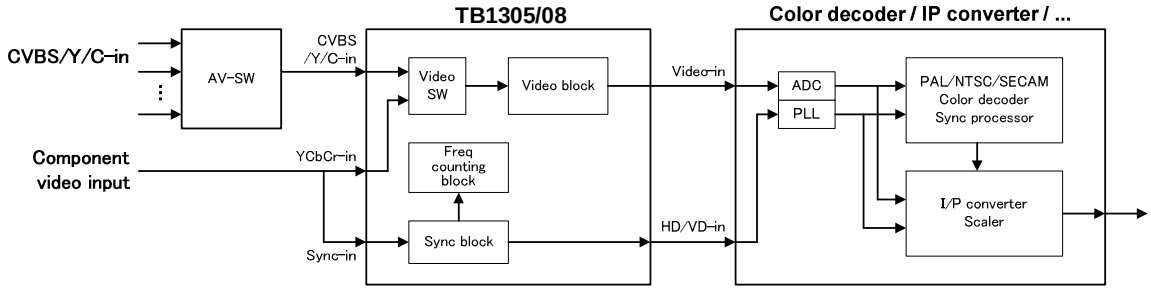
(1) For non-standard signals such as CVBS, YC (S-video), 525i, 625i or so.



The TB1305FG and TB1308FG cannot be used for non-standard signals such as weak strength signals, ghost signals and so on. Therefore, these signals should be dealt with through the use of another device such as a color-decoder which is capable of handling these signals. In such cases, the signal switcher and the video circuits of the TB1305FG and TB1308FG can be used.

The TB1305FG and TB1308FG cannot distinguish between component and RGB video. The different kinds of input signal should be separated through the use of different signal-specific input pins; for example, specific-purpose pins for RGB video input only or component video input only.

(2) For standard component video (SMPTE STANDARD) and standard RGB video (VESA STANDARD)



The TB1305FG and TB1308FG can detect a format type for standard signal inputs.

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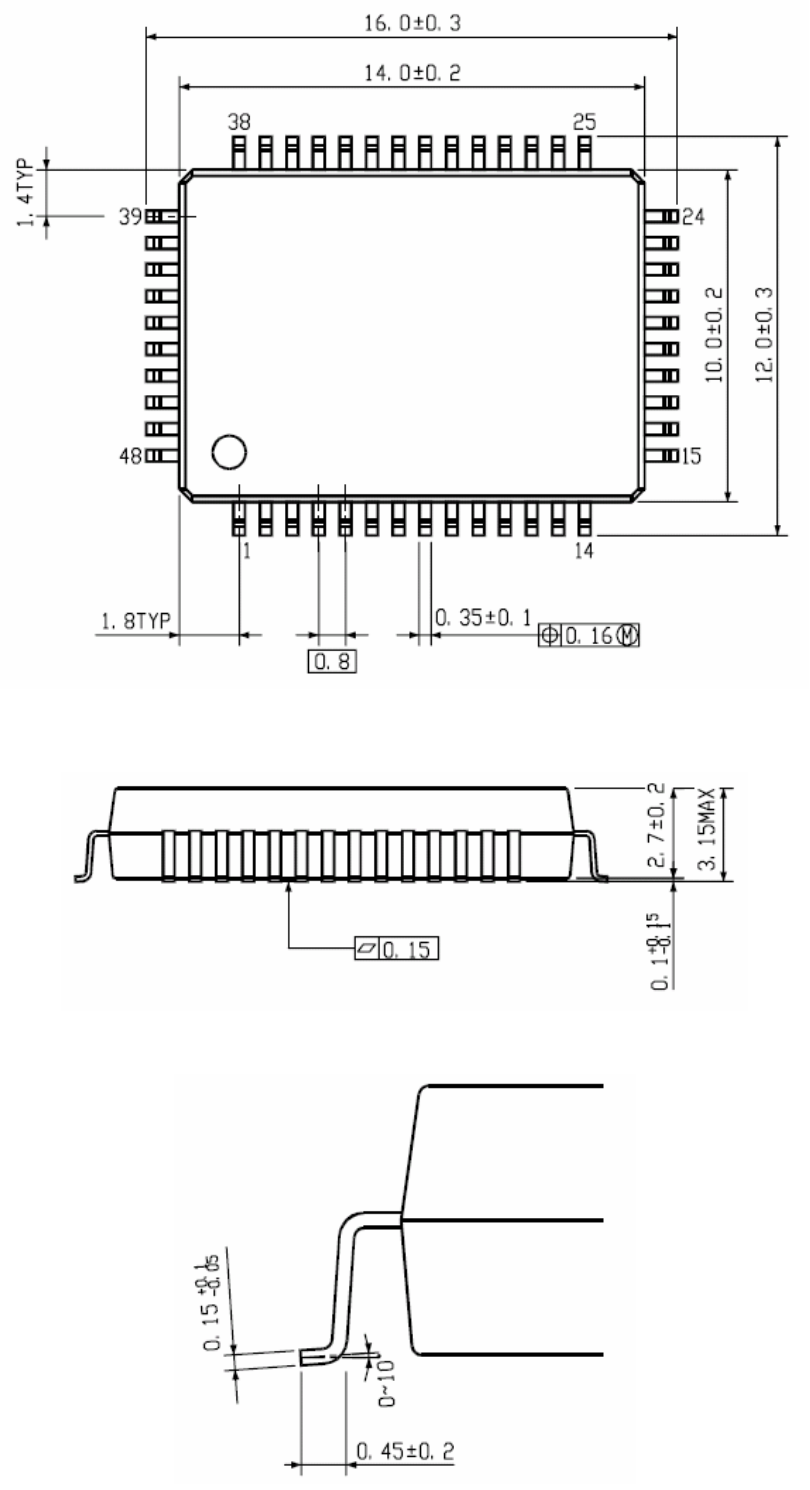
Package dimensions

P-QFP48-1014-0.80 Unit: mm



Weight: 0.83 g (typ.)

Appendix: Comparison Table of the Family

1) Pin functions

Pin No.	TB1305FG	TB1308FG
Pin 38	NC	SYNC3-IN
Pin 39	NC	Y3/G3-IN
Pin 41	NC	Cb3/B3-IN
Pin 43	NC	Cr3/R3-IN

2) Write BUS functions

Name	Data	TB1305FG	TB1308FG
YCbCr SW	11	Not available	Y3/Cb3/Cr3
SYNC SW	010	Not available	SYNC3
	110	HD1/VD1/Not available	HD1/VD1/SYNC3
	111	HD2/VD2/Not available	HD2/VD2/SYNC3

3) Read BUS functions

Name	TB1305FG	TB1308FG
VERSION	00: TB1305FG	01: TB1308FG

About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-37Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

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