

Toshiba CMOS Digital Integrated Circuit Silicon Monolithic

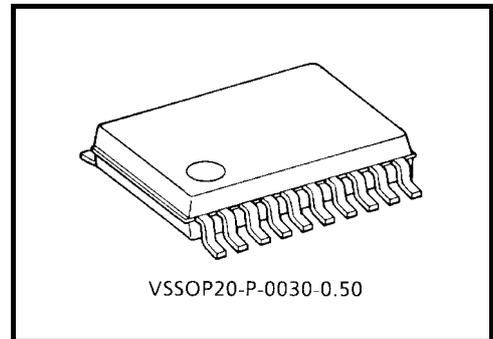
TC7MB3244FK

Octal Bus Switch

The TC7MB3244FK provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low on resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 4-bit low-impedance switches with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the switch is on and data can flow from port A to port B, or vice versa. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

All inputs are equipped with protection circuits against static discharge.

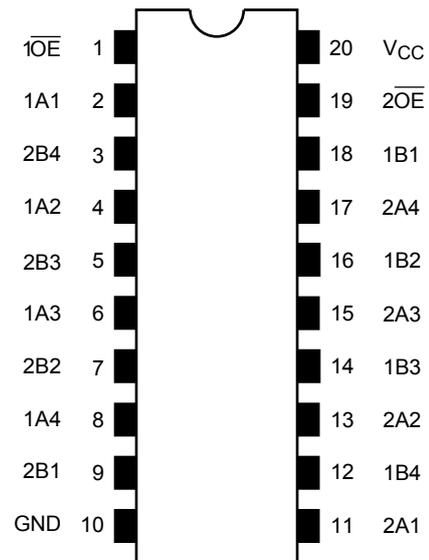


Weight: 0.03 g (typ.)

Features

- Operating voltage: $V_{CC} = 4.5\sim 5.5$ V
- High speed: $t_{pd} = 0.25$ ns (max)
- Low on resistance: $R_{ON} = 5 \Omega$ (typ.)
- ESD performance: Machine model $\geq \pm 200$ V
Human body model $\geq \pm 2000$ V
- Compatible with TTL outputs (control inputs)
- Package: VSSOP (US20)
- Pin compatible with the 74xx244 type.
Functionally equivalent to (FST/CBT) 3244.

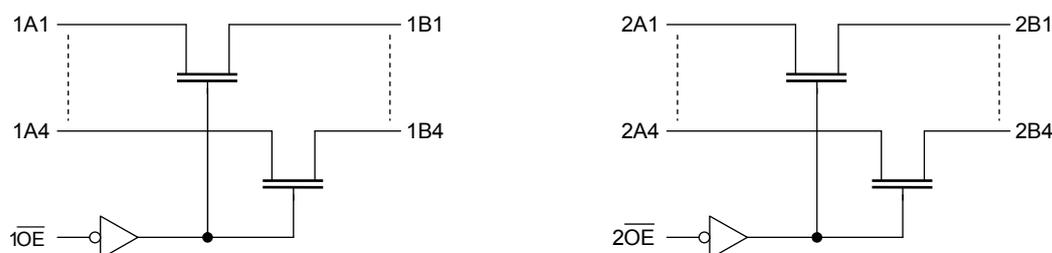
Pin Assignment (top view)



Truth Table

Inputs	Function
$\overline{\text{OE}}$	
L	A port = B port
H	Disconnect

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Power supply range	V_{CC}	-0.5~7.0	V
DC input voltage	V_{IN}	-0.5~7.0	V
DC switch voltage	V_S	-0.5~7.0	V
Input diode current	I_{IK}	-50	mA
Continuous channel circuit	I_S	128	mA
Power dissipation	P_D	180	mW
DC V_{CC} /ground current	I_{CC}/I_{GND}	± 100	mA
Storage temperature	T_{stg}	-65~150	$^{\circ}\text{C}$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5~5.5	V
Input voltage	V_{IN}	0~5.5	V
Switch voltage	V_S	0~5.5	V
Operating temperature	T_{opr}	-40~85	$^{\circ}\text{C}$
Input rise and fall time	dt/dv	0~10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condition		Min	Typ. (Note 1)	Max	Unit
Input voltage	"H" level	V _{IH}	—		4.5~5.5	2.0	—	V
	"L" level	V _{IL}	—		4.5~5.5	—	0.8	
Input leakage current		I _{IN}	V _{IN} = 0~5.5 V		4.5~5.5	—	±1.0	μA
Power off leakage current		I _{OFF}	A, B, \overline{OE} = 0~5.5 V		0	—	±1.0	μA
Off-STATE leakage current (switch off)		I _{SZ}	A, B = 0~5.5 V, \overline{OE} = V _{CC}		4.5~5.5	—	±1.0	μA
ON resistance (Note 2)	R _{ON}	V _{IS} = 0 V	I _{IS} = 64 mA		4.5	—	5	Ω
			I _{IS} = 30 mA		4.5	—	5	
		V _{IS} = 2.4 V, I _{IS} = 15 mA		4.5	—	10	15	
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND, I _{OUT} = 0		5.5	—	10	μA
Increase in I _{CC} per input		ΔI _{CC}	V _{IN} = 3.4 V (one input)		5.5	—	2.5	mA

Note 1: Typical values are at V_{CC} = 5 V, Ta = 25°C.

Note 2: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = -40~85°C)

Characteristics		Symbol	Test Condition		Min	Max	Unit	
								V _{CC} (V)
Propagation delay time (bus to bus)		t _{pLH} t _{pHL}	Figure 1, Figure 2 (Note)		4.5	—	0.25	ns
Output enable time		t _{pZL} t _{pZH}	Figure 1, Figure 3		4.5	—	5.0	ns
Output disable time		t _{pLZ} t _{pHZ}	Figure 1, Figure 3		4.5	—	5.0	ns

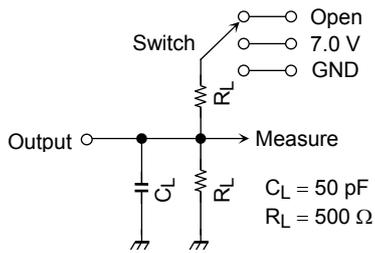
Note: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitive Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition		Typ.	Unit		
							V _{CC} (V)	
Control pin input capacitance		C _{IN}	(Note)		5.0	3	pF	
Switch terminal capacitance		C _{I/O}	\overline{OE} = V _{CC}		(Note)	5.0	10	pF

Note: Parameter guaranteed by design.

AC Test Circuit



Parameter	Switch
t_{pLH} , t_{pHL}	Open
t_{pLZ} , t_{pZL}	7.0 V
t_{pHZ} , t_{pZH}	Open

Figure 1

AC Waveform

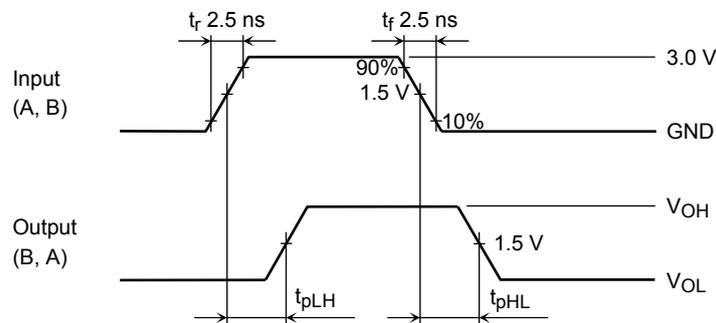


Figure 2 t_{pLH} , t_{pHL}

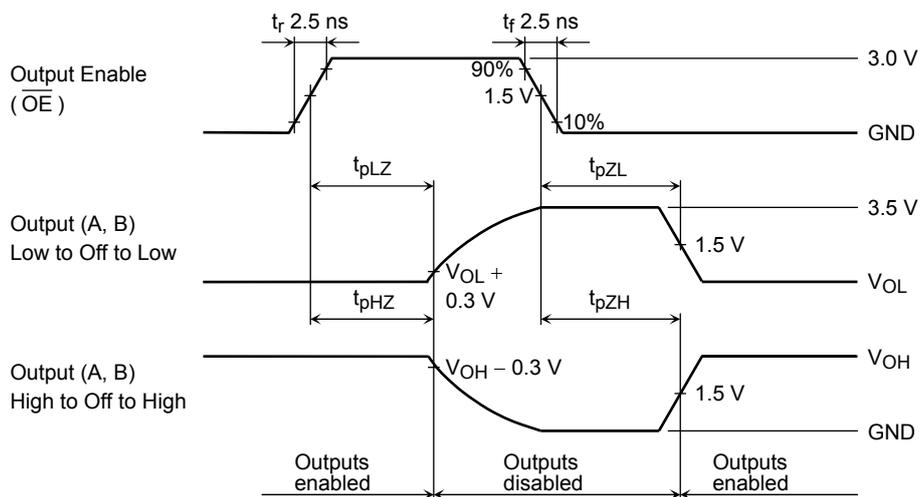
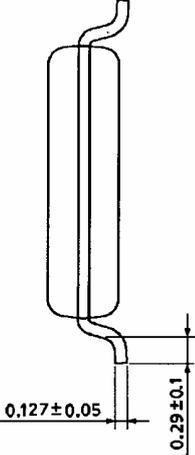
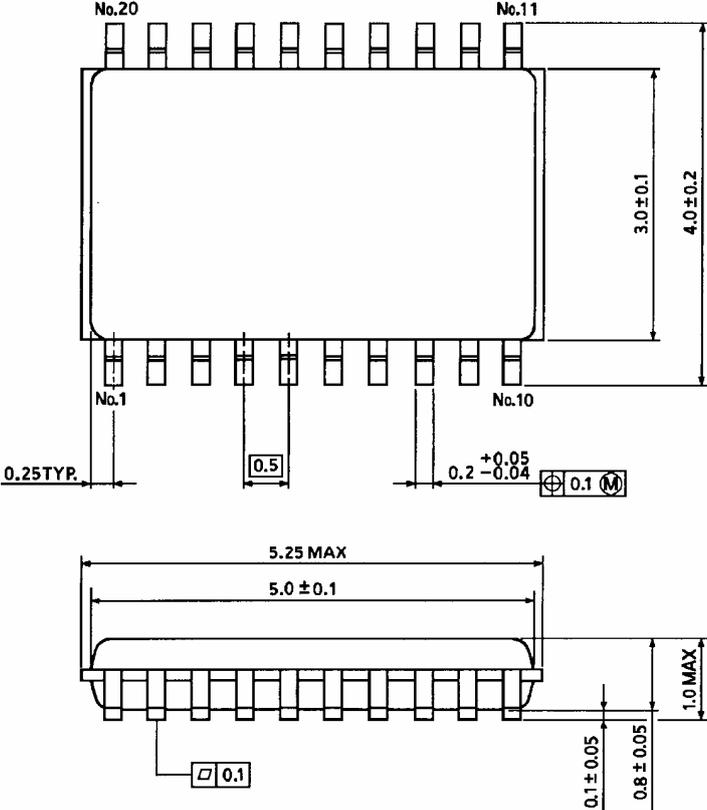


Figure 3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm



Weight: 0.03 g (typ.)

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20070701-EN GENERAL

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