

Ultra Low Power/High Speed CMOS SRAM 512K X 16 bit

Green package materials are compliant to RoHS

BH616UV8011

n FEATURES

Ÿ Wide V_{CC} low operation voltage: 1.65V ~ 3.6V

Ÿ Ultra low power consumption:

V_{CC} = 3.6V Operation current : 12mA (Max.)at 55ns

2mA (Max.) at 1MHz

Standby current: 2.5uA (Typ.) at 3.0V/25°C

 $V_{CC} = 1.2V$ Data retention current : 1.2uA (Typ.) at 25° C

Ÿ High speed access time:

-55 55ns (Max.) at V_{CC}=1.65~3.6V

- Ÿ Automatic power down when chip is deselected
- Ÿ Easy expansion with CE1, CE2 and OE options
- \ddot{Y} I/O Configuration x8/x16 selectable by \overline{LB} and \overline{UB} pin.
- $\ddot{\mathbf{Y}}$ Three state outputs and TTL compatible
- Ÿ Fully static operation, no clock, no refresh
- Ÿ Data retention supply voltage as low as 1.0V

n DESCRIPTION

The BH616UV8011 is a high performance, ultra low power CMOS Static Random Access Memory organized as 524,288 by 16 bits and operates in a wide range of 1.65V to 3.6V supply voltage.

Advanced CMOS technology and circuit techniques provide both high speed and low power features with typical operating current of 1.5mA at 1MHz at 3.6V/25°C and maximum access time of 55ns at 1.65V/85°C.

Easy memory expansion is provided by an active LOW chip enable $(\overline{CE1})$, an active HIGH chip enable $(\overline{CE2})$ and active LOW output enable (\overline{OE}) and three-state output drivers.

The BH616UV8011 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.

The BH616UV8011 is available in 48-ball BGA package.

n POWER CONSUMPTION

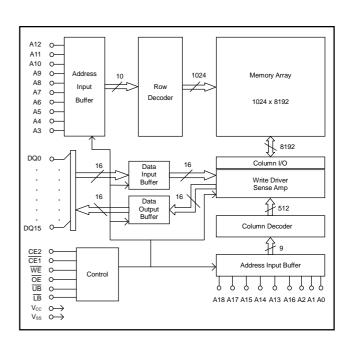
		POWER DISSIPATION								
PRODUCT FAMILY	OPERATING TEMPERATURE	STANDBY (I _{CCSB1} , Max)			Operating (I _{CC} , Max)					PKG TYPE
FAMILY IEMPER	I LIMII LIXATOILE	V _{CC} =3.6V	V _{CC} =1.8V		V _{CC} =3.6V			V _{CC} =1.8V		
		V _{CC} =3.0V	V _{CC} =1.6V	1MHz	10MHz	f _{Max.}	1MHz	10MHz	f _{Max.}	
BH616UV8011AI	Industrial -40°C to +85°C	15uA	12uA	2mA	6mA	12mA	1.5mA	5mA	8mA	BGA-48-0608

n PIN CONFIGURATIONS

3 5 6 OE Α2 LB A0 Α1 CE2 DQ8 UB CE1 DQ0 АЗ A4 В Α5 A6 DQ1 С DQ9 (DQ10) DQ2 _ vss (DQ11 A17 Α7 DQ3 vcc D vcc (DQ12 NC A16 DQ4 VSS Ε DQ14 (DQ13 A14 A15 DQ5 DQ6 F A13 DQ15 NC A12 WE DQ7 G A18 A10 A11 NC Н

48-ball BGA top view

n BLOCK DIAGRAM



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n PIN DESCRIPTIONS

Name	Function
A0-A18 Address Input	These 19 address inputs select one of the 524,288 x 16 bit in the RAM
CE1 Chip Enable 1 Input CE2 Chip Enable 2 Input	CE1 is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
WE Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{\text{WE}}$ is HIGH and $\overline{\text{OE}}$ is LOW, output data will be present on the DQ pins; when $\overline{\text{WE}}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
OE Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impendence state when OE is inactive.
LB and UB Data Byte Control Input	Lower byte and upper byte data input/output control pins.
DQ0-DQ15 Data Input/Output Ports	16 bi-directional ports are used to read data from or write data into the RAM.
V _{cc}	Power Supply
V _{SS}	Ground

n TRUTH TABLE

MODE	CE1	CE2	WE	OE	LB	UB	DQ0~DQ7	DQ8~DQ15	V _{CC} CURRENT
	Н	X	X	X	X	X	High Z	High Z	I _{CCSB} , I _{CCSB1}
Chip De-selected (Power Down)	Χ	L	Х	Х	Х	X	High Z	High Z	I _{CCSB} , I _{CCSB1}
	Х	X	Х	Х	Н	Н	High Z	High Z	I _{CCSB} , I _{CCSB1}
Output Disabled	L	Н	Н	Н	L	X	High Z	High Z	I _{cc}
Odipul Disabled	L	Н	Н	Н	X	L	High Z	High Z	Icc
					L	L	D _{OUT}	D _{OUT}	I _{cc}
Read	L	Н	Н	L	Н	L	High Z	D _{OUT}	I _{CC}
					L	Н	D _{OUT}	High Z	I _{cc}
					L	L	D _{IN}	D _{IN}	I _{CC}
Write	L	Н	L	Х	Н	L	Х	D _{IN}	I _{cc}
					L	Н	D _{IN}	X	Icc

NOTES: H means $V_{IH};\,L$ means $V_{IL};\,X$ means don't care (Must be V_{IH} or V_{IL} state)



n ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 ⁽²⁾ to 4.6V	V
T _{BIAS}	Temperature Under Bias	-40 to +125	οС
T_{STG}	Storage Temperature	-60 to +150	οС
P_{T}	Power Dissipation	1.0	W
l _{out}	DC Output Current	20	mA

- 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2. -2.0V in case of AC pulse width less than 30 ns

n OPERATING RANGE

RANG	AMBIENT TEMPERATURE	V _{CC}
Industrial	-40°C to + 85°C	1.65V ~ 3.6V

n CAPACITANCE $^{(1)}$ (T_A = 25°C, f = 1.0MHz)

SYMBOL	PAMAMETER	CONDITIONS	MAX.	UNITS
C _{IN}	Input Capacitance	$V_{IN} = 0V$	6	pF
C _{IO}	Input/Output Capacitance	$V_{I/O} = 0V$	8	pF

^{1.} This parameter is guaranteed and not 100% tested.

n DC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MIN.	TYP. ⁽¹⁾	MAX.	UNITS
Vcc	Power Supply			1.65		3.6	V
V _{IL}	Input Low Voltage		V _{CC} =1.8V V _{CC} =3.6V	-0.3 ⁽²⁾		0.4	V
V _{IH}	Input High Voltage		V _{CC} =1.8V V _{CC} =3.6V	1.4 2.2		V _{CC} +0.3 ⁽³⁾	٧
I _{IL}	Input Leakage Current	$\frac{V_{\text{IN}} = 0 \text{V to V}_{\text{CC}},}{\text{CE1}} = V_{\text{IH}} \text{ or CE2} = V_{\text{IL}}$				1	uA
ILO	Output Leakage Current	$V_{I/O} = 0V \text{ to } V_{CC},$ $\overline{CE1} = V_{IH} \text{ or } CE2 = V_{IL} \text{ or } \overline{OE} = V$ $\overline{UB} = \overline{LB} = V_{IH}$	_{IH} Or	-	-	1	uA
V _{OL}	Output Low Voltage	$V_{CC} = Max$, $I_{OL} = 0.2mA$ $V_{CC} = Max$, $I_{OL} = 2.0mA$	V _{CC} =1.8V V _{CC} =3.6V			0.2	V
V _{OH}	Output High Voltage	$V_{CC} = Min, I_{OH} = -0.1mA$ $V_{CC} = Min, I_{OH} = -1.0mA$	V _{CC} =1.8V V _{CC} =3.6V	V _{CC} -0.2			٧
Icc	Operating Power Supply Current	$\overline{\text{CE1}} = \text{V}_{\text{IL}} \text{ and CE2} = \text{V}_{\text{IH}},$ $\text{I}_{\text{DQ}} = \text{0mA}, \text{ f} = \text{F}_{\text{MAX}}^{(4)}$	V _{CC} =1.8V V _{CC} =3.6V		6 8	8 12	mA
I _{CC1}	Operating Power Supply Current	$\overline{CE1} = V_{IL} \text{ and } CE2 = V_{IH},$ $I_{DQ} = 0 \text{mA, } f = 1 \text{MHz}$	V _{CC} =1.8V V _{CC} =3.6V		1.0	1.5 2.0	mA
I _{CCSB}	Standby Current – TTL	$\overline{CE1} = V_{IH}, \text{ or } CE2 = V_{IL}, \\ I_{DQ} = 0mA$	V _{CC} =1.8V V _{CC} =3.6V			0.5	mA
I _{CCSB1}	Standby Current – CMOS	$\label{eq:center_constraint} \begin{split} \overline{\text{CE1}} & \! \geq \! V_{\text{CC}} \text{-} 0.2 \text{V or CE2} \! \leq \! 0.2 \text{V}, \\ V_{\text{IN}} \! \geq \! V_{\text{CC}} \text{-} 0.2 \text{V or } V_{\text{IN}} \! \leq \! 0.2 \text{V} \end{split}$	V _{CC} =1.8V V _{CC} =3.6V		2.0 2.5 ⁽⁵⁾	12 15	uA

^{1.} Typical characteristics are at $T_A \!\!=\!\! 25^{\text{O}}\text{C}$ and not 100% tested.

^{2.} Undershoot: -1.0V in case of pulse width less than 20 ns.

^{3.} Overshoot: V_{CC} +1.0V in case of pulse width less than 20 ns.

^{4.} F_{MAX}=1/t_{RC.}

^{5.} V_{CC}=3.0V

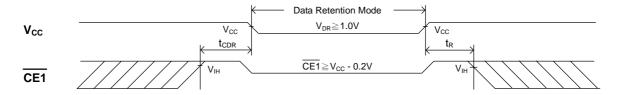


n DATA RETENTION CHARACTERISTICS (T_A = -40°C to +85°C)

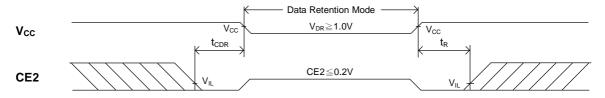
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. (1)	MAX.	UNITS
\mathbf{V}_{DR}	V _{CC} for Data Retention	$\label{eq:central_control_control} \overline{\text{CE1}} \! \ge \! V_{\text{CC}} \! - \! 0.2 \text{V or CE2} \! \le \! 0.2 \text{V}, \\ V_{\text{IN}} \! \ge \! V_{\text{CC}} \! - \! 0.2 \text{V or V}_{\text{IN}} \! \le \! 0.2 \text{V}$		1.0		1	V
I _{CCDR}	Data Retention Current	$\overline{\text{CE1}} \geqq V_{\text{CC}}\text{-}0.2 \text{V or CE2} \leqq 0.2 \text{V}, \\ V_{\text{IN}} \geqq V_{\text{CC}}\text{-}0.2 \text{V or } V_{\text{IN}} \leqq 0.2 \text{V}$	V _{CC} =1.2V		1.2	7.0	uA
t _{CDR}	Chip Deselect to Data Retention Time	Con Detection Way of our		0		1	ns
t _R	Operation Recovery Time	See Retention Waveform		t _{RC} (2)		-	ns

^{1.} Typical characteristics are at T_A=25°C and not 100% tested.

n LOW V_{CC} DATA RETENTION WAVEFORM (1) (CE1 Controlled)



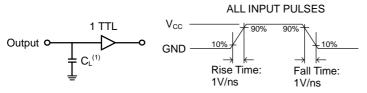
n LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)



n AC TEST CONDITIONS

(Test Load and Input/Output Reference)

Input Pulse Le	V _{CC} / 0V		
Input Rise and	1V/ns		
Input and Outp Reference Lev		0.5Vcc	
Output Load	$t_{\text{CLZ1}},t_{\text{CLZ2}},t_{\text{BE}},t_{\text{OLZ}},t_{\text{CHZ1}},\ t_{\text{CHZ2}},t_{\text{BDO}},t_{\text{OHZ}},t_{\text{WHZ}},t_{\text{OW}}$	$C_L = 5pF+1TTL$	
	Others	$C_L = 30pF+1TTL$	



^{1.} Including jig and scope capacitance.

n KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM "H" TO "L"	WILL BE CHANGE FROM "H" TO "L"
	MAY CHANGE FROM "L" TO "H"	WILL BE CHANGE FROM "L" TO "H"
	DON'T CARE ANY CHANGE PERMITTED	CHANGE : STATE UNKNOW
\longrightarrow	DOES NOT APPLY	CENTER LINE IS HIGH INPEDANCE "OFF" STATE

^{2.} t_{RC} = Read Cycle Time.



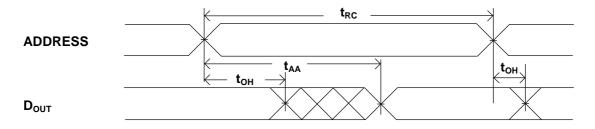
n AC ELECTRICAL CHARACTERISTICS ($T_A = -40^{\circ}$ C to +85°C)

READ CYCLE

JEDEC PARAMETER	PARANETER	DECODINE		CYC	LE TIME :	55ns	UNITS
NAME NAME	NAME	DESCRIPTION		MIN.	TYP.	TYP. MAX.	
t _{AVAX}	t _{RC}	Read Cycle Time		55			ns
t _{AVQX}	t _{AA}	Address Access Time				55	ns
t _{E1LQV}	t _{ACS1}	Chip Select Access Time	(CE1)			55	ns
t _{E2LQV}	t _{ACS2}	Chip Select Access Time	(CE2)			55	ns
t _{BLQV}	t _{BA}	Data Byte Control Access Time	(LB, UB)			55	ns
t _{GLQV}	t _{OE}	Output Enable to Output Valid				30	ns
t _{E1LQX}	t _{CLZ1}	Chip Select to Output Low Z	(CE1)	10			ns
t _{E2LQX}	t _{CLZ2}	Chip Select to Output Low Z	(CE2)	10			ns
t _{BLQX}	t _{BE}	Data Byte Control to Output Low Z	(LB, UB)	10			ns
t _{GLQX}	t _{OLZ}	Output Enable to Output Low Z		5			ns
t _{E1HQZ}	t _{CHZ1}	Chip Select to Output High Z	(CE1)			25	ns
t _{E2HQZ}	t _{CHZ2}	Chip Select to Output High Z	(CE2)			25	ns
t _{BHQZ}	t _{BDO}	Data Byte Control to Output High Z	(LB, UB)			25	ns
t _{GHQZ}	t _{OHZ}	Output Enable to Output High Z				25	ns
t _{AVQX}	t _{OH}	Data Hold from Address Change		10			ns

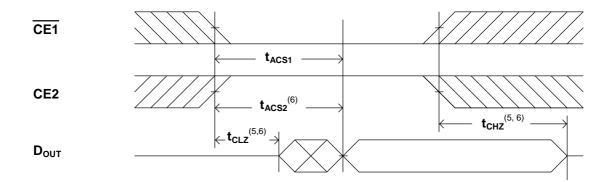
n SWITCHING WAVEFORMS (READ CYCLE)

READ CYCLE 1 (1,2,4)

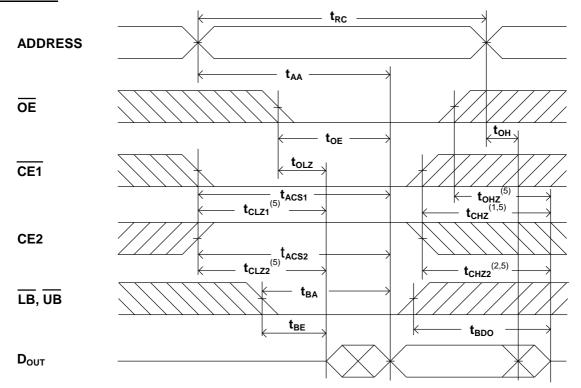




READ CYCLE 2 (1,3,4)



READ CYCLE 3 (1, 4)



NOTES:

- 1. $\overline{\text{WE}}$ is high in read Cycle.
- 2. Device is continuously selected when $\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$.
- 3. Address valid prior to or coincident with CE1 transition low and/or CE2 transition high.
- 4. $\overline{OE} = V_{IL}$.
- 5. Transition is measured \pm 500mV from steady state with C_L = 5pF. The parameter is guaranteed but not 100% tested.

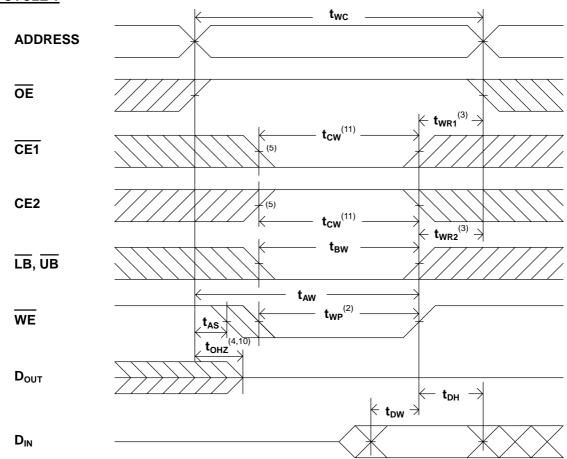


n AC ELECTRICAL CHARACTERISTICS ($T_A = -40^{\circ}$ C to +85°C) WRITE CYCLE

JEDEC	PARANETER	DESCRIPTION		CYC	LE TIME : 5	55ns	UNITS
PARAMETER NAME	NAME	MIN. TYP. MAX.		ONITS			
t _{AVAX}	twc	Write Cycle Time		55			ns
t _{AVWL}	t _{AS}	Address Set up Time		0			ns
t _{AVWH}	t _{AW}	Address Valid to End of Write		45			ns
t _{ELWH}	t _{CW}	Chip Select to End of Write		45			ns
t _{BLWH}	t _{BW}	Data Byte Control to End of Write	(LB, UB)	45			ns
t _{WLWH}	t _{WP}	Write Pulse Width		35			ns
t _{WHAX}	t _{WR1}	Write Recovery Time	(CE1, WE)	0			ns
t _{E2LAX}	t _{WR2}	Write Recovery Time	(CE2)	0			ns
t _{WLQZ}	t _{WHZ}	Write to Output High Z				20	ns
t _{DVWH}	t _{DW}	Data to Write Time Overlap		25			ns
t _{WHDX}	t _{DH}	Data Hold from Write Time		0			ns
t _{GHQZ}	t _{oHZ}	Output Disable to Output in High Z				25	ns
twhqx	tow	End of Write to Output Active		5			ns

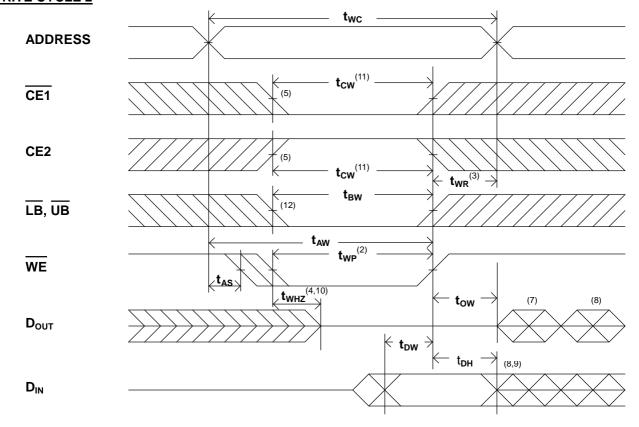
n SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1 (1)





WRITE CYCLE 2 (1,6)

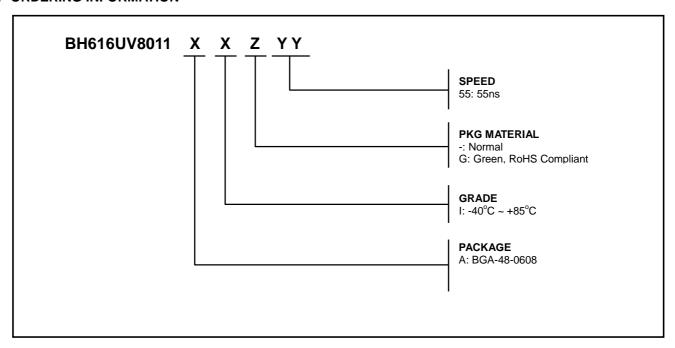


NOTES:

- 1. WE must be high during address transitions.
- The internal write time of the memory is defined by the overlap of CE1 and CE2 active and WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
- t_{WR} is measured from the earlier of CE1 or WE going high or CE2 going low at the end of write cycle.
- 4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
- If the CE1 low transition or the CE2 high transition occurs simultaneously with the WE low transitions or after the WE transition, output remain in a high impedance state.
- 6. \overline{OE} is continuously low ($\overline{OE} = V_{IL}$).
- 7. D_{OUT} is the same phase of write data of this write cycle.
- 8. D_{OUT} is the read data of next address.
- 9. If CE1 is low and CE2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
- 10.Transition is measured \pm 500mV from steady state with C_L = 5pF.
 - The parameter is guaranteed but not 100% tested.
- 11. t_{CW} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of write.

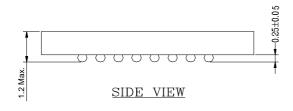


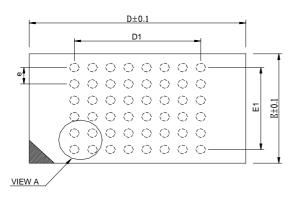
n ORDERING INFORMATION



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n PACKAGE DIMENSIONS



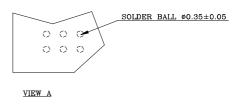


TOP VIEW

NOTES:

- 1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
- 2: PIN#1 DOT MARKING BY LASER OR PAD PRINT. 3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

BALL PITCH e = 0.75					
D	E	N	D1	E1	
8.0	6.0	48	5.25	3.75	



48 mini-BGA (6 x 8)



n Revision History

Revision No.	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
1.0	Initial Production Version	May 10,2006	Initial
1.1	Change I-grade operation temperature range - from -25°C to -40°C	May. 25, 2006	