wolfson microelectronics

WM8956

Hi-Fi DAC with 1W Stereo Class D Speaker Drivers and Headphone Drivers

DESCRIPTION

The WM8956 is a low power, high quality stereo DAC designed for portable multimedia applications.

Stereo class D speaker drivers provide 1W per channel into 8Ω loads with a 5V supply. Low leakage, excellent PSRR and pop/click suppression mechanisms also allow direct battery connection to the speaker supply. Flexible speaker boost settings allow speaker output power to be maximised while minimising other analogue supply currents.

A highly flexible input configuration for up to three stereo sources is integrated, with a complete microphone interface. External component requirements are drastically reduced as no separate microphone, speaker or headphone amplifiers are required.

Stereo 24-bit sigma-delta DACs are used with low power over-sampling digital interpolation filters and a flexible digital audio interface.

The master clock can be input directly or generated internally by an onboard PLL, supporting most commonly-used clocking schemes.

The WM8956 operates at analogue supply voltages down to 2.7V, although the digital supplies can operate at voltages down to 1.71V to save power. The speaker supply can operate at up to 5.5V, providing 1W per channel into 8Ω loads. Unused functions can be disabled using software control to save power.

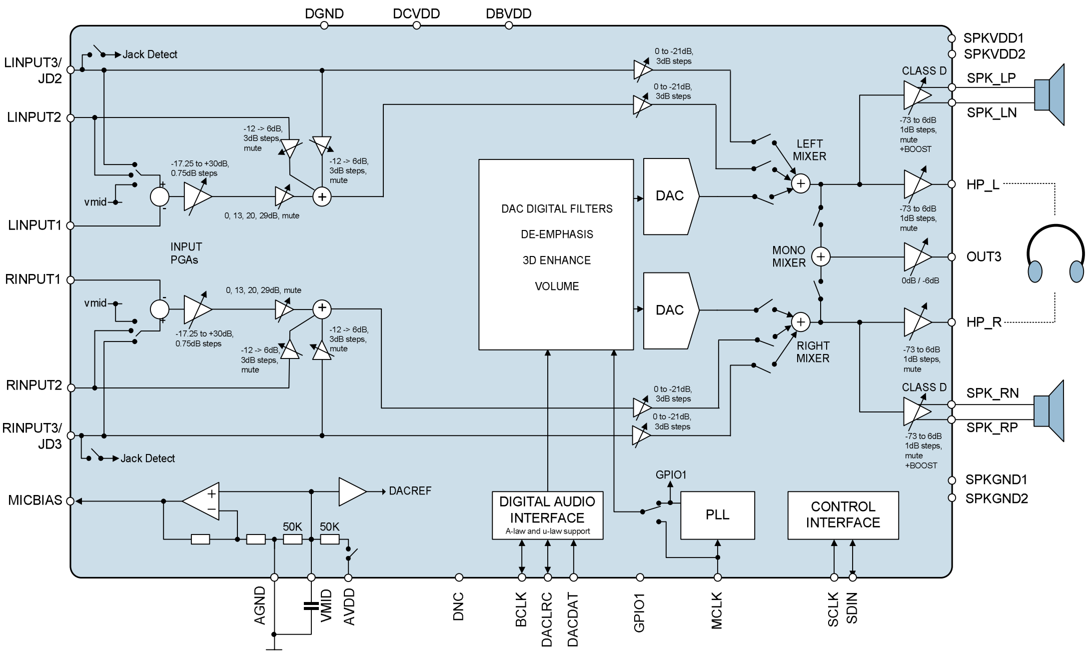
The WM8956 is supplied in a very small and thin 5x5mm QFN package, ideal for use in hand-held and portable systems.

FEATURES

- DAC SNR 99dB ('A' weighted), THD -87dB at 48kHz, 3.3V
- Pop and click suppression
- 3D Enhancement
- Stereo Class D Speaker Driver
  - <0.1% THD with 1W per channel into 8Ω BTL speakers
  - 70dB PSRR @217Hz
  - 87% efficiency (1W output)
  - Flexible internal switching clock
- On-chip Headphone Driver
  - 40mW output power into 16Ω at 3.3V
  - Capless mode support
  - THD+N -70dB at 20mW, SNR 99dB with 16Ω load
- Microphone Interface
  - Pseudo differential for high noise immunity
  - Integrated low noise MICBIAS
- Low Power Consumption
  - 16mW headphone playback (2.7V / 1.8V supplies)
- Low Supply Voltages
  - Analogue 2.7V to 3.6V (Speaker supply up to 5.5V)
  - Digital core and I/O: 1.71V to 3.6V
- On-chip PLL provides flexible clocking scheme
- Sample rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48
- 5x5x0.9mm QFN package

APPLICATIONS

- Mobile multimedia
- Portable media / DVD players
- Games consoles



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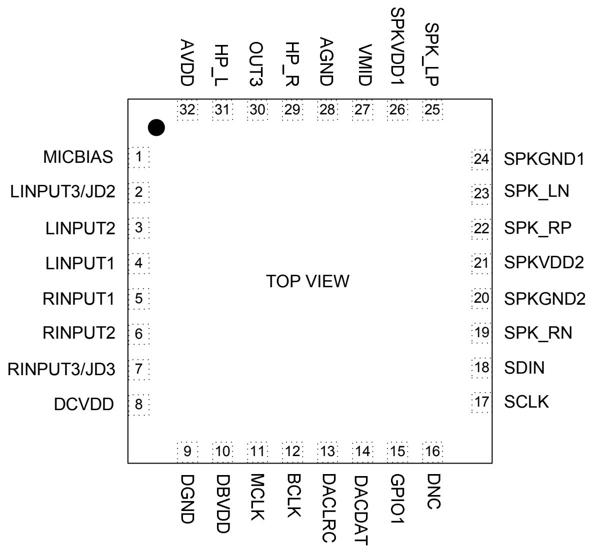
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8956GEFL/V	-40°C to +85°C	32-lead QFN (5x5x0.9mm) (Pb-free)	MSL3	260°C
WM8956GEFL/RV	-40°C to +85°C	32-lead QFN (5x5x0.9mm) (Pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 3500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	MICBIAS	Analogue Output	Microphone bias
2	LINPUT3 / JD2	Analogue Input	Left channel line input / Left channel positive differential MIC input / Jack detect input pin
3	LINPUT2	Analogue Input	Left channel line input / Left channel positive differential MIC input
4	LINPUT1	Analogue Input	Left channel single-ended MIC input / Left channel negative differential MIC input
5	RINPUT1	Analogue Input	Right channel single-ended MIC input / Right channel negative differential MIC input
6	RINPUT2	Analogue Input	Right channel line input / Right channel positive differential MIC input
7	RINPUT3 / JD3	Analogue Input	Right channel line input / Right channel positive differential MIC input / Jack detect input pin
8	DCVDD	Supply	Digital core supply
9	DGND	Supply	Digital ground (Return path for both DCVDD and DBVDD)
10	DBVDD	Supply	Digital buffer (I/O) supply
11	MCLK	Digital Input	Master clock
12	BCLK	Digital Input / Output	Audio interface bit clock
13	DACLRC	Digital Input / Output	Audio interface DAC left / right clock
14	DACDAT	Digital Input	DAC digital audio data
15	GPIO1	Digital Input / Output	GPIO1 pin
16	DNC	Do not connect	Leave this pin floating
17	SCLK	Digital Input	Control interface clock input
18	SDIN	Digital Input/Output	Control interface data input / 2-wire acknowledge output
19	SPK_RN	Analogue Output	Right speaker negative output
20	SPKGND2	Supply	Ground for speaker drivers 2
21	SPKVDD2	Supply	Supply for speaker drivers 2
22	SPK_RP	Analogue Output	Right speaker positive output
23	SPK_LN	Analogue Output	Left speaker negative output
24	SPKGND1	Supply	Ground for speaker drivers 1
25	SPK_LP	Analogue Output	Left speaker positive output
26	SPKVDD1	Supply	Supply for speaker drivers 1
27	VMID	Analogue Output	Midrail voltage decoupling capacitor
28	AGND	Supply	Analogue ground (Return path for AVDD)
29	HP_R	Analogue Output	Right output (Line or headphone)
30	OUT3	Analogue Output	Mono, left, right or buffered midrail output for capless mode
31	HP_L	Analogue Output	Left output (Line or headphone)
32	AVDD	Supply	Analogue supply
33	GND_PADDLE		Die Paddle (Note 1)

Note:

1. It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB.
2. Refer to the application note WAN_0118 on “Guidelines on How to Use QFN Packages and Create Associated PCB Footprints”

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (excluding SPKVDD1 and SPKVDD2)	-0.3V	+4.5V
SPKVDD1, SPKVDD2	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-40°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes

1. Analogue, digital and speaker grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other (i.e. not internally connected).
3. DCVDD must be less than or equal to AVDD and DBVDD.
4. AVDD must be less than or equal to SPKVDD1 and SPKVDD2.
5. SPKVDD1 and SPKVDD2 must be high enough to support the peak output voltage when using DCGAIN and ACGAIN functions, to avoid output waveform clipping. Peak output voltage is AVDD*(DCGAIN+ACGAIN)/2.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.71		3.6	V
Digital supply range (Buffer)	DBVDD	1.71		3.6	V
Analogue supplies range	AVDD	2.7		3.6	V
Speaker supply range	SPKVDD1, SPKVDD2	2.7		5.5	V
Ground	DGND, AGND, SPKGND1, SPKGND2		0		V

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (LINPUT1, RINPUT1, LINPUT2, LINPUT3, RINPUT2, RINPUT3)						
Full-scale Input Signal Level – note this changes in proportion to AVDD	V_{INFS}	L/RINPUT1,2,3 Single-ended		1.0 0		Vrms dBV
		L/RINPUT1/2 or L/RINPUT1/3 Full Differential MIC		0.5 -6		Vrms dBV
		L/RINPUT2 or L/RINPUT3 Pseudo Differential MIC		1.0 0		Vrms dBV
Mic PGA equivalent input noise		0 to 20kHz, +30dB gain		150		uV
Input resistance (Note that input boost and bypass path resistances will be seen in parallel with PGA input resistance when these paths are enabled)	L/R_{INPUT1}	+30dB PGA gain Differential or single-ended MIC configuration		3		kΩ
	L/R_{INPUT1}	0dB PGA gain Differential or single-ended MIC configuration		49		kΩ
	L/R_{INPUT1}	-17.25dB PGA gain Differential or single-ended MIC configuration		87		kΩ
	L/R_{INPUT2}, L/R_{INPUT3}	(Constant for all gains) Differential MIC configuration		85		kΩ
	L/R_{INPUT2}, L/R_{INPUT3}	Max boost gain L/RINPUT2/3 to boost		7.5		kΩ
	L/R_{INPUT2}, L/R_{INPUT3}	0dB boost gain L/RINPUT2/3 to boost		13		kΩ
	L/R_{INPUT2}, L/R_{INPUT3}	Min boost gain L/RINPUT2/3 to boost		37		kΩ
	L/R_{INPUT3}	Max bypass gain L/RINPUT2/3 to bypass		17		kΩ
	L/R_{INPUT3}	Min bypass gain L/RINPUT2/3 to bypass		70		kΩ
Input capacitance				10		pF
MIC Programmable Gain Amplifier (PGA)						
Programmable Gain Min				-17.25		dB
Programmable Gain Max				30		dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
Mute Attenuation		LMIC2B = 0 and RMIC2B = 0		85		dB
Selectable Input Gain Boost						
Gain Boost Steps		Input from PGA		0, 13, 20, 29, MUTE		dB
		Input from L/RINPUT2 or L/RINPUT3		-12, -9, -6, -3 0, 3, 6, MUTE		dB

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (LINPUT1/2 Differential, RINPUT1/2 Differential) to Line-Out (HP_L, HP_R, OUT3 with 10kΩ / 50pF load)						
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 3.3V		99		dB
		AVDD = 2.7V		99		
Total Harmonic Distortion Plus Noise	THD+N	Full Scale Input Signal, AVDD = 3.3V		-93 0.002		dB %
		Full Scale Input Signal, AVDD = 2.7V		-94 0.002		
Analogue Inputs (LINPUT2, RINPUT2) via Boost to Line-Out (HP_L, HP_R, OUT3 with 10kΩ / 50pF load)						
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 3.3V		102		dB
		AVDD = 2.7V		102		
Total Harmonic Distortion Plus Noise	THD+N	Full Scale Input Signal, AVDD = 3.3V		-93 0.002		dB %
		Full Scale Input Signal, AVDD = 2.7V		-94 0.002		
Analogue Inputs (LINPUT3, RINPUT3) via Bypass to Line-Out (HP_L, HP_R, OUT3 with 10kΩ / 50pF load)						
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 3.3V		104		dB
		AVDD = 2.7V		104		
Total Harmonic Distortion Plus Noise	THD+N	Full Scale Input Signal, AVDD = 3.3V		-96 0.002		dB %
		Full Scale Input Signal, AVDD = 2.7V		-97 0.001		
Analogue Inputs (LINPUT1, RINPUT1, LINPUT2, RINPUT2, LINPUT3, RINPUT3) to Line-Out (HP_L, HP_R, OUT3 with 10kΩ / 50pF load)						
Channel Separation		1kHz full scale signal to HP_L/R outputs via L/RINPUT1, MIC amp (single-ended) and boost		98		dB
		1kHz full scale signal to HP_L/R outputs via L/RINPUT2 and boost		90		dB
		1kHz full scale to HP_L/R outputs via L/RINPUT3 and boost		96		dB
Boost / Bypass Separation (Quiescent LINPUT3/RINPUT3 to HP outputs via bypass)		1kHz on LINPUT2/RINPUT2 to input boost mixer via MIC PGA		90		dB
		1kHz on LINPUT1/RINPUT1 to input boost mixer via MIC PGA		90		dB
Channel Matching		1kHz signal		0.2		dB

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Headphone Outputs (HP_L, HP_R)						
0dB Full scale output voltage				AVDD/3.3		Vrms
Mute attenuation		1kHz, full scale signal		86		dB
Channel Separation		L/RINPUT3 to headphone outputs via bypass		110		dB
DAC to Line-Out (HP_L, HP_R, OUT3 with 10kΩ / 50pF load)						
Signal to Noise Ratio (A-weighted)	SNR	AVDD=3.3V		99		dB
		AVDD=2.7V		98		
Total Harmonic Distortion Plus Noise	THD+N	AVDD=3.3V		-85		dB
		AVDD=2.7V		-90		
Total Harmonic Distortion	THD	AVDD=3.3V		-87		dB
		AVDD=2.7V		-92		
Channel Separation		1kHz full scale signal		110		dB
Headphone Output (HP_L, HP_R, using capacitors unless otherwise specified)						
Output Power per channel	P_O	Output power is very closely correlated with THD; see below.				
Total Harmonic Distortion + Noise	THD+N	AVDD=2.7V, R_L=32Ω P_O=5mW		-78 0.013		dB %
		AVDD=2.7V, R_L=16Ω P_O=5mW		-75 0.018		
		AVDD=3.3V, R_L=32Ω, P_O=20mW		-72 0.025		
		AVDD=3.3V, R_L=16Ω, P_O=20mW		-70 0.032		
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 3.3V	92	99		dB
		AVDD = 2.7V		98		
Speaker Outputs (SPK_LP, SPK_LN, SPK_RP, SPK_RN with 8Ω bridge tied load)						
Output Power	P_O	Output power is very closely correlated with THD; see below				
Total Harmonic Distortion + Noise (DAC to speaker outputs)	THD+N	P_O =200mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V		-78 0.013		dB %
		P_O =320mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V		-72 0.025		dB %
		P_O =500mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V		-75 0.018		dB %
		P_O =1W, R_L = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V		-70 0.032		dB %
Total Harmonic Distortion + Noise (LINPUT3 and RINPUT3 to speaker outputs)	THD+N	P_O =200mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V		-78 0.013		dB %
		P_O =320mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V		-72 0.025		dB %
		P_O =500mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V		-75 0.018		dB %
		P_O =1W, R_L = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V		-70 0.032		dB %

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal to Noise Ratio (A-weighted) (DAC to speaker outputs)	SNR	SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V; R_L = 8Ω, ref=2.0Vrms		90		dB
		SPKVDD1=SPKVDD2 =5V; AVDD=3.3V; R_L = 8Ω, ref=2.8Vrms		92		dB
Signal to Noise Ratio (A-weighted) (LINNPUT3 and RINPUT3 to speaker outputs)	SNR	SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V; R_L = 8Ω, ref=2.0Vrms		90		dB
		SPKVDD1=SPKVDD2 =5V; AVDD=3.3V; R_L = 8Ω, ref=2.8Vrms		92		dB
Speaker Supply Leakage current	I_{SPKVDD}	SPKVDD1=SPKVDD2 =5V; All other supplies disconnected		1		uA
		SPKVDD1=SPKVDD2 =5V; All other supplies 0V		1		uA
Power Supply Rejection Ratio (100mV ripple on SPKVDD1/SPKVDD2 @217Hz)	PSRR	DAC to speaker playback		80		dB
		LINPUT3/RINPUT3 to speaker playback		80		dB
Analogue Reference Levels						
Midrail Reference Voltage	VMID		–3%	AVDD/2	+3%	V
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$	3mA load current MBSEL=1	–5%	0.9×AVDD	+ 5%	V
		3mA load current MBSEL=0	–5%	0.65×AVDD	+ 5%	V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1K to 20kHz		15		nV/√Hz
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OH}-1mA			0.1×DBVDD	V
Input capacitance				10		pF
Input leakage			-0.9		0.9	uA

OUTPUT PGA GAIN

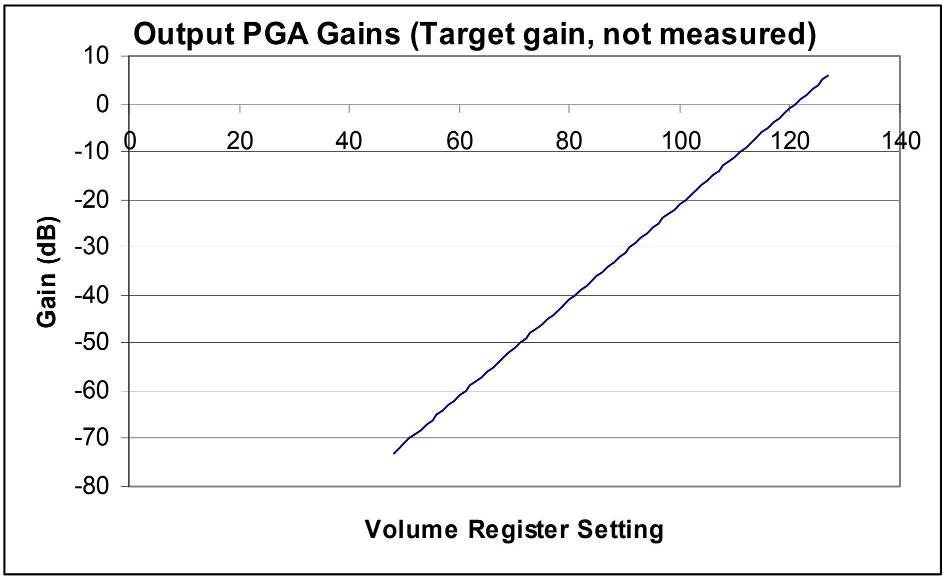


Figure 1 Output PGA Gains (LOUT1VOL, ROUT1VOL, SPKLVOL, SPKRVOL)

TYPICAL POWER CONSUMPTION

Mode	AVDD (V)	SPKVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	ISPKVDD (mA)	IDBVDD (mA)	IDCVDD (mA)	Total (mW)
Off (Default state at power-up, no clocks)	2.7	2.7	1.71	1.71	0.0314	0	0	0	0.085
	3	3	1.8	1.8	0.0326	0	0	0	0.098
	3.3	3.3	3.3	1.8	0.033	0	0	0	0.109
	3.6	5.5	3.6	3.6	0.0345	0	0	0	0.124
Off (Thermal sensor disabled, no clocks)	2.7	2.7	1.71	1.71	0.0086	0	0	0	0.023
	3	3	1.8	1.8	0.0092	0	0	0	0.028
	3.3	3.3	3.3	1.8	0.0096	0	0	0	0.032
	3.6	5.5	3.6	3.6	0.0102	0	0	0	0.037
Sleep (Thermal sensor enabled, VMID enabled using 250k VMID resistors)	2.7	2.7	1.71	1.71	0.0537	0	0	0	0.145
	3	3	1.8	1.8	0.0621	0	0	0	0.186
	3.3	3.3	3.3	1.8	0.0674	0	0	0	0.222
	3.6	5.5	3.6	3.6	0.0728	0	0	0	0.262
DAC Playback to 16Ohm headphones @44.1kHz, (no signal)	2.7	2.7	1.71	1.71	3.869	0	0.0029	3.38	16.231
	3	3	1.8	1.8	4.35	0	0.0031	3.6	19.536
	3.3	3.3	3.3	1.8	4.8	0	0.0098	3.78	22.676
	3.6	5.5	3.6	3.6	5.33	0	0.0145	9.4	53.080
DAC Playback to 16Ohm headphones @44.1kHz, (white noise 1Vrms)	2.7	2.7	1.71	1.71	19.6	0	0.003	3.6	59.081
	3	3	1.8	1.8	22.1	0	0.004	3.9	73.327
	3.3	3.3	3.3	1.8	23.8	0	0.012	3.9	85.600
	3.6	5.5	3.6	3.6	26	0	0.02	9.9	129.312
DAC Playback to 16Ohm headphones @44.1kHz, (1kHz tone 100mVrms)	2.7	2.7	1.71	1.71	7.8	0	0.003	3.5	27.050
	3	3	1.8	1.8	8.9	0	0.004	3.8	33.547
	3.3	3.3	3.3	1.8	9.6	0	0.012	3.8	38.560
	3.6	5.5	3.6	3.6	10.5	0	0.014	9.5	72.050
DAC Playback to 16Ohm headphones @44.1kHz, PLL enabled, MCLK=12MHz, no signal, master mode	2.7	2.7	1.71	1.71	4.77	0	0.23	3.7	19.599
	3	3	1.8	1.8	5.4	0	0.25	3.9	23.670
	3.3	3.3	3.3	1.8	6.04	0	0.46	3.9	28.470
	3.6	5.5	3.6	3.6	6.6	0	0.49	10.1	61.884
DAC Playback to 8Ohm speakers @44.1kHz (no signal)	2.7	2.7	1.71	1.71	5.1	1.4	0.0032	3.57	23.660
	3.3	3.3	3.3	1.8	6.3	1.79	0.01	3.84	33.642
	3.3	5	3.3	1.8	6.3	2.9	0.01	3.8	42.163
	3.3	5.5	3.3	1.8	6.9	3.2	0.0132	9.8	58.054
DAC Playback to 8Ohm speakers @44.1kHz (1kHz tone, full scale)	2.7	2.7	1.71	1.71	5.1	240	0.0032	3.57	667.880
	3.3	3.3	3.3	1.8	6.3	304	0.01	3.84	1030.935
	3.3	5	3.3	1.8	6.3	450	0.01	3.8	2277.663
	3.3	5.5	3.3	1.8	6.9	486	0.0132	9.8	2713.454
DAC Playback to 8Ohm speakers @44.1kHz (white noise, 1Vrms)	2.7	2.7	1.71	1.71	5.1	48	0.0032	3.57	149.480
	3.3	3.3	3.3	1.8	6.3	56	0.01	3.84	212.535
	3.3	5	3.3	1.8	6.3	82	0.01	3.8	437.663
	3.3	5.5	3.3	1.8	6.9	90	0.0132	9.8	535.454
DAC Playback to mono speaker @44.1kHz (1kHz tone, full scale)	2.7	2.7	1.71	1.71	3	125	0.0034	3.63	351.813
	3.3	3.3	3.3	1.8	3.77	154	0.0126	3.89	527.685
	3.3	5	3.3	1.8	3.79	229	0.0126	3.7	1164.209
	3.6	5.5	3.6	3.6	4.2	250	0.0163	9.7	1425.099

Note:

1. Power in the load is included.

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

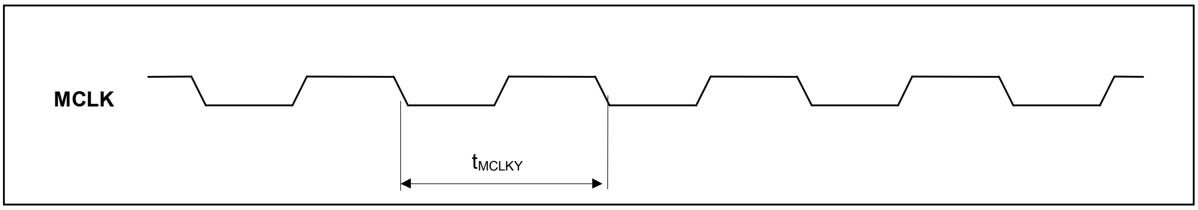


Figure 2 System Clock Timing Requirements

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V, T_A = +25^{o}C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time	T_{MCLKY}		33.33			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	

AUDIO INTERFACE TIMING – MASTER MODE

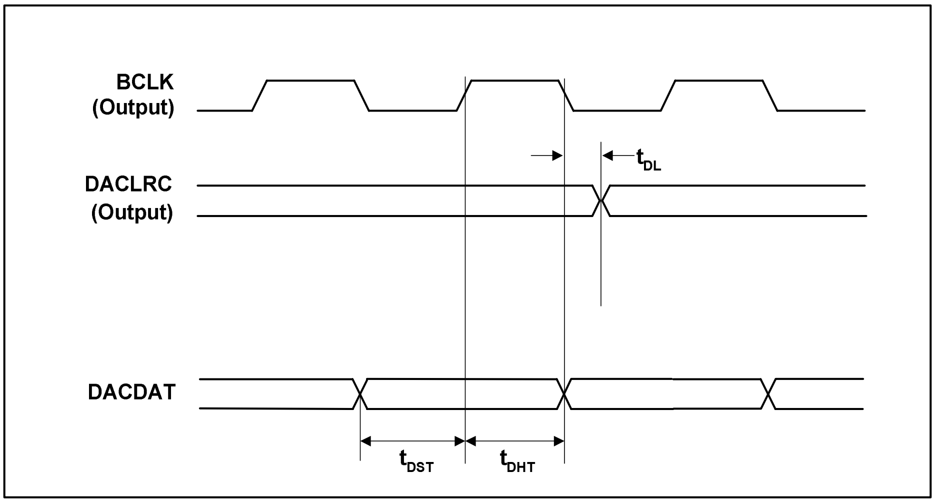


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
DACLRC propagation delay from BCLK falling edge	t_{DL}			10	ns
DACDAT setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

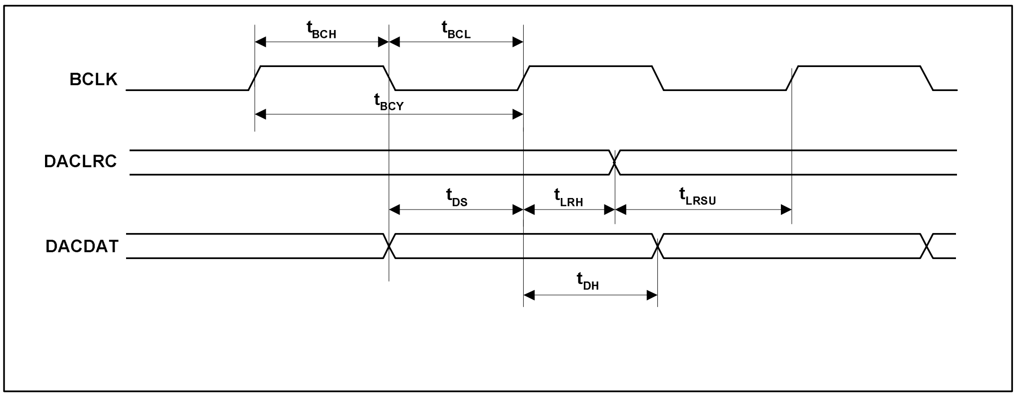


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V, T_A=+25°C, Slave Mode, fs=48kHz,
MCLK= 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
DACLRC set-up time to BCLK rising edge	t_{LRSU}	10			ns
DACLRC hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
DACDAT set-up time to BCLK rising edge	t_{DS}	10			ns

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – 2-WIRE MODE

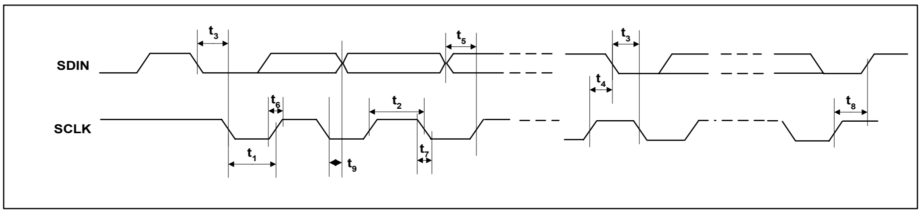


Figure 4 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency				526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

INTERNAL POWER ON RESET CIRCUIT

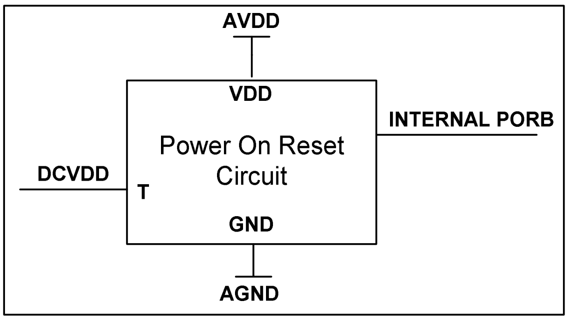


Figure 5 Internal Power on Reset Circuit Schematic

The WM8956 includes an internal Power-On-Reset Circuit, as shown in Figure 5, which is used to reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DCVDD. It asserts PORB low if AVDD or DCVDD is below a minimum threshold.

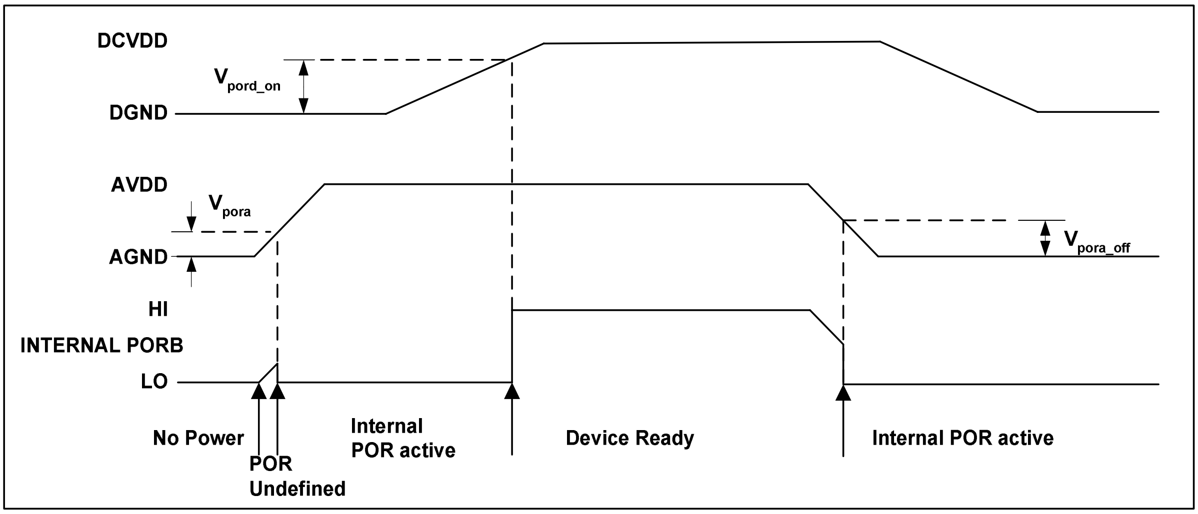


Figure 6 Typical Power up Sequence where AVDD is Powered before DCVDD

Figure 6 shows a typical power-up sequence where AVDD comes up first. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DCVDD rises to V_{pord_on} and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold V_{pora_off}.

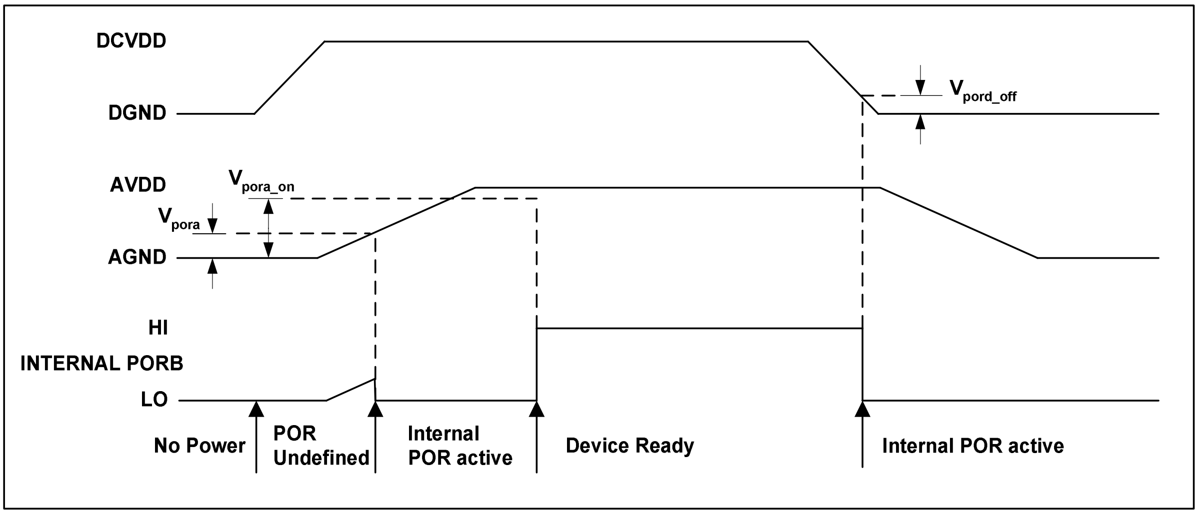


Figure 7 Typical Power up Sequence where DCVDD is Powered before AVDD

Figure 7 shows a typical power-up sequence where DCVDD comes up first. First it is assumed that DCVDD is already up to specified operating voltage. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to V_{pora_on}, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DCVDD falls first, PORB is asserted low whenever DCVDD drops below the minimum threshold V_{pord_off}.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}	0.4	0.6	0.8	V
V_{pora_on}	0.9	1.2	1.6	V
V_{pora_off}	0.4	0.6	0.8	V
V_{pord_on}	0.5	0.7	0.9	V
V_{pord_off}	0.4	0.6	0.8	V

Table 1 Typical POR Operation (typical values, not tested)

Notes:

1. If AVDD and DCVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below V_{pora_off} or V_{pord_off}) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.

2. The chip will enter reset at power down when AVDD or DCVDD falls below V_{pora_off} or V_{pord_off}. This may be important if the supply is turned on and off frequently by a power management system.

3. The minimum t_{por} period is maintained even if DCVDD and AVDD have zero rise time. This specification is guaranteed by design rather than test.

DEVICE DESCRIPTION

INTRODUCTION

The WM8956 is a low power audio DAC offering a combination of high quality audio, advanced features, low power and small size. These characteristics make it ideal for portable digital audio applications with stereo speaker and headphone outputs such as games consoles, portable media players and multimedia phones.

Stereo class D speaker drivers can provide 1W per channel into 8Ω loads. BTL configuration provides high power output and excellent PSRR. Low leakage and pop/click suppression mechanisms allow direct battery connection, reducing component count and power consumption in portable battery-powered applications. Highly flexible speaker boost settings provide fully internal level-shifting of analogue output signals, allowing speaker output power to be maximised while minimising other analogue supply currents, and requiring no additional components.

A flexible input configuration includes support for two stereo microphone interfaces (single-ended or pseudo-differential) and additional stereo line inputs. Up to three stereo analogue input sources are available, removing the need for external analogue switches in many applications. Boost amplifiers are available for additional gain on the microphone inputs.

The stereo DACs are of hi-fi quality using a 24-bit, low-order oversampling architecture to deliver optimum performance.

The DAC output signal can be mixed with analogue input signals from the line inputs or bypass paths. This mix is available on speaker and headphone/line outputs.

The WM8956 has a configurable digital audio interface where digital audio playback data is fed to the DAC. It supports a number of audio data formats including I^2S, DSP Mode (a burst mode in which frame sync plus two data packed words are transmitted), MSB-First, left justified and MSB-First, right justified, and can operate in master or slave modes. In PCM mode A-law and μ-law companding is supported.

The SYSCLK (system clock) provides clocking for the DACs, DSP core, class D outputs and the digital audio interface. SYSCLK can be derived directly from the MCLK pin or via an integrated PLL, providing flexibility to support a wide range of clocking schemes. All MCLK frequencies typically used in portable systems are supported for sample rates between 8kHz and 48kHz. A flexible switching clock for the class D speaker drivers (synchronous with the audio DSP clocks for best performance) is also derived from SYSCLK.

To allow full software control over all its features, the WM8956 uses a 2 wire control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled via software to save power, while low leakage currents extend standby and off time in portable battery-powered applications.

INPUT SIGNAL PATH

The WM8956 has three flexible stereo analogue input channels which can be configured as line inputs, differential microphone inputs or single-ended microphone inputs. Line inputs and microphone PGA outputs can be routed directly to the output mixers via a bypass path.

MICROPHONE INPUTS

Differential microphones can be connected between LINPUT1 and LINPUT2 or LINPUT3, and between RINPUT1 and RINPUT2 or RINPUT3. Alternatively single-ended microphones can be connected to LINPUT1 or RINPUT1.

In single-ended microphone input configuration the microphone signal should be input to LINPUT1 or RINPUT1 and the internal non-inverting input of the input PGA should be switched to VMID.

In differential mode the larger signal should be input to LINPUT2 or LINPUT3 on the left channel, or RINPUT2 or RINPUT3 on the right channel. The smaller (e.g. noisy ground connection) should be input to LINPUT1 or RINPUT1.

The gain of the microphone PGAs is controlled directly via software.

The inputs LINPUT2, RINPUT2, LINPUT3 and RINPUT3 should not be connected to the boost mixer or bypass path while operating as the non-inverting input in differential microphone configuration.

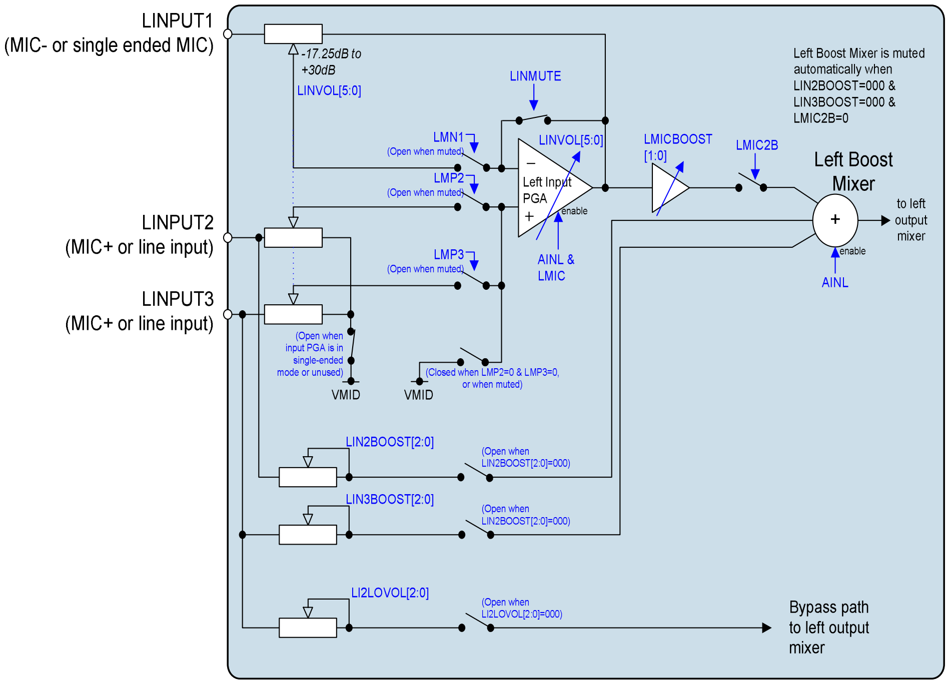


Figure 8 Analogue Left Input Equivalent Circuit

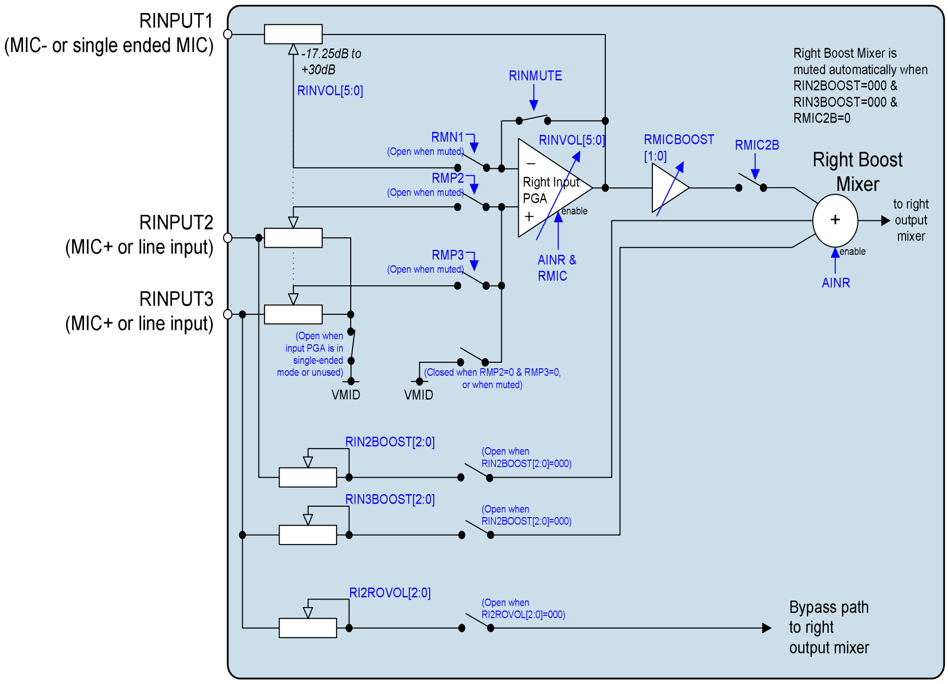


Figure 9 Analogue Right Input Equivalent Circuit

The input PGAs and boost mixers are enabled by the AINL and AINR register bits. The microphone PGAs can be also be disabled independently of the boost mixer to save power, using LMIC and RMIC register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power Management (1)	5	AINL	0	Left channel input PGA and boost stage enable 0 = PGA disabled, boost disabled 1 = PGA enabled (if LMIC = 1), boost enabled
	4	AINR	0	Right channel input PGA and boost stage enable 0 = PGA disabled, boost disabled 1 = PGA enabled (if LMIC = 1), boost enabled
R47 (2Fh) Power Management (3)	5	LMIC	0	Left channel input PGA enable 0 = PGA disabled 1 = PGA enabled (if AINL = 1)
	4	RMIC	0	Right channel input PGA enable 0 = PGA disabled 1 = PGA enabled (if AINR = 1)

Table 2 Input PGA and Boost Enable Register Settings

The input PGAs can be configured as differential inputs, using LINPUT1/LINPUT2 or LINPUT1/LINPUT3, and RINPUT1/RINPUT2 or RINPUT1/RINPUT3. The input impedance to these non-inverting inputs is constant in this configuration. Differential configuration is controlled by LMP2, LMP3, RMP2 and RMP3 as shown in Table 3.

When single-ended configuration is selected, the non-inverting input of the PGA is connected to VMID.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) Left Input Signal Path	3	LMIC2B	0	Connect Left Input PGA to Left Input Boost mixer 0 = Not connected 1 = Connected
	6	LMP2	0	Connect LINPUT2 to non-inverting input of Left Input PGA 0 = LINPUT2 not connected to PGA 1 = LINPUT2 connected to PGA (Constant input impedance)
	7	LMP3	0	Connect LINPUT3 to non-inverting input of Left Input PGA 0 = LINPUT3 not connected to PGA 1 = LINPUT3 connected to PGA (Constant input impedance)
	8	LMN1	1	Connect LINPUT1 to inverting input of Left Input PGA 0 = LINPUT1 not connected to PGA 1 = LINPUT1 connected to PGA
R33 (21h) Right Input Signal Path	3	RMIC2B	0	Connect Right Input PGA to Right Input Boost mixer 0 = Not connected 1 = Connected
	6	RMP2	0	Connect RINPUT2 to non-inverting input of Right Input PGA 0 = RINPUT2 not connected to PGA 1 = RINPUT2 connected to PGA (Constant input impedance)

	7	RMP3	0	Connect RINPUT3 to non-inverting input of Right Input PGA 0 = RINPUT3 not connected to PGA 1 = RINPUT3 connected to PGA (Constant input impedance)
	8	RMN1	1	Connect RINPUT1 to inverting input of Right Input PGA 0 = RINPUT1 not connected to PGA 1 = RINPUT1 connected to PGA

Table 3 Input PGA Control

INPUT PGA VOLUME CONTROLS

The input PGAs have a gain range from -17.25dB to +30dB in 0.75dB steps. The gains from the inverting inputs (LINPUT1 and RINPUT1) to the PGA outputs and from the non-inverting inputs (LINPUT2/RINPUT2 and LINPUT3/RINPUT3) to the PGA output are always common in differential configuration and controlled by the register bits LINVOL[5:0] and RINVOL[5:0].

The left and right input PGAs can be independently muted using the LINMUTE and RINMUTE register bits.

To allow simultaneous volume updates of left and right channels, PGA gains are not altered until a 1 is written to the IPVU bit.

To prevent "zipper noise", a zero-cross function is provided, so that when enabled, volume updates will not take place until a zero-crossing is detected. In the event of a long period without zero-crossings, a timeout function is available. When this function is enabled (using the TOEN register bit), the volume will update automatically after a timeout. The timeout period is set by TOCLKSEL. Note that an MCLK must be input to the device and SYSCLK running internally to use the timeout function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Left Channel PGA	8	IPVU	0	Input PGA Volume Update 0 = Store LINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LINVOL, right = intermediate latch)
	7	LINMUTE	1	Left Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.
	6	LIZC	0	Left Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	LINVOL [5:0]	010111 (0dB)	Left Input PGA Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R1 (01h) Right Channel PGA	8	IPVU	0	Input PGA Volume Update 0 = Store RINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (right = RINVOL, left = intermediate latch)

	7	RINMUTE	1	Right Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.
	6	RIZC	0	Right Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	RINVOL [5:0]	010111 (0dB)	Right Input PGA Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R23 (17h) Additional Control (1)	0	TOEN	0	Timeout Enable (Also enables jack detect debounce clock) 0 = Timeout disabled 1 = Timeout enabled
	1	TOCLKSEL	0	Slow Clock Selection (Used for volume update timeouts and for jack detect debounce) 0 = SYSCLK / 2^{21} (Slower Response) 1 = SYSCLK / 2^{19} (Faster Response)

Table 4 Input PGA Volume Control

See "Volume Updates" for more information on volume update bits, zero cross and timeout operation.

LINE INPUTS

Two pairs of stereo line inputs (LINPUT2 / RINPUT2 and LINPUT3 / RINPUT3) are available as analogue inputs into the output mixers via the bypass paths.

See "Output Signal Path" for more information on the bypass paths.

INPUT BOOST

The boost stage in the input path can mix signals from the microphone PGAs and the line inputs.

The boost stage can provide up to +29dB additional gain from the microphone PGA output, providing a total maximum available analogue gain of +59dB from microphone to output mixers. The microphone PGA path to the boost mixer is muted using LINMUTE and RINMUTE as shown in Table 4. Microphone PGA to boost gain settings are shown in Table 5.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) Left Input Signal Path	5:4	LMICBOOST [1:0]	00	Left Channel Input PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB
R33 (21h) Right Input Signal Path	5:4	RMICBOOST [1:0]	00	Right Channel Input PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB

Table 5 Microphone PGA Boost Control

For line inputs, -12dB to +6dB gain is available on the boost mixer, with mute control, as shown in Table 6.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R43 (2Bh) Input Boost Mixer 1	6:4	LIN3BOOST [2:0]	000	LINPUT3 to Boost Mixer gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB
	3:1	LIN2BOOST [2:0]	000	LINPUT2 to Boost Mixer gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB
R44 (2Ch) Input Boost Mixer 2	6:4	RIN3BOOST [2:0]	000	RINPUT3 to Boost Mixer gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB
	3:1	RIN2BOOST [2:0]	000	RINPUT2 to Boost Mixer gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB

Table 6 Line Input Boost Control

When all three input paths to the boost mixer are disabled, the boost mixer will automatically be muted.

MICROPHONE BIASING CIRCUIT

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be altered via the MBSEL register bit. When MBSEL=0, MICBIAS=0.9*AVDD and when MBSEL=1, MICBIAS=0.65*AVDD. The output can be enabled or disabled using the MICB control bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power management (1)	1	MICB	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON
R48 (30h) Additional Control (4)	0	MBSEL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD

Table 7 Microphone Bias Control

The internal MICBIAS circuitry is shown in Figure 10. The maximum source current capability for MICBIAS is 3mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 3mA.

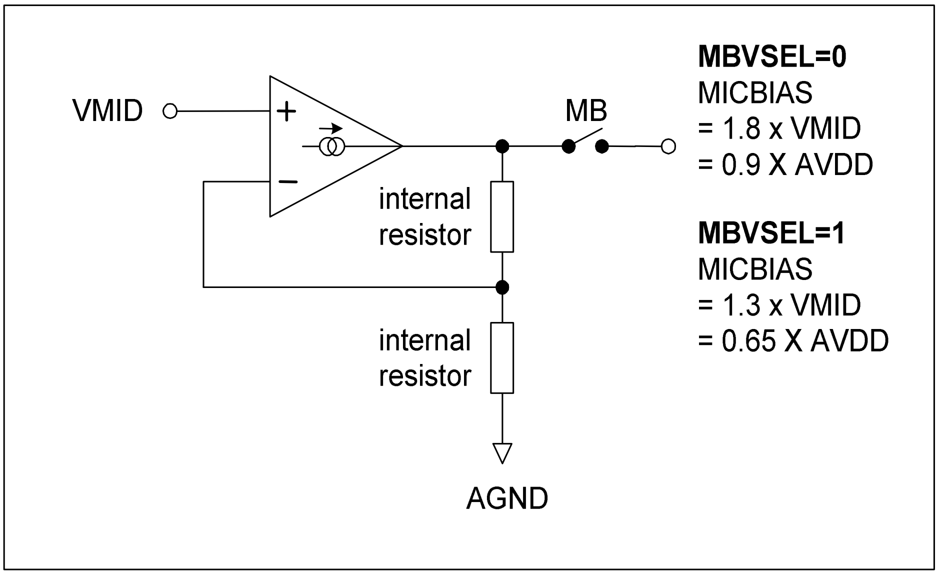
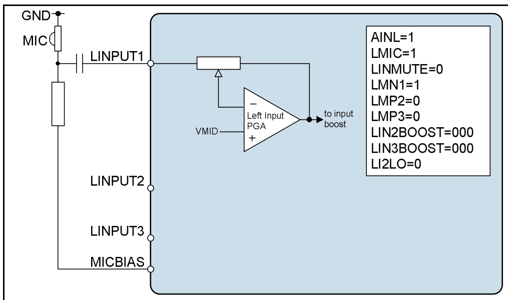
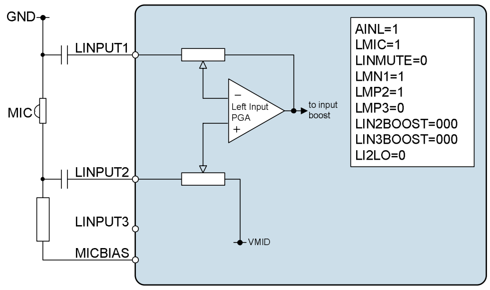


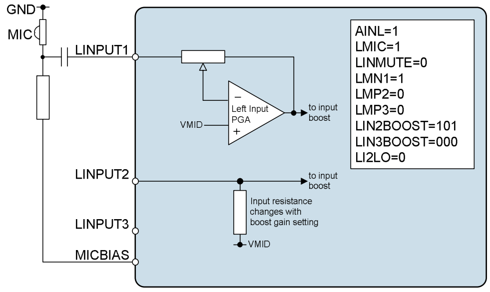
Figure 10 Microphone Bias Schematic

EXAMPLE INPUT CONFIGURATIONS

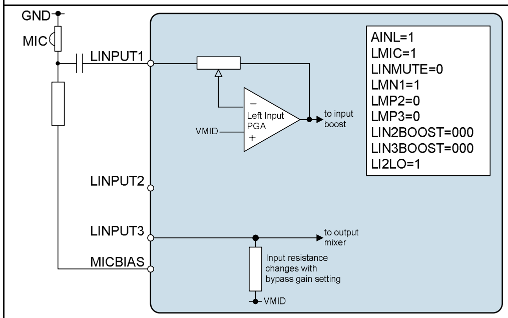
Some example input configurations are shown below.

<table>
<tr><td>
</td><td>Single-ended MIC configuration on left channel.

LINPUT2 and LINPUT3 unused</td></tr>
<tr><td>
</td><td>Pseudo-differential MIC configuration on left channel using LINPUT1 as ground connection and LINPUT2 as signal input.

LINPUT3 unused.</td></tr>
<tr><td>
</td><td>Single-ended MIC configuration on left channel.

LINPUT2 used as additional input to boost stage.

LINPUT3 unused.</td></tr>
<tr><td>
</td><td>Single-ended MIC configuration on left channel.

LINPUT3 used as input to bypass path.

LINPUT2 unused.</td></tr>
</table>

Figure 11 Example Microphone Input Configurations (See also "Recommended External Components")

OUTPUT SIGNAL PATH

The hi-fi DACs and DAC digital filters are enabled by register bits DACL and DACR. The mixers and output drivers can be separately enabled by individual control bits (see Analogue Outputs). Thus it is possible to utilise the analogue mixing and amplification provided by the WM8956, irrespective of whether the DACs are enabled or not.

The WM8956 DACs receive digital input data on the DACDAT pin. The digital filter block processes the data to provide the following functions:

- Digital volume control with soft mute and soft un-mute
- Mono mix
- 3D stereo enhancement
- De-emphasis
- Sigma-delta modulation

High performance sigma-delta 24-bit audio DAC converts the digital data into an analogue signal.

The analogue outputs from the DACs can then be mixed with the analogue line inputs. This mix is fed to the output drivers for headphone or speaker output. OUT3 can provide a mono mix of left and right mixers or a pseudo-ground for capless headphone drive.

DIGITAL PLAYBACK (DAC) PATH

Digital data is passed to the WM8956 via the flexible audio interface to the hi-fi DACs. The DACs are enabled by the DACL and DACR register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) Power Management (2)	8	DACL	0	Left Channel DAC Enable 0 = DAC disabled 1 = DAC enabled
	7	DACR	0	Right Channel DAC Enable 0 = DAC disabled 1 = DAC enabled

Table 8 DAC Enable Control

DIGITAL DAC VOLUME CONTROL

The signal volume from each DAC can be controlled digitally. The gain and attenuation range is –127dB to 0dB in 0.5dB steps. The level of attenuation for an eight-bit code X is given by:

$0.5 \times (X\text{-}255)$ dB for $1 \leq X \leq 255$; MUTE for $X = 0$

The DACVU control bit controls the loading of digital volume control data. When DACVU is set to 0, the LDACVOL or RDACVOL control data is loaded into an intermediate register, but the actual gain does not change. Both left and right gain settings are updated simultaneously when DACVU is set to 1.

See "Volume Updates" for more information on volume update bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) Left Channel Digital Volume	8	DACVU	0	DAC Volume Update 0 = Store LDACVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LDACVOL, right = intermediate latch)
	7:0	LDACVOL [7:0]	11111111 (0dB)	Left DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB
R11 (0Bh) Right Channel Digital Volume	8	DACVU	0	DAC Volume Update 0 = Store RDACVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RDACVOL)
	7:0	RDACVOL [7:0]	11111111 (0dB)	Right DAC Digital Volume Control similar to LDACVOL

Table 9 Digital Volume Control

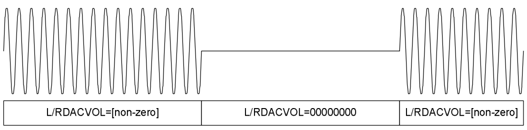
DAC SOFT MUTE AND SOFT UN-MUTE

The WM8956 also has a soft mute function, which, when enabled, gradually attenuates the volume of the digital signal to zero. When soft mute is disabled, the gain will either gradually ramp back up to the digital gain setting, or return instantly to the digital gain setting, depending on the DACSMM register bit.

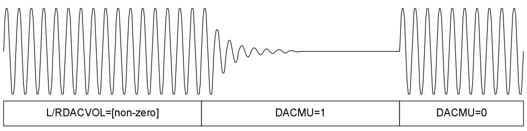
The DAC is soft-muted by default. To play back an audio signal, this function must first be disabled by setting the DACMU bit to zero.

DACSMM would typically be enabled when using soft mute during playback of audio data so that when soft mute is then disabled, the sudden volume increase will not create pop noise by jumping immediately to the previous volume level (e.g. resuming playback after pausing during a track).

DACSMM would typically be disabled when un-muting at the start of a digital music file, so that the first part of the track is not attenuated (e.g. when starting playback of a new track, or resuming playback after pausing between tracks).

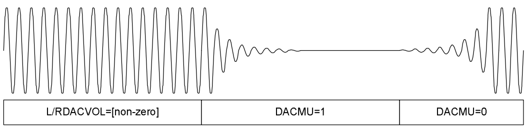


DAC muting and un-muting using volume control bits LDACVOL and RDACVOL.



DAC muting and un-muting using soft mute bit DACMU.

Soft un-mute not enabled (DACSMM = 0).



DAC muting and un-muting using soft mute bit DACMU.

Soft un-mute enabled (DACSMM = 1).

Figure 12 DAC Mute Control

The volume ramp rate during soft mute and un-mute is controlled by the DACMR bit. Ramp rates of fs/32 and fs/2 are selectable as shown in Table 10 (fs = DAC sample rate).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) DAC Control (1)	3	DACMU	1	Digital Soft Mute 1 = Mute 0 = No mute (signal active)
R6 (06h) DAC Control (2)	3	DACSMM	0	DAC Soft Mute Mode 0 = Disabling soft-mute (DACMU=0) will cause the volume to change immediately to the LDACVOL / RDACVOL settings 1 = Disabling soft-mute (DACMU=0) will cause the volume to ramp up gradually to the LDACVOL / RDACVOL settings
	2	DACMR	0	DAC Soft Mute Ramp Rate 0 = Fast ramp (fs/2, providing maximum delay of 10.7ms at fs=48k) 1 = Slow ramp (fs/32, providing maximum delay of 171ms at fs=48k)

Table 10 DAC Soft-Mute Control

DAC DE-EMPHASIS

Digital de-emphasis can be applied to the DAC playback data (e.g. when the data comes from a CD with pre-emphasis used in the recording). De-emphasis filtering is available for sample rates of 48kHz, 44.1kHz and 32kHz.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) DAC Control (1)	2:1	DEEMPH [1:0]	00	De-Emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No de-emphasis

Table 11 DAC De-Emphasis Control

DAC OUTPUT PHASE AND MONO MIXING

The digital audio data is converted to oversampled bit streams in the on-chip, true 24-bit digital interpolation filters. The bitstream data enters two multi-bit, sigma-delta DACs, which convert them to high quality analogue audio signals. The multi-bit DAC architecture reduces high frequency noise and sensitivity to clock jitter. It also uses a Dynamic Element Matching technique for high linearity and low distortion.

In normal operation, the left and right channel digital audio data is converted to analogue in two separate DACs. There is a mono-mix mode where the two audio channels are mixed together digitally and then converted to analogue using only one DAC, while the other DAC is switched off. The mono-mix signal can be selected to appear on both analogue output channels. The mono mix is automatically attenuated by 6dB to prevent clipping.

The DAC output defaults to non-inverted. Setting DACPOL[0] bit will invert the left DAC output phase and setting DACPOL[1] bit will invert the right DAC output phase.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) DAC Control (2)	6:5	DACPOL[1:0]	00	DAC Polarity Control: 00 = Polarity not inverted 01 = DAC L inverted 10 = DAC R inverted 11 = DAC L and R inverted
R23 (17h) Additional Control (1)	4	DMONOMIX	0	DAC Mono Mix 0 = Stereo 1 = Mono (Mono MIX output on enabled DACs)

Table 12 DAC Mono Mix and Phase Invert Select

3D STEREO ENHANCEMENT

The WM8956 has a digital 3D enhancement option to artificially increase the separation between the left and right channels. This effect can only be used for playback, not for record.

The 3D enhancement function is activated by the 3DEN bit, and the 3DDEPTH setting controls the degree of stereo expansion. Additionally, one of four filter characteristics can be selected for the 3D processing, using the 3DUC and 3DLC control bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 (10h) 3D enhance	6	3DUC	0	Upper Cut-Off Frequency 0 = High (Recommended for fs>=32kHz) 1 = Low (Recommended for fs<32kHz)
	5	3DLC	0	Lower Cut-Off Frequency 0 = Low (Recommended for fs>=32kHz) 1 = High (Recommended for fs<32kHz)
	4:1	3DDEPTH [3:0]	0000	3D Stereo Depth 0000 = 0% (minimum 3D effect) 0001 = 6.67% .... 1110 = 93.3% 1111 = 100% (maximum 3D effect)
	0	3DEN	0	3D Stereo Enhancement Enable 0 = Disabled 1 = Enabled

Table 13 3D Stereo Enhancement Function

When 3D enhancement is enabled it may be necessary to attenuate the signal by 6dB to avoid limiting. This is a user-selectable function, enabled by setting DACDIV2.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) DAC control (1)	7	DACDIV2	0	DAC 6dB attenuate enable 0 = disabled (0dB) 1 = -6dB enabled

Table 14 DAC 6dB Attenuation Select

OUTPUT MIXERS

Left and right analogue mixers allow the DAC output and analogue bypass paths to be mixed. Programmable attenuation and mute is available on the analogue bypass paths from LINPUT3, RINPUT3 and from the input boost mixers as shown in Figure 13. A mono mix of left and right output mixers is also available on OUT3.

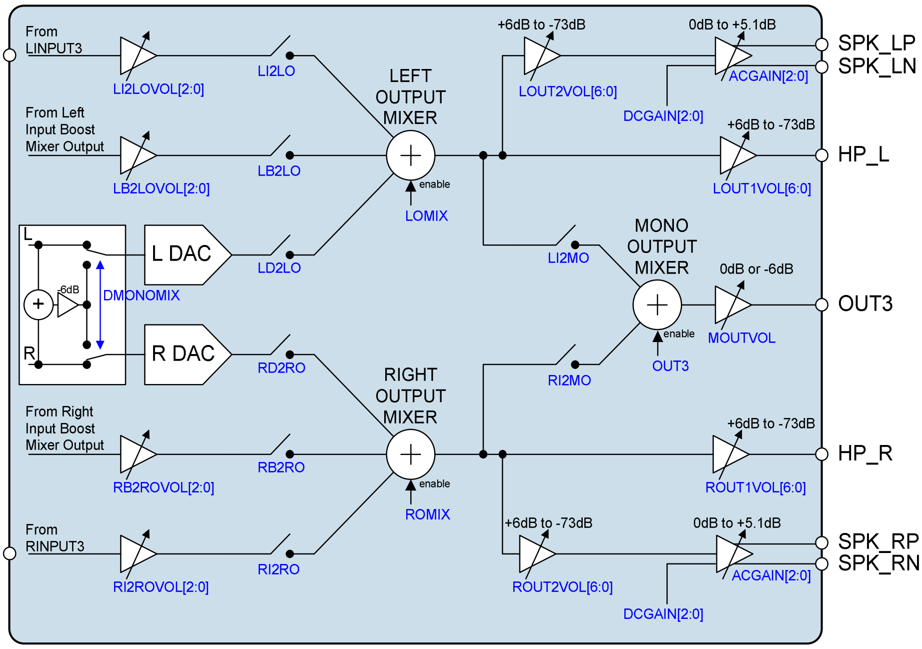


Figure 13 Output Mixer Path

Left and right mixers are enabled by the LOMIX and ROMIX register bits. The mono mixer is enabled by OUT3 register bit, which also enables the OUT3 driver.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 (2Fh) Power Management (3)	3	LOMIX	0	Left Output Mixer Enable Control 0 = Disabled 1 = Enabled
	4	ROMIX	0	Right Output Mixer Enable Control 0 = Disabled 1 = Enabled
R26 (1Ah) Power Management (2)	1	OUT3	0	Mono Output and Mono Mixer Enable Control 0 = Mono mixer and output disabled 1 = Mono mixer and output enabled

Table 15 Output Mixer Enable Control

Inputs to the mixers from the DAC and bypass paths can be individually muted. The bypass paths have programmable attenuation as shown in Table 16. To prevent pop noise, it is recommended not to change volume levels of these paths during playback.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R34 (22h) Left Output Mixer Control	8	LD2LO	0	Left DAC to Left Output Mixer 0 = Disable (Mute) 1 = Enable Path
	7	LI2LO	0	LINPUT3 to Left Output Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	LI2LOVOL [2:0]	101 (-15dB)	LINPUT3 to Left Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB
R45 (2Dh) Bypass (1)	7	LB2LO	0	Left Input Boost Mixer to Left Output Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	LB2LOVOL [2:0]	101 (-15dB)	Left Input Boost Mixer to Left Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB
R37 (25h) Right Output Mixer Control	8	RD2RO	0	Right DAC to Right Output Mixer 0 = Disable (Mute) 1 = Enable Path
	7	RI2RO	0	RINPUT3 to Right Output Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	RI2ROVOL [2:0]	101 (-15dB)	RINPUT3 to Right Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB
R46 (2Eh) Bypass (2)	7	RB2RO	0	Right Input Boost Mixer to Right Output Mixer 0 = Disable (Mute) 1 = Enable Path
	6:4	RB2ROVOL [2:0]	101 (-15dB)	Right Input Boost Mixer to Right Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB

Table 16 Left and Right Output Mixer Mute and Volume Control

The mono output mixer can output, left, right, left+right or a buffered VMID. 0dB or 6dB attenuation is selectable using MOUTVOL register bit. It is recommended to attenuate a mono mix of left and right channels by 6dB in order to prevent clipping. This attenuation control (MOUTVOL) should not be modified while OUT3 is enabled as this may cause an audible click noise.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R38 (26h) Mono Out Mix (1)	7	L2MO	0	Left Output Mixer to Mono Output Mixer Control 0 = Left channel mix disabled 1 = Left channel mix enabled
R39 (27h) Mono Out Mix (2)	7	R2MO	0	Right Output Mixer to Mono Output Mixer Control 0 = Right channel mix disabled 1 = Right channel mix enabled
R42 (2Ah) Mono Out Volume	6	MOUTVOL	1	Mono Output Mixer Volume Control 0 = 0dB 1 = -6dB

Table 17 Output Mixer Enable Control

When left and right inputs to the mono mixer are both disabled, the mono mixer will output VMID.

ANALOGUE OUTPUTS

HP_L AND HP_R OUTPUTS

The HP_L and HP_R pins can drive a 16Ω or 32Ω headphone or a line output (see Headphone Output and Line Output sections, respectively). The signal volume on HP_L and HP_R can be independently adjusted under software control by writing to LOUT1VOL and ROUT1VOL, respectively. Note that gains over 0dB may cause clipping if the signal is large. Any gain setting below 0101111 (minimum) mutes the output driver. The corresponding output pin remains at the same DC level (the reference voltage on the VREF pin), so that no click noise is produced when muting or un-muting.

A zero cross detect on the analogue output may also be enabled when changing the gain setting to minimize audible clicks and zipper noise as the gain updates. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R23 (17h). The timeout period is set by TOCLKSEL. Note that SYSCLK must be enabled to use this function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) LOUT1 Volume	8	OUT1VU	0	Headphone Volume Update 0 = Store LOUT1VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LOUT1VOL, right = intermediate latch)
	7	LO1ZC	0	Left zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6:0	LOUT1VOL [6:0]	0000000 (MUTE)	LOUT1 Volume 1111111 = +6dB … 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE
R3 (03h) ROUT1 Volume	8	OUT1VU	0	Headphone Volume Update 0 = Store ROUT1VOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = ROUT1VOL)
	7	RO1ZC	0	Right zero cross enable 0 = Change gain immediately 1 = Change gain on zero cross only
	6:0	ROUT1VOL [6:0]	0000000 (MUTE)	ROUT1 Volume Similar to LOUT1VOL

Table 18 LOUT1/ROUT1 Volume Control

See "Volume Updates" for more information on volume update bits, zero cross and timeout operation.

CLASS D SPEAKER OUTPUTS

The SPK_LP/SPK_LN and SPK_RP/SPK_RN output pins are class D speaker drivers. Each pair is independently controlled and can drive an 8Ω BTL speaker (see Speaker Output section). Output mixer volume is relative to AVDD, while an additional boost stage is available to accommodate higher SPKVDD1/SPKVDD2 supply voltages. This allows AVDD to be run at a lower voltage to save power, while maximum output power can be delivered to the load, utilising the full range of SPKVDD1/SPKVDD2. Note that the BTL speaker connection provides an additional +6dB gain at the output.

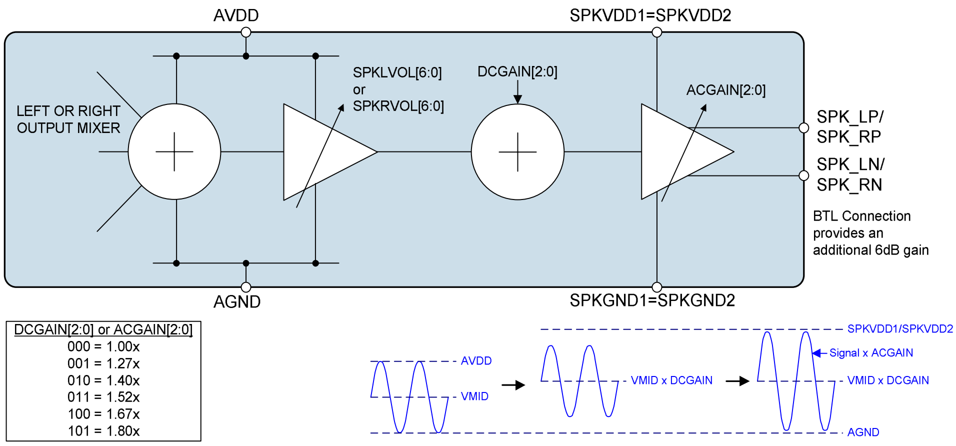


Figure 14 Speaker Boost Operation

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) Left Speaker Volume	6:0	SPKLVOL [6:0]	0000000 (MUTE)	SPK_LP/SPK_LN Volume 1111111 = +6dB … 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE
	7	SPKLZC	0	Left Speaker Zero Cross Enable 1 = Change gain on zero cross only 0 = Change gain immediately
	8	SPKVU	0	Speaker Volume Update 0 = Store SPKLVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = SPKLVOL, right = intermediate latch)
R41 (29h) Right Speaker Volume	6:0	SPKRVOL [6:0]	0000000 (MUTE)	SPK_RP/SPK_RN Volume 1111111 = +6dB … 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE
	7	SPKRZC	0	Right Speaker Zero Cross Enable 1 = Change gain on zero cross only 0 = Change gain immediately
	8	SPKVU	0	Speaker Volume Update 0 = Store SPKRVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = SPKRVOL)
R51 (33h) Class D Control (3)	5:3	DCGAIN [2:0]	000 (1.0x)	DC Speaker Boost (Boosts speaker DC output level by up to 1.8 x on left and right channels) 000 = 1.00x boost (+0dB) 001 = 1.27x boost (+2.1dB) 010 = 1.40x boost (+2.9dB) 011 = 1.52x boost (+3.6dB) 100 = 1.67x boost (+4.5dB) 101 = 1.8x boost (+5.1dB) 110 to 111 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2:0	ACGAIN [2:0]	000 (1.0x)	AC Speaker Boost (Boosts speaker AC output signal by up to 1.8 x on left and right channels) 000 = 1.00x boost (+0dB) 001 = 1.27x boost (+2.1dB) 010 = 1.40x boost (+2.9dB) 011 = 1.52x boost (+3.6dB) 100 = 1.67x boost (+4.5dB) 101 = 1.8x boost (+5.1dB) 110 to 111 = Reserved

Table 19 SPK_L/SPK_R Volume and Speaker Boost Control

To prevent pop noise, DCGAIN and ACGAIN should not be modified while the speaker outputs are enabled.

To avoid clipping at speaker ground, ACGAIN should not be greater than DCGAIN.

To avoid clipping at speaker supply, SPKVDD1 and SPKVDD2 must be high enough to support the peak output voltage when using DCGAIN and ACGAIN functions. The peak output voltage is AVDD*(DCGAIN+ACGAIN)/2.

DCGAIN should normally be set to the same value as ACGAIN.

See "Volume Updates" for more information on volume update bits, zero cross and timeout operation.

See "Class D Speaker Outputs" for more information on class D speaker operation.

OUT3 OUTPUT

The OUT3 pin can drive a 16Ω or 32Ω headphone or a line output or be used as a pseudo-ground for capless headphone drive (see Headphone Output section). It can also drive out a mono mix of left and right output mixers (See Output Signal Path).

ENABLING THE OUTPUTS

Each analogue output of the WM8956 can be independently enabled or disabled. The analogue mixer associated with each output is powered on or off along with the output pin. All outputs are disabled by default. To save power, unused outputs should remain disabled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) Power Management (2)	6	LOUT1	0	LOUT1 Output Enable
	5	ROUT1	0	ROUT1 Output Enable
	4	SPKL	0	SPK_LP and SPK_LN Volume Control Enable
	3	SPKR	0	SPK_RP and SPK_RN Volume Control Enable
	1	OUT3	0	OUT3 Enable
R49 (31h) Class D Control (1)	7:6	SPK_OP_EN [1:0]	00	Enable Class D Speaker Outputs 00 = Off 01 = Left speaker only 10 = Right speaker only 11 = Left and right speakers enabled
Note: All “Enable” bits are 1 = ON, 0 = OFF				

Table 20 Analogue Output Control

The speaker output enable bits SPK_OP_EN[1:0] should not be enabled until there is a valid switching clock to drive the class D outputs. This means that SYSCLK must be active, and DCLKDIV set to an appropriate value to produce a class D clock of between 700kHz and 800kHz for best performance (See "Class D Speaker Outputs" and "Clocking and Sample Rates" sections for more information).

Whenever an analogue output is disabled, it remains connected to VREF through a resistor. This helps to prevent pop noise when the output is re-enabled. The resistance between VREF and each output can be controlled using the VROI bit in register 27. If a high impedance is desired for disabled outputs, VROI can then be set to 1, increasing the resistance to about 20kΩ.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 (1Bh) Additional (1)	6	VROI	0	VREF to Analogue Output Resistance (Disabled Outputs) 0 = 500Ω VMID to output 1 = 20kΩ VMID to output

Table 21 Disabled Outputs to VREF Resistance

HEADPHONE OUTPUT

Analogue outputs HP_L/HP_R, and OUT3, can drive a 16Ω or 32Ω headphone load, either through DC blocking capacitors, or DC coupled without any capacitor.

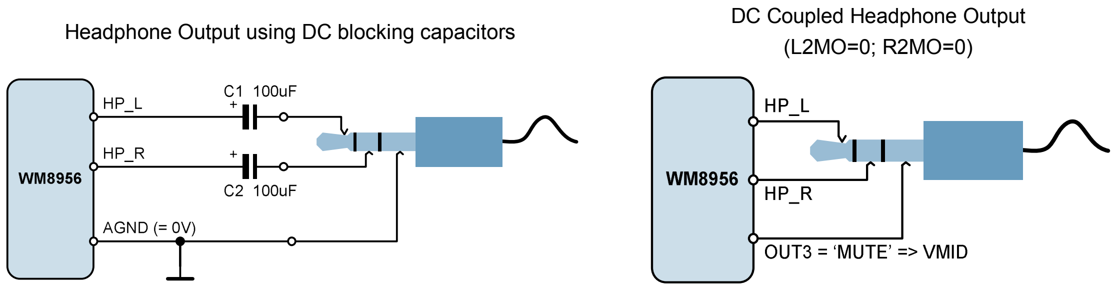


Figure 15 Recommended Headphone Output Configurations

When DC blocking capacitors are used, then their capacitance and the load resistance together determine the lower cut-off frequency, f_c. Increasing the capacitance lowers f_c, improving the bass response. Smaller capacitance values will diminish the bass response. Assuming a 32Ω load and C1, C2 = 100µF:

$f_c = 1 / 2\pi R_L C_1 = 1 / (2\pi \times 32\Omega \times 100\mu F) = 50$ Hz

In the DC coupled configuration, the headphone “ground” is connected to the OUT3 pin, which must be enabled by setting OUT3 = 1 and muted by setting L2MO=0 and R2MO=0. As the OUT3 pin produces a DC voltage of AVDD/2 (=VREF), there is no DC offset between HP_L/HP_R and OUT3, and therefore no DC blocking capacitors are required. This saves space and material cost in portable applications.

It is recommended to connect the DC coupled headphone outputs only to headphones, and not to the line input of another device. Although the built-in short circuit protection will prevent any damage to the headphone outputs, such a connection may be noisy, and may not function properly if the other device is grounded.

CLASS D SPEAKER OUTPUTS

The class D speaker outputs SPK_LN/SPK_LP and SPK_RN/SPK_RP can drive 1W into 8Ω BTL speakers. Class D outputs reduce power consumption and maximise efficiency by reducing power dissipated in the output drivers, delivering most of the power directly to the load. This is achieved by pulse width modulation (PWM) of a high frequency square wave, allowing the audio signal level to be set by controlling the pulse width. The frequency of the output waveform is controlled by DCLKDIV, and is derived from SYSCLK.

When the speakers are close to the device (typically less than about 100mm) the internal filtering effects of the speaker can be used. Where signals are routed over longer distances, it is recommended to use additional passive filtering, positioned close to the WM8956, to reduce EMI. See "Applications Information" for more information on EMI reduction.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 (08h) Clocking (2)	8:6	DCLKDIV	111	Controls clock division from SYSCLK to generate suitable class D clock. 000 = SYSCLK / 1.5 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16
R49 (31h) Class D Control (1)	7:6	SPK_OP_EN [1:0]	00	Enable Class D Speaker Outputs 00 = Off 01 = Left speaker only 10 = Right speaker only 11 = Left and right speakers enabled

Table 22 Class D Control Registers

The class D outputs require a PWM switching clock, which is derived from SYSCLK. This clock should not be altered or disabled while the class D outputs are enabled.

See "Clocking and Sample Rates" for more information.

VOLUME UPDATES

Volume settings will not be applied to input or output PGAs until a '1' is written to one of the update bits (IPVU, OUT1VU, SPKVU bits). This is to allow left and right channels to be updated at the same time, as shown in Figure 16.

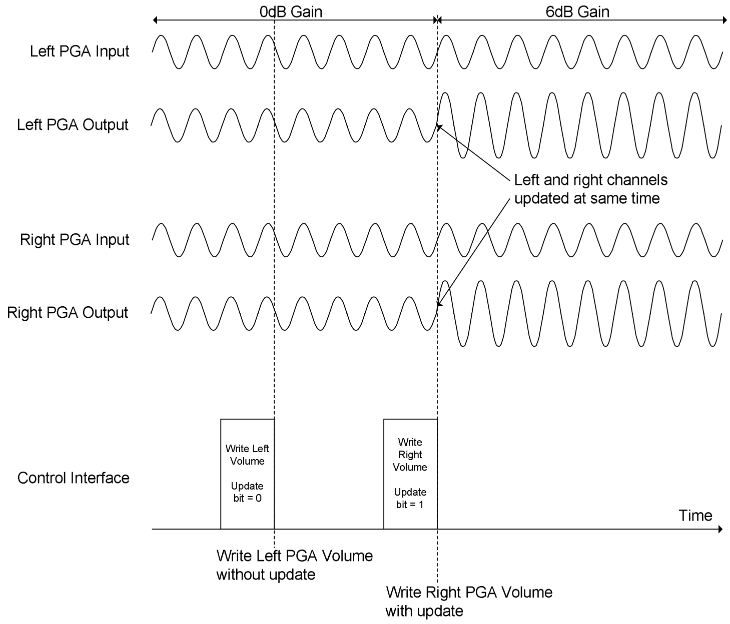


Figure 16 Simultaneous Left and Right Volume Updates

If the volume is adjusted while the signal is a non-zero value, an audible click can occur as shown in Figure 17.

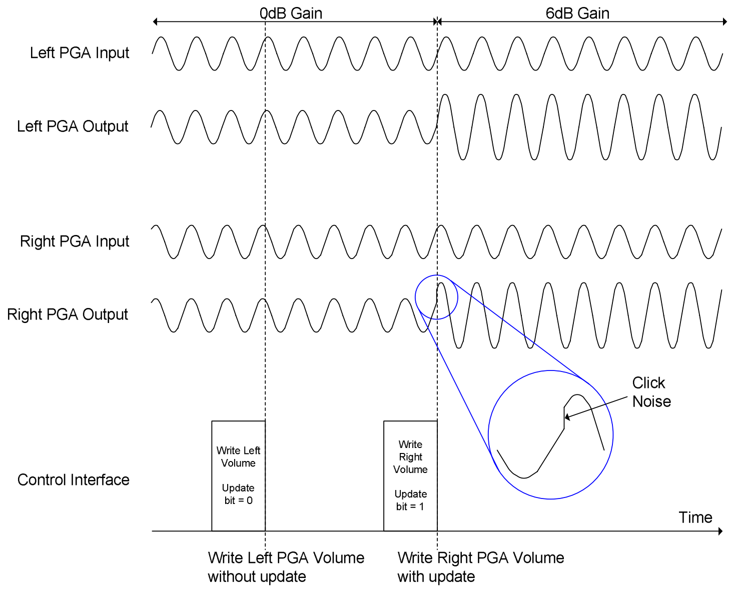


Figure 17 Click Noise During Volume Update

In order to prevent this click noise, a zero cross function is provided. When enabled, this will cause the PGA volume to update only when a zero crossing occurs, minimising click noise as shown in Figure 18.

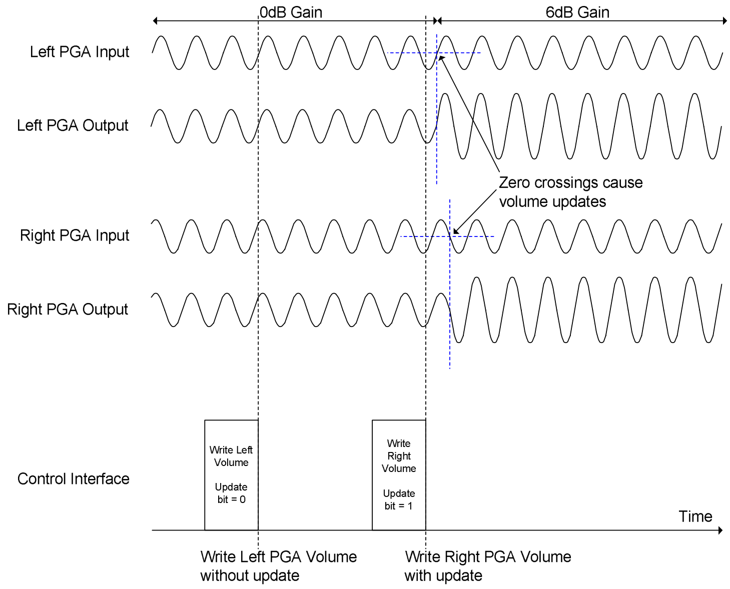


Figure 18 Volume Update Using Zero Cross Detection

If there is a long period where no zero-crossing occurs, a timeout circuit in the WM8956 will automatically update the volume. The volume updates will occur between one and two timeout periods, depending on when the volume update bit is set as shown in Figure 19. The TOEN register bit must be set to enable this timeout function. The timeout period is set by TOCLKSEL.

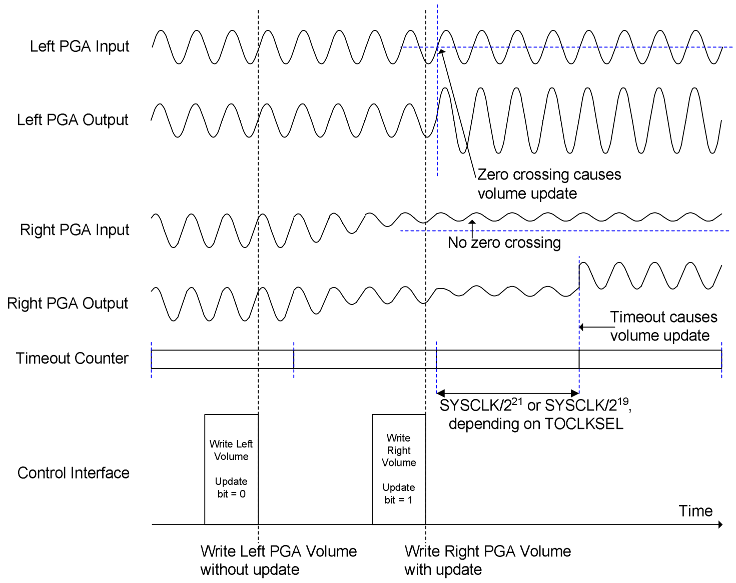


Figure 19 Volume Update After Timeout

HEADPHONE JACK DETECT

The GPIO1, LINPUT3/JD2 and RINPUT3/JD3 pins can be selected as headphone jack detect inputs to automatically disable the speaker output and enable the headphone output e.g. when a headphone is plugged into a jack socket. In this mode, enabled by setting HPSWEN, the headphone detect input pin switches between headphone and speaker outputs (e.g. when the pin is connected to a mechanical switch in the headphone socket to detect plug-in). The HPSEL[1:0] bits select the input pin used for this function. The HPSWPOL bit reverses the pin's polarity. Note that the LOUT1, ROUT1, SPKL and SPKR bits in register 26 must also be set for headphone and speaker output (see Table 23 and Table 24).

TOEN must also be set to enable the clock which is used for de-bouncing the jack detect input. TOCLKSEL selects a fast or slow de-bounce period. Note that SYSCLK must be enabled to use this function.

When using capless mode, the OUT3CAP bit should be enabled so that OUT3 is enabled/disabled at the same time as HP_L and HP_R to prevent pop noise.

The debounced headphone detect signal can also be output to the GPIO1 pin (See GPIO section). This function is not available when using GPIO1 as an input.

When using the GPIO1 pin as a headphone detect input, the ALRCGPIO register bit needs to be set to 1 (See GPIO section for more information).

Note:

When LINPUT3 or RINPUT3 is used as the headphone detect input, the thresholds become CMOS levels (0.3 AVDD / 0.7 AVDD).

HPSWEN	HPSWPOL	HEADPHONE DETECT PIN (LINPUT3/JD2, RINPUT3/JD3 OR GPIO1)	L/ROUT1 (AND OUT3 IN CAPLESS MODE) (REG. 26)	SPKL/R (REG. 26)	HEADPHONE ENABLED (AND OUT3 IN CAPLESS MODE)	SPEAKER ENABLED
0	X	X	0	0	no	no
0	X	X	0	1	no	yes
0	X	X	1	0	yes	no
0	X	X	1	1	yes	yes
1	0	0	X	0	no	no
1	0	0	X	1	no	yes
1	0	1	0	X	no	no
1	0	1	1	X	yes	no
1	1	0	0	X	no	no
1	1	0	1	X	yes	no
1	1	1	X	0	no	no
1	1	1	X	1	no	yes

Table 23 Headphone Jack Detect Operation

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Additional Control (2)	6	HPSWEN	0	Headphone Switch Enable 0 = Headphone switch disabled 1 = Headphone switch enabled
	5	HPSWPOL	0	Headphone Switch Polarity 0 = HPDETECT high = headphone 1 = HPDETECT high = speaker
R27 (1Bh) Additional Control (3)	3	OUT3CAP	0	Capless Mode Headphone Switch Enable 0 = OUT3 unaffected by jack detect events 1 = OUT3 enabled and disabled together with HP_L and HP_R in response to jack detect events
R48 (30h) Additional Control (4)	3:2	HPSEL[1:0]	00	Headphone Switch Input Select 0X = GPIO1 used for jack detect input (Requires pin to be configured as a GPIO using ALRCGPIO) 10 = JD2 used for jack detect input 11 = JD3 used for jack detect input
R23 (17h) Additional Control (1)	0	TOEN	0	Slow Clock Enable (Must be enabled for jack detect de-bounce) 0 = Slow Clock Disabled 1 = Slow Clock Enabled
	1	TOCLKSEL	0	Slow Clock Selection (Used for volume update timeouts and for jack detect debounce) 0 = SYSCLK / 2^{21} (Slower Response) 1 = SYSCLK / 2^{19} (Faster Response)

Table 24 Headphone Jack Detect

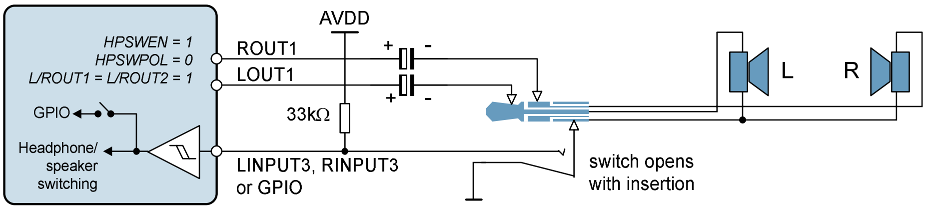


Figure 20 Example Headset Detection Circuit Using Normally-Open Switch

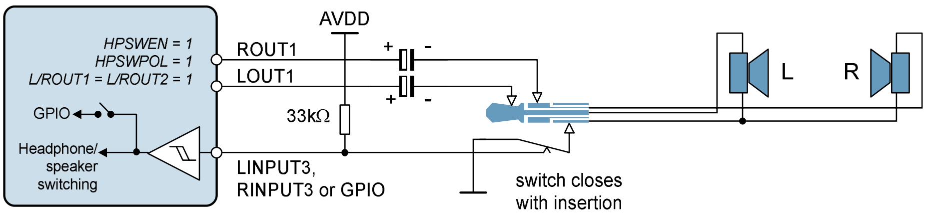


Figure 21 Example Headset Detection Circuit Using Normally-Closed Switch

THERMAL SHUTDOWN

The speaker and headphone outputs can drive very large currents. To protect the WM8956 from overheating a thermal shutdown circuit is included and is enabled by default. If the device temperature reaches approximately 150^0C and the thermal shutdown circuit is enabled (TSDEN = 1; TSENSEN = 1) the speaker and headphone amplifiers (HP_L, HP_R, SPK_LP, SPK_LN, SPK_RP, SPK_RN and OUT3) will be disabled. This feature can be disabled to save power when the device is in standby mode.

TSENSEN must be set to 1 to enable the temperature sensor when using the TSDEN thermal shutdown function. The output of the temperature sensor can also be output to the GPIO1 pin.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	8	TSDEN	1	Thermal Shutdown Enable 0 = Thermal shutdown disabled 1 = Thermal shutdown enabled (TSENSEN must be enabled for this function to work)
R48 (30h) Additional Control (4)	1	TSENSEN	1	Temperature Sensor Enable 0 = Temperature sensor disabled 1 = Temperature sensor enabled

Table 25 Thermal Shutdown

GENERAL PURPOSE INPUT/OUTPUT

The WM8956 has two dual purpose GPIO pins and one dedicated GPIO pin.

- LINPUT3/JD2: Analogue input or headphone detect input.
- RINPUT3/JD3: Analogue input or headphone detect input.
- GPIO1: GPIO pin.

The GPIO1 pin can be configured as a headphone detect input, or one of a number of GPIO output functions as shown in Table 26.

The default configuration for the LINPUT3 and RINPUT2 pins is to be analogue inputs. The ALRCGPIO bit must be set to enable GPIO1 pin to operate as a GPIO.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h) Audio Interface (2)	6	ALRCGPIO	0	GPIO1 Pin Function Select 0 = GPIO1 pin disabled 1 = GPIO1 pin configured as GPIO
R48 (30h) Additional Control (4)	6:4	GPIOSEL [2:0]	000	GPIO1 GPIO Function Select: 000 = Jack detect input 001 = Reserved 010 = Temperature ok 011 = Debounced jack detect output 100 = SYSCLK output 101 = PLL lock 110 = Logic 0 111 = Logic 1
	7	GPIOPOL	0	GPIO Polarity Invert 0 = Non inverted 1 = Inverted
R52 (34h) Clocking (2)	8:6	OPCLKDIV [2:0]	000	SYSCLK Output to GPIO Clock Division Ratio 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 5.5 101 = SYSCLK / 6

Table 26 GPIO Control

Slow clock must be enabled (TOEN = 1) when using the jack detect function. This slow clock is used to debounce the jack detect input. The debounce period can be selected using TOCLKSEL.

The temperature sensor must be enabled for the "Temperature ok" GPIO output to function properly.

For further details of the Jack detect operation see the Headphone Switch section.

DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting DAC data into the WM8956. It uses three pins:

- DACDAT: DAC data input
- DACLRC: DAC data alignment clock
- BCLK: Bit clock, for synchronisation

The clock signals BCLK and DACLRC can be outputs when the WM8956 operates as a master, or inputs when it is a slave (see Master and Slave Mode Operation, below).

Four different audio data formats are supported:

- Left justified
- Right justified
- I^2S
- DSP mode

All four of these modes are MSB first. They are described in Audio Data Formats, below. Refer to the Electrical Characteristic section for timing information.

MASTER AND SLAVE MODE OPERATION

The WM8956 can be configured as either a master or slave mode device. As a master device the WM8956 generates BCLK and DACLRC and thus controls sequencing of the data transfer on DACDAT. In slave mode, the WM8956 responds with data to clocks it receives over the digital audio interface. The mode can be selected by writing to the MS bit. Master and slave modes are illustrated below.

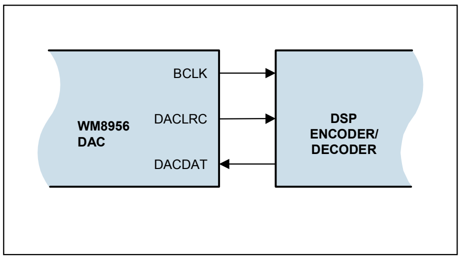


Figure 22 Master Mode

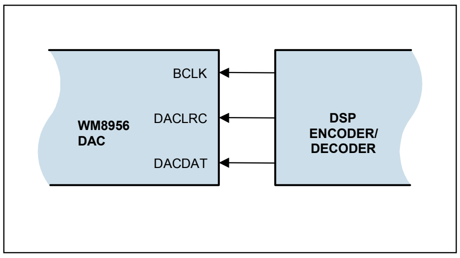


Figure 23 Slave Mode

BCLK DIVIDE

The BCLK frequency is controlled by BCLKDIV[3:0]. See Clocking and Sample Rates section for more information.

AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

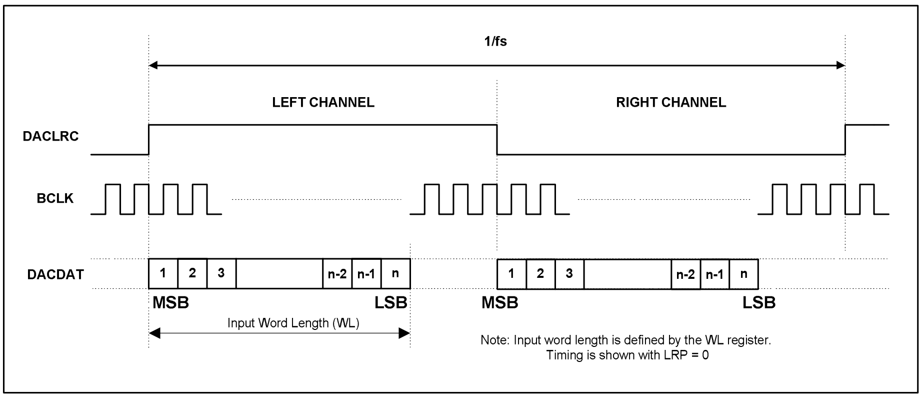


Figure 24 Left Justified Audio Interface (assuming n-bit word length)

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.

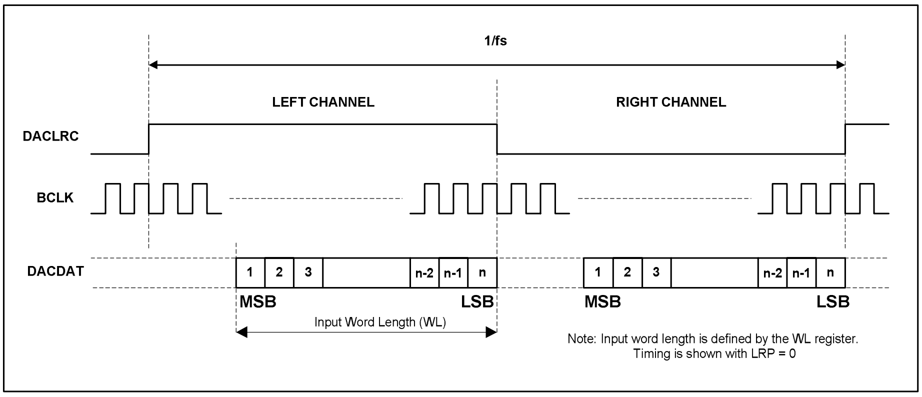


Figure 25 Right Justified Audio Interface (assuming n-bit word length)

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

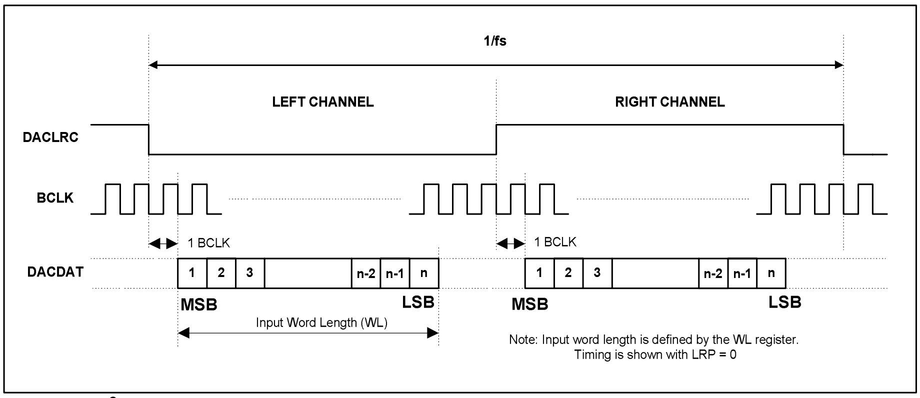


Figure 26 I²S Justified Audio Interface (assuming n-bit word length)

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 27 and Figure 28. In device slave mode, Figure 29 and Figure 30, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

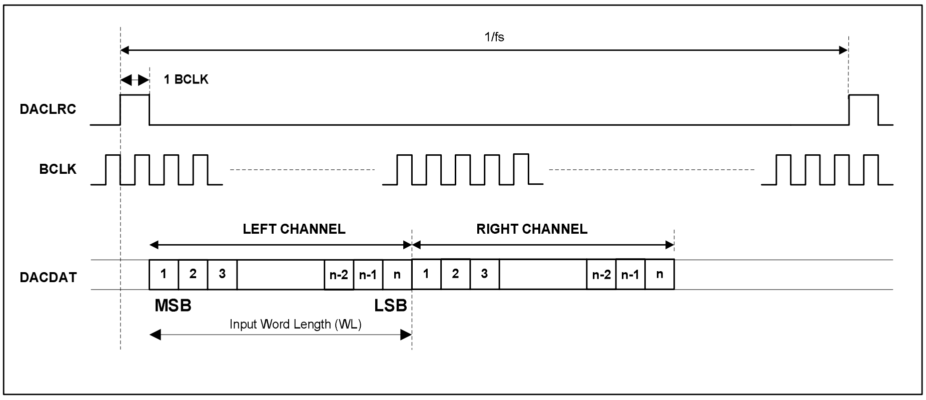


Figure 27 DSP/PCM Mode Audio Interface (mode A, LRP=0, Master)

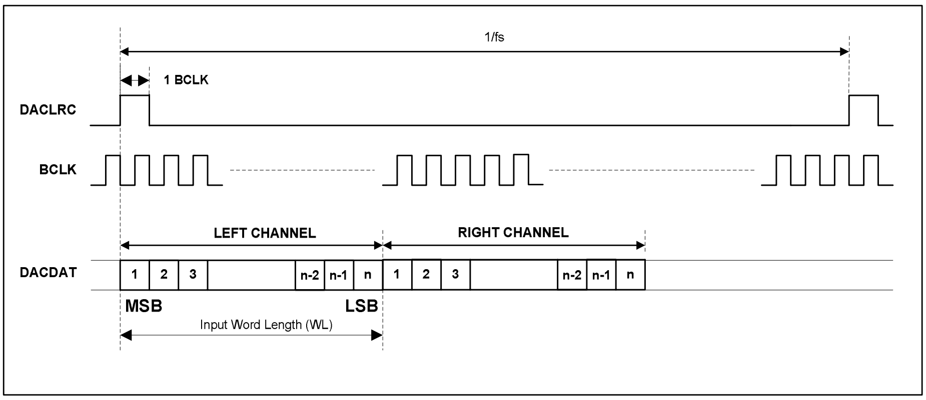


Figure 28 DSP/PCM Mode Audio Interface (mode B, LRP=1, Master)

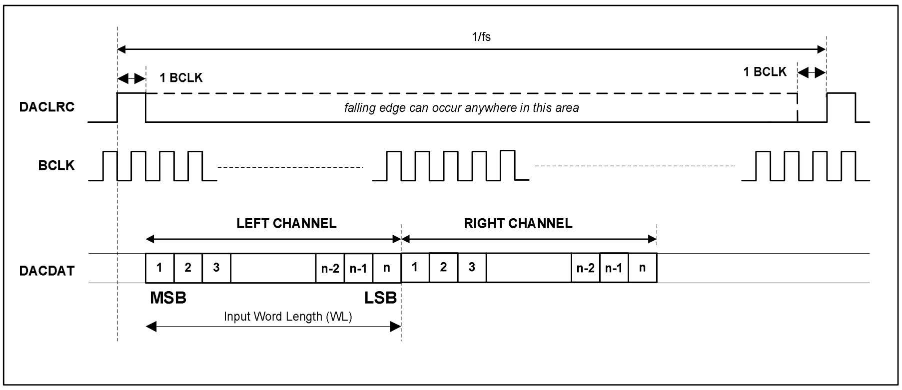


Figure 29 DSP/PCM Mode Audio Interface (mode A, LRP=0, Slave)

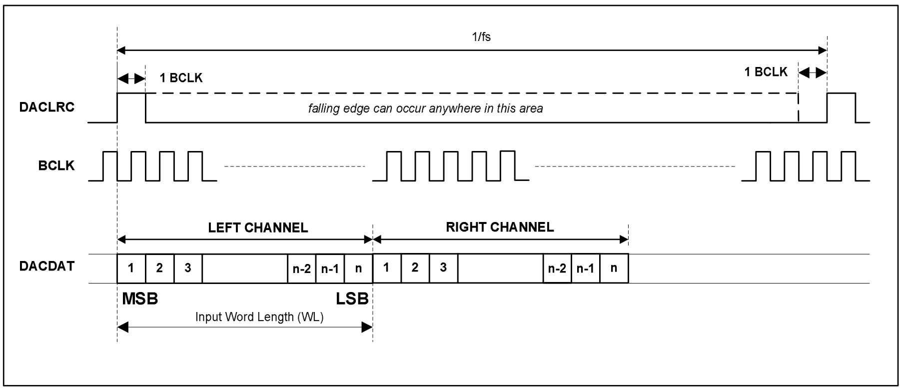


Figure 30 DSP/PCM Mode Audio Interface (mode B, LRP=1, Slave)

AUDIO INTERFACE CONTROL

The register bits controlling audio format, word length and master / slave mode are summarised in Table 27. MS selects audio interface operation in master or slave mode. In Master mode BCLK and DACLRC are outputs. The frequency of DACLRC is set by the DACDIV bits and the frequency of BCLK is set by the BCLKDIV bits (See "Clocking and Sample Rates"). In Slave mode BCLK and DACLRC are inputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) Digital Audio Interface Format	7	BCLKINV	0	BCLK invert bit (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted
	6	MS	0	Master / Slave Mode Control 0 = Enable slave mode 1 = Enable master mode
	5	DLRSWAP	0	Left/Right DAC Channel Swap 0 = Output left and right data as normal 1 = Swap left and right DAC data in audio interface
	4	LRP	0	Right, left and I^2S modes – LRCLK polarity 0 = normal LRCLK polarity 1 = invert LRCLK polarity
				DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B)
	3:2	WL[1:0]	10	Audio Data Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits (see Note)
	1:0	FORMAT[1:0]	10	Audio Data Format Select 00 = Right justified 01 = Left justified 10 = I^2S Format 11 = DSP Mode

Table 27 Audio Data Format Control

Note: Right Justified mode does not support 32-bit data.

AUDIO INTERFACE OUTPUT TRISTATE

Register bit TRIS, register 24(18h) bit[3] can be used to switch DACLRC and BCLK to inputs. In Slave mode (MS=0) DACLRC and BCLK are by default configured as inputs (see Table 28).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R24 (18h) Additional Control (2)	3	TRIS	0	Switches DACLRC and BCLK to inputs. 0 = DACLRC and BCLK are inputs (slave mode) or outputs (master mode) 1 = DACLRC and BCLK are inputs

Table 28 Tri-stating the Audio Interface

MASTER MODE DACLRC ENABLE

In master mode, by default DACLRC and BCLK are disabled when the DACs are both disabled.

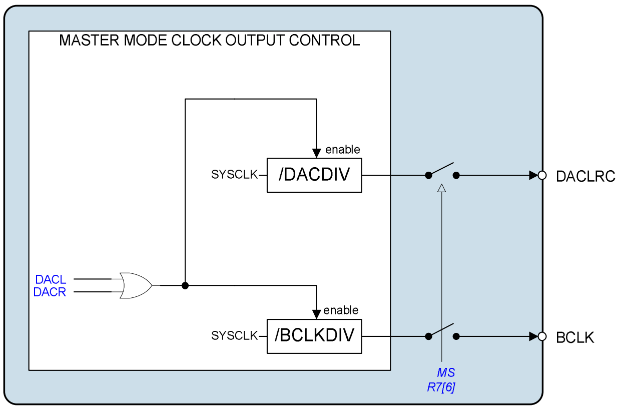


Figure 31 Master Mode Clock Output Control

COMPANDING

The WM8956 supports A-law and μ-law companding. Companding can be enabled on the DAC audio interface by writing the appropriate value to the DACCOMP register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 (09h) Audio Interface (2)	4:3	DACCOMP	00	DAC companding 00 = off 01 = reserved 10 = μ-law 11 = A-law
	5	WL8	0	0 = off 1 = device operates in 8-bit mode.

Table 29 Companding Control

Companding involves using a piecewise linear approximation of the following equations (as set out by ITU-T G.711 standard) for data compression:

μ-law (where μ=255 for the U.S. and Japan):

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu) \qquad -1 \le x \le 1$

A-law (where A=87.6 for Europe):

$F(x) = A|x| / (1 + \ln A) \qquad \} \text{ for } x \le 1/A$

$F(x) = (1 + \ln A|x|) / (1 + \ln A) \qquad \} \text{ for } 1/A \le x \le 1$

The companded data is also inverted as recommended by the G.711 standard (all 8 bits are inverted for μ-law, all even data bits are inverted for A-law). The data will be transmitted as the first 8 MSB's of data.

Companding converts 13 bits (μ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. The input data range is separated into 8 levels, allowing low amplitude signals better precision than that of high amplitude signals. This is to exploit the operation of the human auditory system, where louder sounds do not require as much resolution as quieter sounds. The companded signal is an 8-bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits).

Setting the WL8 register bit allows the device to operate with 8-bit data. In this mode it is possible to use 8 BCLK cycles per LRC frame. When using DSP mode B, this allows 8-bit data words to be output consecutively every 8 BCLK cycles and can be used with 8-bit data words using the A-law and u-law companding functions.

BIT7	BIT[6:4]	BIT[3:0]
SIGN	EXPONENT	MANTISSA

Table 30 8-bit Companded Word Composition

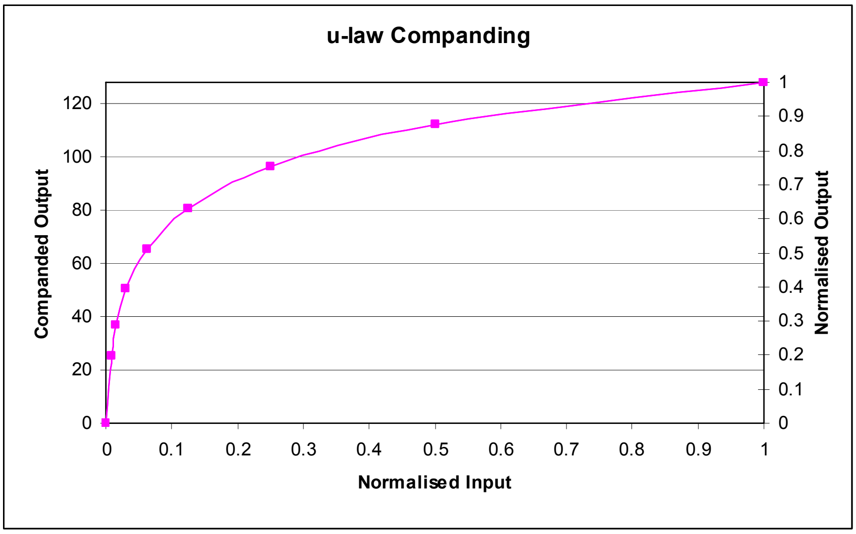


Figure 32 μ-Law Companding

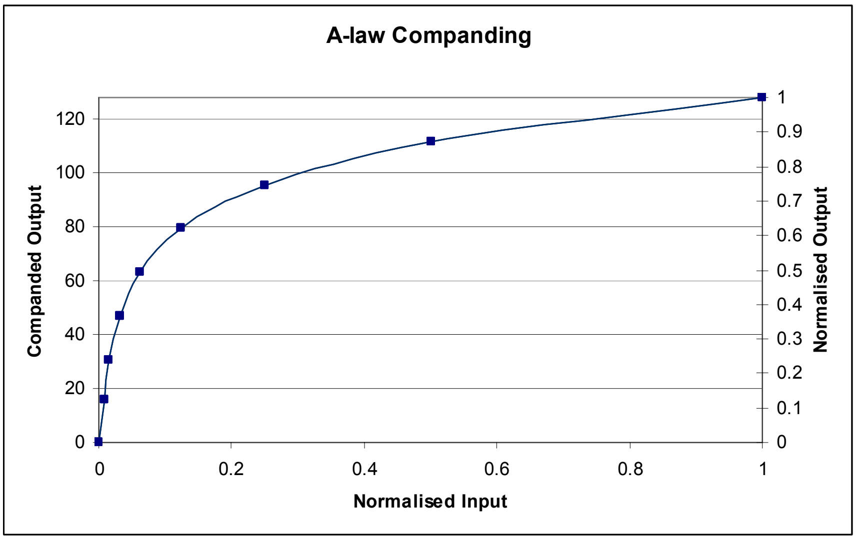


Figure 33 A-Law Companding

CLOCKING AND SAMPLE RATES

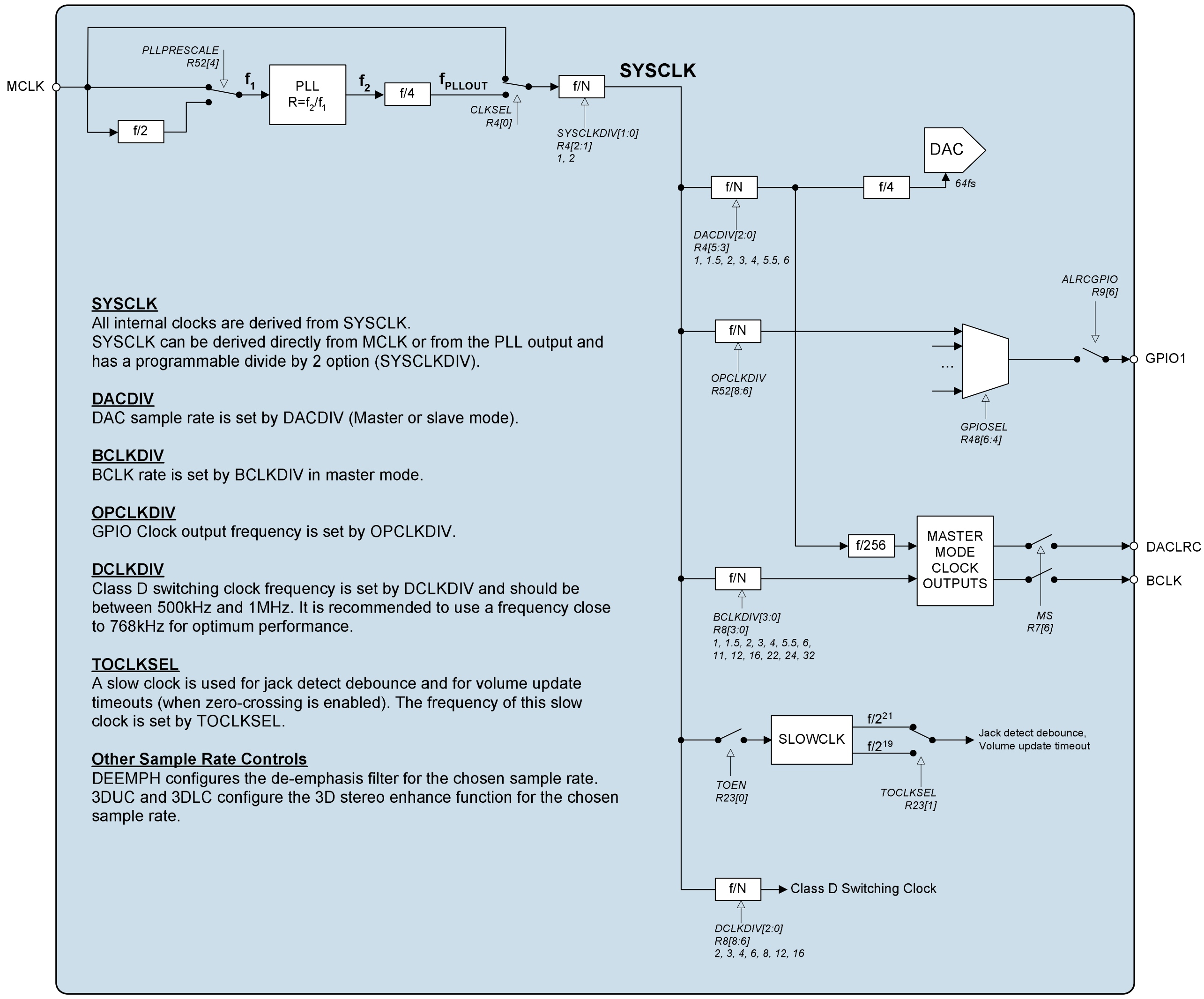


Figure 34 Clocking Scheme

Clocks for the DACs, the DSP core functions, the digital audio interface and the class D outputs are all derived from SYSCLK as show in Figure 34.

SYSCLK can either be derived directly from MCLK, or generated from a PLL using MCLK as a reference. The clock source is selected by CLKSEL. Many commonly-used audio sample rates can be derived directly from MCLK, while the PLL provides additional flexibility.

The DAC sample rate is selectable, relative to SYSCLK, using DACDIV. In master mode, BCLK is also derived from SYSCLK via a programmable clock divide (BCLKDIV).

When the GPIO1 pin is configured as a GPIO, a clock derived from SYSCLK can be output on this pin to provide clocking for other parts of the system. The frequency of this output clock is set by OPCLKDIV.

A slow clock derived from SYSCLK is used to de-bounce the headphone detect function, and to set the timeout period for volume updates when zero-cross functions are used. This clock is enabled by TOEN and its frequency is set by TOCLKSEL.

The class D outputs require a clock, and this is also derived from SYSCLK via a programmable divider (DCLKDIV) as shown in Figure 34. The class D switching clock should be set between 700kHz and 800kHz.

The class D switching clock should not be disabled when the speaker outputs are active, as this would prevent the speaker outputs from functioning. The class D switching clock frequency should not be altered while the speaker outputs are active as this may generate an audible click.

Table 31 shows the clocking and sample rate controls for MCLK input, BCLK output (in master mode), DACs, class D outputs and GPIO clock output. Refer to Table 32 for example clocking configurations.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R4 (04h) Clocking (1)	5:3	DACDIV [2:0]	000	DAC Sample rate divider (Also determines DACLRC in master mode) 000 = SYSCLK / (1.0 * 256) 001 = SYSCLK / (1.5 * 256) 010 = SYSCLK / (2 * 256) 011 = SYSCLK / (3 * 256) 100 = SYSCLK / (4 * 256) 101 = SYSCLK / (5.5 * 256) 110 = SYSCLK / (6 * 256) 111 = Reserved
	2:1	SYSCLKDIV [1:0]	00	SYSCLK Pre-divider. Clock source (MCLK or PLL output) will be divided by this value to generate SYSCLK. 00 = Divide SYSCLK by 1 01 = Reserved 10 = Divide SYSCLK by 2 11 = Reserved
	0	CLKSEL	0	SYSCLK selection 0 = SYSCLK derived from MCLK 1 = SYSCLK derived from PLL output
R8 (08h) Clocking (2)	8:6	DCLKDIV	111	Class D switching clock divider. 000 = SYSCLK / 1.5 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16
	3:0	BCLKDIV[3:0]	0000	BCLK Frequency (Master Mode) 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101 to 1111 = SYSCLK / 32

Table 31 DAC and BCLK Control

SYSCLK (=MCLK OR PLL OUTPUT) (MHz)	DACDIV	DAC SAMPLE RATE (kHz)
12.288	000 (=1)	48
	001 (=1.5)	32
	010 (=2)	24
	011 (=3)	16
	100 (=4)	12
	101 (=5.5)	(Not used)
	110 (=6)	8
	111	Reserved
11.2896	000 (=1)	44.1
	001 (=1.5)	(Not used)
	010 (=2)	22.05
	011 (=3)	(Not used)
	100 (=4)	11.025
	101 (=5.5)	8.018
	110 (=6)	(Not used)
	111	Reserved
2.048	000 (=1)	8
	001 (=1.5)	(Not used)
	010 (=2)	(Not used)
	011 (=3)	(Not used)
	100 (=4)	(Not used)
	101 (=5.5)	(Not used)
	110 (=6)	(Not used)
	111	Reserved

Table 32 DAC Sample Rates

When operating in slave mode, the host device must provide sufficient BCLK cycles to transfer complete data words to the DACs.

Table 33 shows the maximum word lengths supported for a given SYSCLK and BCLKDIV, assuming that the DACs are running at maximum rate (i.e. DACDIV[2:0]=000).

SYSCLK (=MCLK OR PLL OUTPUT) (MHz)	BCLKDIV[3:0]	BCLK RATE (MASTER MODE) (MHz)	MAXIMUM WORD LENGTH (AT MAXIMUM DAC SAMPLE RATE)
12.288	0000 (=1)	12.288	32
	0001 (=1.5)	8.192	32
	0010 (=2)	6.144	32
	0011 (=3)	4.096	32
	0100 (=4)	3.072	32
	0101 (=5.5)	2.2341818	20
	0110 (=6)	2.048	20
	0111 (=8)	1.536	16
	1000 (=11)	1.117091	8
	1001 (=12)	1.024	8
	1010 (=16)	0.768	8
	1011 (=22)	0.558545	N/A
	1100 (=24)	0.512	N/A
	1101 (=32)	0.384	N/A
	1110 (=32)	0.384	N/A
	1111 (=32)	0.384	N/A
11.2896	0000 (=1)	11.2896	32
	0001 (=1.5)	7.5264	32
	0010 (=2)	5.6448	32
	0011 (=3)	3.7632	32
	0100 (=4)	2.8224	32
	0101 (=5.5)	2.052655	20
	0110 (=6)	1.8816	20
	0111 (=8)	1.4112	16
	1000 (=11)	1.026327	8
	1001 (=12)	0.9408	8
	1010 (=16)	0.7056	8
	1011 (=22)	0.513164	N/A
	1100 (=24)	0.4704	N/A
	1101 (=32)	0.3528	N/A
	1110 (=32)	0.3528	N/A
	1111 (=32)	0.3528	N/A

Table 33 BCLK Divider in Master Mode

OTHER SAMPLE RATE CONTROL BITS

The de-emphasis filter and 3D stereo enhance functions all need to be configured for the chosen sample rate when in use, as show in Table 34.

DEEMPH, 3DUC and 3DUC should be configured to match the chosen DAC sample rate.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) DAC Control (1)	2:1	DEEMPH [1:0]	00	De-Emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No de-emphasis
R16 (10h) 3D Enhance	6	3DUC	0	Upper Cut-Off Frequency 0 = High (Recommended for fs>=32kHz) 1 = Low (Recommended for fs<32kHz)
	5	3DLC	0	Lower Cut-Off Frequency 0 = Low (Recommended for fs>=32kHz) 1 = High (Recommended for fs<32kHz)

Table 34 Additional Sample Rate Controls

PLL

The integrated PLL can be used to generate SYSCLK for the WM8956 or provide clocking for external devices via the GPIO1 pin.

The PLL is enabled by the PLLEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 (1Ah) Power management (2)	0	PLLEN	0	PLL Enable 0 = PLL off 1 = PLL on
R52 (34h) PLL (1)	5	SDM	0	Enable Integer Mode 0 = Integer mode 1 = Fractional mode

Table 35 PLLEN Control Bit

The PLL frequency ratio R = f_2/f_1 (See Figure 34) can be set using the register bits PLLK and PLLN:

PLLN = int R

PLLK = int (2^{24} (R-PLLN))

EXAMPLE:

MCLK=12MHz, required clock = 12.288MHz.

R should be chosen to ensure 5 < PLLN < 13. There is a fixed divide by 4 in the PLL and a selectable divide by N after the PLL which should be set to divide by 2 to meet this requirement.

Enabling the divide by 2 sets the required f_2 = 4 x 2 x 12.288MHz = 98.304MHz.

R = 98.304 / 12 = 8.192

PLLN = int R = 8

k = int (2^{24} x (8.192 – 8)) = 3221225 = 3126E9h

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R52 (34h) PLL N value	4	PLLPRESCALE	0	Divide MCLK by 2 before input to PLL 0 = Divide by 1 1 = Divide by 2
	3:0	PLLN	8h	Integer (N) part of PLL input/output frequency ratio. Use values greater than 5 and less than 13.
R53 (35h) PLL K value (1)	5:0	PLLK [23:16]	31h	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).
R54 (36h) PLL K Value (2)	8:0	PLLK [15:8]	26h	
R55 (37h) PLL K Value (3)	8:0	PLLK [7:0]	E9h	

Table 36 PLL Frequency Ratio Control

The PLL performs best when f_2 is between 90MHz and 100MHz. Its stability peaks at N=8. Some example settings are shown in Table 37.

MCLK (MHz) (f1)	**DESIRED OUTPUT (SYSCLK)** (MHz)	**f2** (MHz)	**PRESCALE DIVIDE (PLLPRESCALE)**	**POSTSCALE DIVIDE (SYSCLKDIV[1:0])**	**FIXED POST-DIVIDE**	**R**	**N**	**K**
12	11.2896	90.3168	1	2	4	7.5264	7h	86C226h
12	12.288	98.304	1	2	4	8.192	8h	3126E8h
13	11.2896	90.3168	1	2	4	6.947446	6h	F28BD4h
13	12.288	98.304	1	2	4	7.561846	7h	8FD525h
14.4	11.2896	90.3168	1	2	4	6.272	6h	45A1CAh
14.4	12.288	98.304	1	2	4	6.826667	6h	D3A06Eh
19.2	11.2896	90.3168	2	2	4	9.408	9h	6872AFh
19.2	12.288	98.304	2	2	4	10.24	Ah	3D70A3h
19.68	11.2896	90.3168	2	2	4	9.178537	9h	2DB492h
19.68	12.288	98.304	2	2	4	9.990243	9h	FD809Fh
19.8	11.2896	90.3168	2	2	4	9.122909	9h	1F76F7h
19.8	12.288	98.304	2	2	4	9.929697	9h	EE009Eh
24	11.2896	90.3168	2	2	4	7.5264	7h	86C226h
24	12.288	98.304	2	2	4	8.192	8h	3126E8h
26	11.2896	90.3168	2	2	4	6.947446	6h	F28BD4h
26	12.288	98.304	2	2	4	7.561846	7h	8FD525h
27	11.2896	90.3168	2	2	4	6.690133	6h	B0AC93h
27	12.288	98.304	2	2	4	7.281778	7h	482296h

Table 37 PLL Frequency Examples

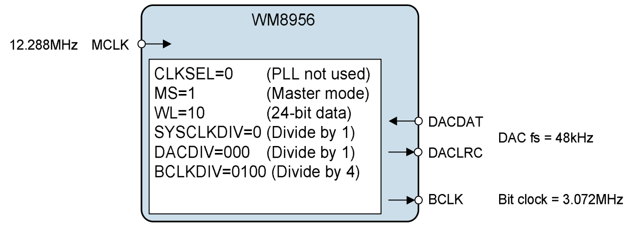
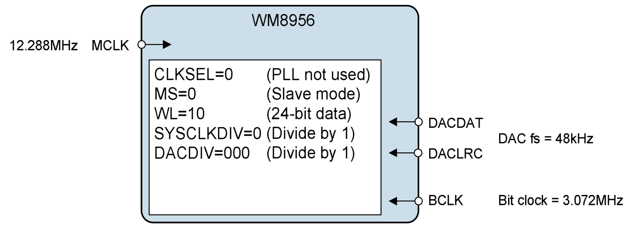
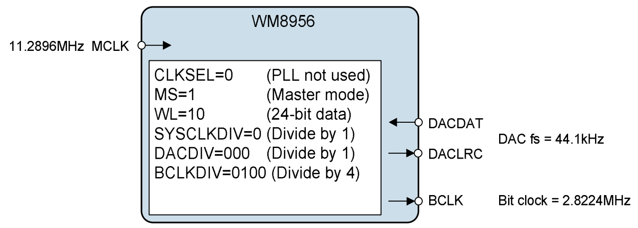
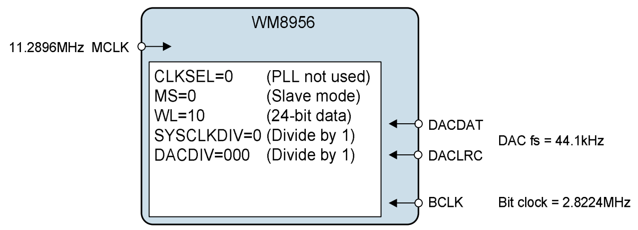
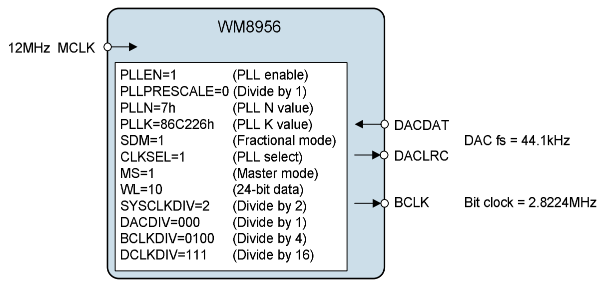
	Device running in master mode with 24-bit data MCLK input at 12.288MHz DAC running at fs=48kHz BCLK running at 64fs
	Device running in slave mode with 24-bit data MCLK input at 12.288MHz DAC running at fs=48kHz BCLK supplied from host at 64fs in this example
	Device running in master mode with 24-bit data MCLK input at 11.2896MHz DAC running at fs=44.1kHz BCLK running at 64fs in this example
	Device running in slave mode with 24-bit data MCLK input at 11.2896MHz DAC running at fs=44.1kHz BCLK supplied from host at 64fs in this example.
	Device running in master mode with 24-bit data MCLK input at 12MHz PLL Enabled and configured for SYSCLK=11.2896MHz DAC running at fs=44.1kHz BCLK running at 64fs in this example Class D clocks running at 705.6kHz

Table 38 Example Clocking Schemes

CONTROL INTERFACE

2-WIRE SERIAL CONTROL INTERFACE

The WM8956 is controlled by writing to registers through a 2-wire serial control interface. A control word consists of 16 bits. The first 7 bits (B15 to B9) are address bits that select which control register is accessed. The remaining 9 bits (B8 to B0) are data bits, corresponding to the 9 bits in each control register. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the WM8956).

The device address is 0011010 (**0x34h**).

The WM8956 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8956 and the R/W bit is ‘0’, indicating a write, then the WM8956 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is ‘1’, the WM8956 returns to the idle condition and wait for a new start condition and valid address.

Once the WM8956 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8956 register address plus the first bit of register data). The WM8956 then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8956 acknowledges again by pulling SDIN low.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8956 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

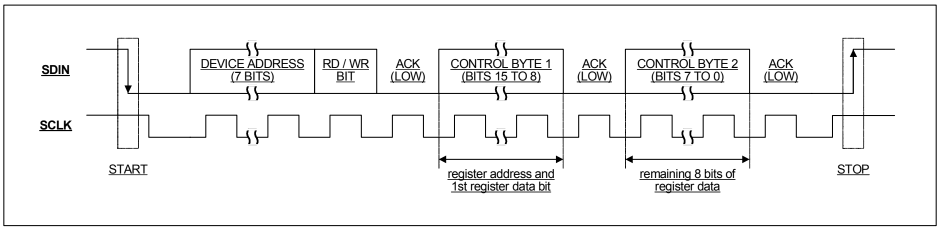


Figure 35 2-Wire Serial Control Interface

POWER MANAGEMENT

The WM8956 has three control registers that allow users to select which functions are active. For minimum power consumption, unused functions should be disabled. To avoid any pop or click noise, it is important to enable or disable functions in the correct order (see Applications Information). VMIDSEL is the enable for the Vmid reference, which defaults to disabled and can be enabled as a 2x50kΩ potential divider or, for low power maintenance of Vref when all other blocks are disabled, as a 2x250kΩ potential divider.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power Management (1)	8:7	VMIDSEL	00	Vmid Divider Enable and Select 00 = Vmid disabled (for OFF mode) 01 = 2 x 50kΩ divider enabled (for playback / record) 10 = 2 x 250kΩ divider enabled (for low-power standby) 11 = 2 x 5kΩ divider enabled (for fast start-up)
	6	VREF	0	VREF (necessary for all other functions) 0 = Power down 1 = Power up
	5	AINL	0	Analogue Input PGA and Boost Left 0 = Power down 1 = Power up (Note: LMIC must also be set to enable the PGA)
	4	AINR	0	Analogue Input PGA and Boost Right 0 = Power down 1 = Power up (Note: RMIC must also be set to enable the PGA)
	1	MICB	0	MICBIAS 0 = Power down 1 = Power up
	0	DIGENB	0	Master Clock Disable 0 = Master clock enabled 1 = Master clock disabled
R26 (1Ah) Power Management (2)	8	DACL	0	DAC Left 0 = Power down 1 = Power up
	7	DACR	0	DAC Right 0 = Power down 1 = Power up
	6	LOUT1	0	LOUT1 Output Buffer 0 = Power down 1 = Power up
	5	ROUT1	0	ROUT1 Output Buffer 0 = Power down 1 = Power up
	4	SPKL	0	SPK_LP/SPK_LN Output PGA. 0 = Power down 1 = Power up (Note: Speaker output also requires SPK_OP_EN[0] to be set)
	3	SPKR	0	SPK_RP/SPK_RN Output PGA 0 = Power down 1 = Power up (Note: Speaker output also requires SPK_OP_EN[1] to be set)
	1	OUT3	0	OUT3 Output Buffer 0 = Power down 1 = Power up

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	0	PLL_EN	0	PLL Enable 0 = Power down 1 = Power up
R47 (2Fh) Power Management (3)	5	LMIC		Left Input PGA Enable 0 = Power down 1 = Power up (Note: PGA also requires AINL to be set)
	4	RMIC		RIght Input PGA Enable 0 = Power down 1 = Power up (Note: PGA also requires AINR to be set)
	3	LOMIX		Left Output Mixer Enable 0 = Power down 1 = Power up
	2	ROMIX		Right Output Mixer Enable 0 = Power down 1 = Power up

Table 39 Power Management

STOPPING THE MASTER CLOCK

In order to minimise power consumed in the digital core of the WM8956, the master clock may be stopped in Standby and OFF modes. If this cannot be done externally at the clock source, the DIGENB bit (R25, bit 0) can be set to stop the MCLK signal from propagating into the device core. In Standby mode, setting DIGENB will typically provide an additional power saving on DCVDD of 20uA. However, since setting DIGENB has no effect on the power consumption of other system components external to the WM8956, it is preferable to disable the master clock at its source wherever possible.

MCLK should not be stopped while the class D outputs are enabled, as this would prevent the outputs from functioning.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Additional Control (1)	0	DIGENB	0	Master clock disable 0 = Master clock enabled 1 = Master clock disabled

Table 40 Enabling the Master Clock

NOTE: Before DIGENB can be set, the control bits DACL and DACR must be set to zero and a waiting time of 1ms must be observed. Any failure to follow this procedure may prevent DACs from re-starting correctly.

SAVING POWER AT HIGHER SUPPLY VOLTAGE

The AVDD supply of the WM8956 can operate beteen 2.7V and 3.6V. By default, all analogue circuitry on the device is optimized to run at 3.3V. This set-up is also good for all other supply voltages down to 2.7V. At lower voltages, performance can be improved by increasing the bias current by setting VSEL[1:0] = 01. If low power operation is preferred the bias current can be left at the default setting. This is controlled as shown below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	7:6	VSEL [1:0]	11	Analogue Bias Optimisation 00 = Reserved 01 = Increased bias current, optimized for AVDD=2.7V 1X = Lowest bias current, optimized for AVDD=3.3V

Table 41 Bias Optimisation

REGISTER MAP

REGISTER	remarks	Bit[8]	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]	default
R0 (00h)	Left Input volume	IPVU	LINMUTE	LIZC	LINVOL[5:0]						0_1001_0111
R1 (01h)	Right Input volume	IPVU	RINMUTE	RIZC	RINVOL[5:0]						0_1001_0111
R2 (02h)	LOUT1 volume	OUT1VU	LO1ZC	LOUT1VOL[6:0]							0_0000_0000
R3 (03h)	ROUT1 volume	OUT1VU	RO1ZC	ROUT1VOL[6:0]							0_0000_0000
R4 (04h)	Clocking (1)	0	0	0	DACDIV[2:0]			SYSCLKDIV[1:0]		CLKSEL	0_0000_0000
R5 (05h)	DAC Control (CTR1)	0	DACDIV2	0	0	0	DACMU	DEEMPH[1:0]		0	0_0000_1000
R6 (06h)	DAC Control (CTR2)	0	0	DACPOL[1:0]		0	DACSMM	DACMR	DACSLOPE	0	0_0000_0000
R7 (07h)	Audio Interface	0	BCLKINV	MS	DLRSWAP	LRP	WL[1:0]		FORMAT[1:0]		0_0000_1010
R8 (08h)	Clocking (2)	DCLKDIV[2:0]			0	0	BCLKDIV[3:0]				1_1100_0000
R9 (09h)	Audio Interface	0	0	ALRCGPIO	WL8	DACCOMP[1:0]		0	0	0	0_0000_0000
R10 (0Ah)	Left DAC volume	DACVU	LDACVOL[7:0]								0_1111_1111
R11 (0Bh)	Right DAC volume	DACVU	RDACVOL[7:0]								0_1111_1111
R12 (0Ch)	Reserved	0	0	0	0	0	0	0	0	0	0_0000_0000
R13 (0Dh)	Reserved	0	0	0	0	0	0	0	0	0	0_0000_0000
R14 (0Eh)	Reserved	0	0	0	0	0	0	0	0	0	0_0000_0000
R15 (0Fh)	Reset	writing to this register resets all registers to their default state									not reset
R16 (10h)	3D control	0	0	3DUC	3DLC	3DDEPTH[3:0]				3DEN	0_0000_0000
R17 (11h)	Reserved	0	0	1	1	1	1	0	1	1	0_0111_1011
R18 (12h)	Reserved	1	0	0	0	0	0	0	0	0	1_0000_0000
R19 (13h)	Reserved	0	0	0	1	1	0	0	1	0	0_0011_0010
R20 (14h)	Reserved	0	0	0	0	0	0	0	0	0	0_0000_0000
R21 (15h)	Reserved	0	1	1	0	0	0	0	1	1	0_1100_0011
R22 (16h)	Reserved	0	1	1	0	0	0	0	1	1	0_1100_0011
R23 (17h)	Additional control(1)	TSDEN	VSEL[1:0]		0	DMONOMIX	0	0	TOCLKSEL	TOEN	1_1100_0000
R24 (18h)	Additional control(2)	0	0	HPSWEN	HPSWPOL	0	TRIS	0	0	0	0_0000_0000
R25 (19h)	Pwr Mgmt (1)	VMIDSEL[1:0]		VREF	AINL	AINR	0	0	MICB	DIGENB	0_0000_0000
R26 (1Ah)	Pwr Mgmt (2)	DACL	DACR	LOUT1	ROUT1	SPKL	SPKR	0	OUT3	PLL_EN	0_0000_0000
R27 (1Bh)	Additional Control (3)	0	0	VROI	0	0	OUT3CAP	0	0	0	0_0000_0000
R28 (1Ch)	Anti-pop 1	0	POBCTRL	0	0	BUFDCOPEN	BUFIOEN	SOFT_ST	0	HPSTBY	0_0000_0000
R29 (1Dh)	Anti-pop 2	0	0	DISOP	DRES[1:0]		0	0	0	0	0_0000_0000
R30 (1Eh)	Reserved	0	0	0	0	0	0	0	0	0	0_0000_0000
R31 (1Fh)	Reserved	0	0	0	0	0	0	0	0	0	0_0000_0000
R32 (20h)	L input signal path	LMN1	LMP3	LMP2	LMICBOOST[1:0]		LMIC2B	0	0	0	1_0000_0000
R33 (21h)	R input signal path	RMN1	RMP3	RMP2	RMICBOOST[1:0]		RMIC2B	0	0	0	1_0000_0000
R34 (22h)	Left out Mix (1)	LD2LO	LI2LO	LI2LOVOL[2:0]			0	0	0	0	0_0101_0000
R35 (23h)	Reserved	0	0	1	0	1	0	0	0	0	0_0101_0000
R36 (24h)	Reserved	0	0	1	0	1	0	0	0	0	0_0101_0000
R37 (25h)	Right out Mix (2)	RD2RO	RI2RO	RI2ROVOL[2:0]			0	0	0	0	0_0101_0000
R38 (26h)	Mono out Mix (1)	0	L2MO	0	0	0	0	0	0	0	0_0000_0000
R39 (27h)	Mono out Mix (2)	0	R2MO	0	0	0	0	0	0	0	0_0000_0000
R40 (28h)	LOUT2 volume	SPKVU	SPKLZC	SPKLVOL[6:0]							0_0000_0000
R41 (29h)	ROUT2 volume	SPKVU	SPKRZC	SPKRVOL[6:0]							0_0000_0000
R42 (2Ah)	MONOOUT volume	0	0	MOUTVOL	0	0	0	0	0	0	0_0100_0000
R43 (2Bh)	Input boost mixer (1)	0	0	LIN3BOOST[2:0]			LIN2BOOST[2:0]			0	0_0000_0000
R44 (2Ch)	Input boost mixer (2)	0	0	RIN3BOOST[2:0]			RIN2BOOST[2:0]			0	0_0000_0000
R45 (2Dh)	Bypass (1)	0	LB2LO	LB2LOVOL[2:0]			0	0	0	0	0_0101_0000
R46 (2Eh)	Bypass (2)	0	RB2RO	RB2ROVOL[2:0]			0	0	0	0	0_0101_0000
R47 (2Fh)	Pwr Mgmt (3)	0	0	0	LMIC	RMIC	LOMIX	ROMIX	0	0	0_0000_0000
R48 (30h)	Additional Control (4)	0	GPIOPOL	GPIOSEL[2:0]			HPSEL[1:0]		TSENSEN	MBSEL	0_0000_0010
R49 (31h)	Class D Control (1)	0	SPK_OP_EN[1:0]		1	1	0	1	1	1	0_0011_0111
R50 (32h)	Reserved	0	0	1	0	0	1	1	0	1	0_0100_1101
R51 (33h)	Class D Control (3)	0	1	0	DCGAIN[2:0]			ACGAIN[2:0]			0_1000_0000
R52 (34h)	PLL N	OPCLKDIV[2:0]			SDM	PLLRESCALE	PLLN[3:0]				0_0000_1000
R53 (35h)	PLL K 1	0	PLLK[23:16]								0_0011_0001
R54 (36h)	PLL K 2	0	PLLK[15:8]								0_0010_0110
R55 (37h)	PLL K 3	0	PLLK[7:0]								0_1110_1001

REGISTER BITS BY ADDRESS

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R0 (00h) Left Input Volume	8	IPVU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause left and right input PGA volumes to be updated (LINVOL and RINVOL)	Input Signal Path
	7	LINMUTE	1	Left Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.	Input Signal Path
	6	LIZC	0	Left Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately	Input Signal Path
	5:0	LINVOL[5:0]	010111	Left Input PGA Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB	Input Signal Path
R1 (01h) Right Input Volume	8	IPVU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause left and right input PGA volumes to be updated (LINVOL and RINVOL)	Input Signal Path
	7	RINMUTE	1	Right Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.	Input Signal Path
	6	RIZC	0	Right Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately	Input Signal Path
	5:0	RINVOL[5:0]	010111	Right Input PGA Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB	Input Signal Path
R2 (02h) LOUT1 Volume	8	OUT1VU	N/A	Headphone Output PGA Volume Update Writing a 1 to this bit will cause left and right headphone output volumes to be updated (LOUT1VOL and ROUT1VOL)	Analogue Outputs
	7	LO1ZC	0	Left Headphone Output Zero Cross Enable 0 = Change gain immediately 1 = Change gain on zero cross only	Analogue Outputs
	6:0	LOUT1VOL[6:0]	0000000	LOUT1 Volume 1111111 = +6dB … 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE	Analogue Outputs
R3 (03h) ROUT1 Volume	8	OUT1VU	N/A	Headphone Output PGA Volume Update Writing a 1 to this bit will cause left and right headphone output volumes to be updated (LOUT1VOL and ROUT1VOL)	Analogue Outputs
	7	RO1ZC	0	Right Headphone Output Zero Cross Enable 0 = Change gain immediately 1 = Change gain on zero cross only	Analogue Outputs

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:0	ROUT1VOL[6:0]	0000000	ROUT1 Volume 1111111 = +6dB … 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE	Analogue Outputs
R4 (04h) Clocking (1)	8:6		000	Reserved	
	5:3	DACDIV[2:0]	000	DAC Sample rate divider (Also determines DACLRC in master mode) 000 = SYSCLK / (1.0 * 256) 001 = SYSCLK / (1.5 * 256) 010 = SYSCLK / (2 * 256) 011 = SYSCLK / (3 * 256) 100 = SYSCLK / (4 * 256) 101 = SYSCLK / (5.5 * 256) 110 = SYSCLK / (6 * 256) 111 = Reserved	Clocking and Sample Rates
	2:1	SYSCLKDIV[1:0]	00	SYSCLK Pre-divider. Clock source (MCLK or PLL output) will be divided by this value to generate SYSCLK. 00 = Divide SYSCLK by 1 01 = Reserved 10 = Divide SYSCLK by 2 11 = Reserved	Clocking and Sample Rates
	0	CLKSEL	0	SYSCLK Selection 0 = SYSCLK derived from MCLK 1 = SYSCLK derived from PLL output	Clocking and Sample Rates
R5 (05h) DAC Control (1)	8		0	Reserved	
	7	DACDIV2	0	DAC 6dB Attenuate Enable 0 = Disabled (0dB) 1 = -6dB Enabled	Output Signal Path
	6:4		000	Reserved	
	3	DACMU	1	DAC Digital Soft Mute 1 = Mute 0 = No mute (signal active)	Output Signal Path
	2:1	DEEMPH[1:0]	00	De-emphasis Control 11 = 48kHz sample rate 10 = 44.1kHz sample rate 01 = 32kHz sample rate 00 = No de-emphasis	Output Signal Path
	0		0	Reserved	
R6 (06h) DAC Control (2)	8:7		00	Reserved	
	6:5	DACPOL[1:0]	00	DAC polarity control: 00 = Polarity not inverted 01 = DAC L inverted 10 = DAC R inverted 11 = DAC L and R inverted	Output Signal Path
	4		0	Reserved	
	3	DACSMM	0	DAC Soft Mute Mode 0 = Disabling soft-mute (DACMU=0) will cause the volume to change immediately to the LDACVOL / RDACVOL settings 1 = Disabling soft-mute (DACMU=0) will cause the volume to ramp up gradually to the LDACVOL / RDACVOL settings	Output Signal Path

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2	DACMR	0	DAC Soft Mute Ramp Rate 0 = Fast ramp (fs/2, providing maximum delay of 10.7ms at fs=48k) 1 = Slow ramp (fs/32, providing maximum delay of 171ms at fs=48k)	Output Signal Path
	1	DACSLOPE	0	Selects DAC filter characteristics 0 = Normal mode 1 = Sloping stopband	Output Signal Path
	0		0	Reserved	
R7 (07h) Audio Interface	8		0	Reserved	
	7	BCLKINV	0	BCLK invert bit (for master and slave modes) 0 = BCLK not inverted 1 = BCLK inverted	Audio Interface Control
	6	MS	0	Master / Slave Mode Control 0 = Enable slave mode 1 = Enable master mode	Audio Interface Control
	5	DLRSWAP	0	Left/Right DAC Channel Swap 0 = Output left and right data as normal 1 = Swap left and right DAC data in audio interface	Audio Interface Control
	4	LRP	0	Right, left and I^{2}S modes – LRCLK polarity 0 = normal LRCLK polarity 1 = invert LRCLK polarity	Audio Interface Control
				DSP Mode – mode A/B select 0 = MSB is available on 2nd BCLK rising edge after LRC rising edge (mode A) 1 = MSB is available on 1st BCLK rising edge after LRC rising edge (mode B)	
	3:2	WL[1:0]	10	Audio Data Word Length 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits (see Note)	Audio Interface Control
	1:0	FORMAT[1:0]	10	00 = Right justified 01 = Left justified 10 = I^{2}S Format 11 = DSP Mode	Audio Interface Control
R8 (08h) Clocking (2)	8:6	DCLKDIV[2:0]	111	Class D switching clock divider. 000 = SYSCLK / 1.5 (Not recommended) 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 6 101 = SYSCLK / 8 110 = SYSCLK / 12 111 = SYSCLK / 16	Class D Speaker Outputs; Clocking and Sample Rates
	5:4		00	Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	3:0	BCLKDIV[3:0]	0000	BCLK Frequency (Master Mode) 0000 = SYSCLK 0001 = SYSCLK / 1.5 0010 = SYSCLK / 2 0011 = SYSCLK / 3 0100 = SYSCLK / 4 0101 = SYSCLK / 5.5 0110 = SYSCLK / 6 0111 = SYSCLK / 8 1000 = SYSCLK / 11 1001 = SYSCLK / 12 1010 = SYSCLK / 16 1011 = SYSCLK / 22 1100 = SYSCLK / 24 1101 to 1111 = SYSCLK / 32	Clocking and Sample Rates
R9 (09h) Audio Interface	8:7		00	Reserved	
	6	ALRCGPIO	0	GPIO1 Pin Function Select 0 = GPIO pin function disabled 1 = GPIO pin function enabled	General Purpose Input / Output; Digital Audio Interface
	5	WL8	0	8-Bit Word Length Select (Used with companding) 0 = Off 1 = Device operates in 8-bit mode.	Audio Interface Control
	4:3	DACCOMP[1:0]	00	DAC companding 00 = off 01 = reserved 10 = μ-law 11 = A-law	Audio Interface Control
	2:0		000	Reserved	
R10 (0Ah) Left DAC Volume	8	DACVU	N/A	DAC Volume Update Writing a 1 to this bit will cause left and right DAC volumes to be updated (LDACVOL and RDACVOL)	Output Signal Path
	7:0	LDACVOL[7:0]	11111111	Left DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB	Output Signal Path
R11 (0Bh) Right DAC Volume	8	DACVU	N/A	DAC Volume Update Writing a 1 to this bit will cause left and right DAC volumes to be updated (LDACVOL and RDACVOL)	Output Signal Path
	7:0	RDACVOL[7:0]	11111111	Right DAC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB	Output Signal Path
R12 (0Ch)	8:0		000000000	Reserved	
R13 (0Dh)	8:0		000000000	Reserved	
R14 (0Eh)	8:0		000000000	Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R15 (0Fh) Reset	8:0	Reset	N/A	Writing to this register resets all registers to their default state.	
R16 {10h) 3D Control	8		0	Reserved	
	7		0	Reserved	
	6	3DUC	0	3D Enhance Filter Upper Cut-Off Frequency 0 = High (Recommended for fs>=32kHz) 1 = Low (Recommended for fs<32kHz)	Output Signal Path
	5	3DLC	0	3D Enhance Filter Lower Cut-Off Frequency 0 = Low (Recommended for fs>=32kHz) 1 = High (Recommended for fs<32kHz)	Output Signal Path
	4:1	3DDEPTH[3:0]	0000	3D Stereo Depth 0000 = 0% (minimum 3D effect) 0001 = 6.67% .... 1110 = 93.3% 1111 = 100% (maximum 3D effect)	Output Signal Path
	0	3DEN	0	3D Stereo Enhancement Enable 0 = Disabled 1 = Enabled	Output Signal Path
R17 (11h)	8:0		0000001011	Reserved	
R18 (12h)	8:0		100000000	Reserved	
R19 (13h)	8:0		000110010	Reserved	
R20 (14h)	8:0		000000000	Reserved	
R21 (15h)	8:0		011000011	Reserved	
R22 (16h)	8:0		011000011	Reserved	
R23 (17h) Additional Control (1)	8	TSDEN	1	Thermal Shutdown Enable 0 = Thermal shutdown disabled 1 = Thermal shutdown enabled (TSENSEN must be enabled for this function to work)	Thermal Shutdown
	7:6	VSEL[1:0]	11	Analogue Bias Optimisation 00 = Reserved 01 = Bias current optimized for AVDD=2.7V 1X = Lowest bias current, optimized for AVDD=3.3V	Power Management
	5		0	Reserved	
	4	DMONOMIX	0	DAC Mono Mix 0 = Stereo 1 = Mono (Mono MIX output on enabled DACs)	Output Signal Path
	3:2		00	Reserved	
	1	TOCLKSEL	0	Slow Clock Select (Used for volume update timeouts and for jack detect debounce) 0 = SYSCLK / 2^{21} (Slower Response) 1 = SYSCLK / 2^{19} (Faster Response)	Volume Updates; Headphone Jack Detect
	0	TOEN	0	Enables Slow Clock for Volume Update Timeout and Jack Detect Debounce 0 = Slow clock disabled 1 = Slow clock enabled	Volume Updates; Headphone Jack Detect
R24 (18h) Additional Control (2)	8:7		00	Reserved	
	6	HPSWEN	0	Headphone Switch Enable 0 = Headphone switch disabled 1 = Headphone switch enabled	Headphone Jack Detect

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	5	HPSWPOL	0	Headphone Switch Polarity 0 = HPDETECT high = headphone 1 = HPDETECT high = speaker	Headphone Jack Detect
	4			Reserved	
	3	TRIS	0	Switches DACLRC and BCLK to inputs. 0 = DACLRC and BCLK are inputs (slave mode) or outputs (master mode) 1 = DACLRC and BCLK are inputs	Audio Interface Control
	2:0		000	Reserved	
R25 (19h) Power Mgmt (1)	8:7	VMIDSEL[1:0]	00	Vmid Divider Enable and Select 00 = Vmid disabled (for OFF mode) 01 = 2 x 50kΩ divider enabled (for playback / record) 10 = 2 x 250kΩ divider enabled (for low-power standby) 11 = 2 x 5kΩ divider enabled (for fast start-up)	Power Management
	6	VREF	0	VREF (necessary for all other functions) 0 = Power down 1 = Power up	Power Management
	5	AINL	0	Analogue in PGA Left 0 = Power down 1 = Power up	Power Management
	4	AINR	0	Analogue in PGA Right 0 = Power down 1 = Power up	Power Management
	3:2		00	Reserved	
	1	MICB	0	MICBIAS 0 = Power down 1 = Power up	Power Management
	0	DIGENB	0	Master Clock Disable 0 = Master clock enabled 1 = Master clock disabled	Power Management
R26 (1Ah) Power Mgmt (2)	8	DACL	0	DAC Left 0 = Power down 1 = Power up	Power Management
	7	DACR	0	DAC Right 0 = Power down 1 = Power up	Power Management
	6	LOUT1	0	LOUT1 Output Buffer 0 = Power down 1 = Power up	Power Management
	5	ROUT1	0	ROUT1 Output Buffer 0 = Power down 1 = Power up	Power Management
	4	SPKL	0	SPK_LP/SPK_LN Output Buffers 0 = Power down 1 = Power up	Power Management
	3	SPKR	0	SPK_RP/SPK_RN Output Buffers 0 = Power down 1 = Power up	Power Management
	2		0	Reserved	
	1	OUT3	0	OUT3 Output Buffer 0 = Power down 1 = Power up	Power Management

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	0	PLL_EN	0	PLL Enable 0 = Power down 1 = Power up	Power Management
R27 (1Bh) Additional Control (3)	8:7		00	Reserved	
	6	VROI	0	VREF to Analogue Output Resistance (Disabled Outputs) 0 = 500Ω VMID to output 1 = 20kΩ VMID to output	Enabling the Outputs
	5		0	Reserved	
	4		0	Reserved	
	3	OUT3CAP	0	Capless Mode Headphone Switch Enable 0 = OUT3 unaffected by jack detect events 1 = OUT3 enabled and disabled together with HP_L and HP_R in response to jack detect events	Headphone Jack Detect
	2:0		000	Reserved	
R28 (1Ch) Anti-Pop	8		0	Reserved	
	7	POBCTRL	0	Selects the bias current source for output amplifiers and VMID buffer 0 = VMID / R bias 1 = VGS / R bias	
	6:5		00	Reserved	
	4	BUFDCOPEN	0	Enables the VGS / R current generator 0 = Disabled 1 = Enabled	
	3	BUFIOEN	0	Enables the VGS / R current generator and the analogue input and output bias 0 = Disabled 1 = Enabled	
	2	SOFT_ST	0	Enables VMID soft start 0 = Disabled 1 = Enabled	
	1		0	Reserved	
	0	HPSTBY	0	Headphone Amplifier Standby 0 = Standby mode disabled (Normal operation) 1 = Standby mode enabled	
R29 (1Dh)	8:7		00	Reserved	
	6	DISOP	0	Discharges the DC-blocking headphone capacitors on HP_L and HP_R 0 = Enabled 1 = Disabled	
	5:4	DRES[1:0]	00	DRES determines the value of the resistors used to discharge the DC-blocking headphone capacitors when DISOP=1 D600 D200 Resistance 0 0 400 0 1 200 1 0 600 1 1 150	
	3:0		0000	Reserved	
R30 (1Eh)	8:0		000000000	Reserved	
R31 (1Fh)	8:0		000000000	Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
R32 (20h) Left Input Signal Path	8	LMN1	1	Connect LINPUT1 to inverting input of Left Input PGA 0 = LINPUT1 not connected to PGA 1 = LINPUT1 connected to PGA	Input Signal Path
	7	LMP3	0	Connect LINPUT3 to non-inverting input of Left Input PGA 0 = LINPUT3 not connected to PGA 1 = LINPUT3 connected to PGA (Constant input impedance)	Input Signal Path
	6	LMP2	0	Connect LINPUT2 to non-inverting input of Left Input PGA 0 = LINPUT2 not connected to PGA 1 = LINPUT2 connected to PGA (Constant input impedance)	Input Signal Path
	5:4	LMICBOOST[1:0]	00	Left Channel Input PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB	Input Signal Path
	3	LMIC2B	0	Connect Left Input PGA to Left Input Boost Mixer 0 = Not connected 1 = Connected	Input Signal Path
	2:0		000	Reserved	
R33 (21h) Right Input Signal Path	8	RMN1	1	Connect RINPUT1 to inverting input of Right Input PGA 0 = RINPUT1 not connected to PGA 1 = RINPUT1 connected to PGA	Input Signal Path
	7	RMP3	0	Connect RINPUT3 to non-inverting input of Right Input PGA 0 = RINPUT3 not connected to PGA 1 = RINPUT3 connected to PGA (Constant input impedance)	Input Signal Path
	6	RMP2	0	Connect RINPUT2 to non-inverting input of Right Input PGA 0 = RINPUT2 not connected to PGA 1 = RINPUT2 connected to PGA (Constant input impedance)	Input Signal Path
	5:4	RMICBOOST[1:0]	00	Right Channel Input PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB	Input Signal Path
	3	RMIC2B	0	Connect Right Input PGA to Right Input Boost Mixer 0 = Not connected 1 = Connected	Input Signal Path
	2:0		000	Reserved	
R34 (22h) Left Out Mix	8	LD2LO	0	Left DAC to Left Output Mixer 0 = Disable (Mute) 1 = Enable Path	Output Signal Path
	7	LI2LO	0	LINPUT3 to Left Output Mixer 0 = Disable (Mute) 1 = Enable Path	Output Signal Path

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	6:4	LI2LOVOL[2:0]	101	LINPUT3 to Left Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB	Output Signal Path
	3:0		0000	Reserved	
R35 (23h)	8:0		001010000	Reserved	
R36 (24h)	8:0		001010000	Reserved	
R37 (25h) Right Out Mix	8	RD2RO	0	Right DAC to Right Output Mixer 0 = Disable (Mute) 1 = Enable Path	Output Signal Path
	7	RI2RO	0	RINPUT3 to Right Output Mixer 0 = Disable (Mute) 1 = Enable Path	Output Signal Path
	6:4	RI2ROVOL[2:0]	101	RINPUT3 to Right Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB	Output Signal Path
	3:0		0000	Reserved	
R38 (26h) Mono Out Mix (1)	8		0	Reserved	
	7	L2MO	0	Left Output Mixer to Mono Output Mixer Control 0 = Left channel mix disabled 1 = Left channel mix enabled	Output Signal Path
	6:0		0000000	Reserved	
R39 (27h) Mono Out Mix (2)	8		0	Reserved	
	7	R2MO	0	Right Output Mixer to Mono Output Mixer Control 0 = Right channel mix disabled 1 = Right channel mix enabled	Output Signal Path
	6:0		0000000	Reserved	
R40 (28h) Left Speaker Volume	8	SPKVU	N/A	Speaker Volume Update Writing a 1 to this bit will cause left and right speaker volumes to be updated (SPKLVOL and SPKRVOL)	Analogue Outputs
	7	SPKLZC	0	Left Speaker Zero Cross Enable 1 = Change gain on zero cross only 0 = Change gain immediately	Analogue Outputs
	6:0	SPKLVOL[6:0]	0000000	SPK_LP/SPK_LN Volume 1111111 = +6dB … 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE	Analogue Outputs
R41 (29h) Right Speaker Volume	8	SPKVU	N/A	Speaker Volume Update Writing a 1 to this bit will cause left and right speaker volumes to be updated (SPKLVOL and SPKRVOL)	Analogue Outputs
	7	SPKRZC	0	Right Speaker Zero Cross Enable 1 = Change gain on zero cross only 0 = Change gain immediately	Analogue Outputs
	6:0	SPKRVOL[6:0]	0000000	SPK_RP/SPK_RN Volume 1111111 = +6dB … 1dB steps down to 0110000 = -73dB 0101111 to 0000000 = Analogue MUTE	Analogue Outputs
R42 (2Ah)	8:7		00	Reserved	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
OUT3 Volume	6	MOUTVOL	1	Mono Output Mixer Volume Control 0 = 0dB 1 = -6dB	Output Signal Path
	5:0		000000	Reserved	
R43 (2Bh)	8:7		00	Reserved	
Left Input Boost Mixer	6:4	LIN3BOOST[2:0]	000	LINPUT3 to Boost Mixer Gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB	Input Signal Path
	3:1	LIN2BOOST[2:0]	000	LINPUT2 to Boost Mixer Gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB	Input Signal Path
	0		0	Reserved	
R44 (2Ch)	8:7		00	Reserved	
Right Input Boost Mixer	6:4	RIN3BOOST[2:0]	000	RINPUT3 to Boost Mixer Gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB	Input Signal Path
	3:1	RIN2BOOST[2:0]	000	RINPUT2 to Boost Mixer Gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB	Input Signal Path
	0		0	Reserved	
R45 (2Dh)	8		0	Reserved	
Left Bypass	7	LB2LO	0	Left Input Boost Mixer to Left Output Mixer 0 = Disable (Mute) 1 = Enable Path	Output Signal Path
	6:4	LB2LOVOL[2:0]	101	Left Input Boost Mixer to Left Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB	Output Signal Path
	3:0		0000	Reserved	
R46 (2Eh)	8		0	Reserved	
Right Bypass	7	RB2RO	0	Right Input Boost Mixer to Right Output Mixer 0 = Disable (Mute) 1 = Enable Path	Output Signal Path
	6:4	RB2ROVOL[2:0]	101	Right Input Boost Mixer to Right Output Mixer Volume 000 = 0dB ...(3dB steps) 111 = -21dB	Output Signal Path
	3:0		0000	Reserved	
R47 (2Fh)	8:6		000	Reserved	
Power Mgmt (3)	5	LMIC	0	Left Channel Input PGA Enable 0 = PGA disabled 1 = PGA enabled (if AINL = 1)	Input Signal Path

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	4	RMIC	0	Right Channel Input PGA Enable 0 = PGA disabled 1 = PGA enabled (if AINR = 1)	Input Signal Path
	3	LOMIX	0	Left Output Mixer Enable Control 0 = Disabled 1 = Enabled	Output Signal Path
	2	ROMIX	0	Right Output Mixer Enable Control 0 = Disabled 1 = Enabled	Output Signal Path
	1:0		00	Reserved	
R48 (30h) Additional Control (4)	8		0	Reserved	
	7	GPIOPOL	0	GPIO Polarity Invert 0 = Non inverted 1 = Inverted	General Purpose Input / Output
	6:4	GPIOSEL[2:0]	000	GPIO1 GPIO Function Select: 000 = Jack detect input 001 = Reserved 010 = Temperature ok 011 = Debounced jack detect output 100 = SYSCLK output 101 = PLL lock 110 = Logic 0 111 = Logic 1	General Purpose Input / Output
	3:2	HPSEL[1:0]	00	Headphone Switch Input Select 0X = GPIO1 used for jack detect input (Requires pin to be configured as a GPIO using ALRCGPIO) 10 = JD2 used for jack detect input 11 = JD3 used for jack detect input	Headphone Jack Detect
	1	TSENSEN	1	Temperature Sensor Enable 0 = Temperature sensor disabled 1 = Temperature sensor enabled	Thermal Shutdown
	0	MBSEL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD	Input Signal Path
R49 (31h) Class D Control (1)	8		0	Reserved	
	7:6	SPK_OP_EN[1:0]	00	Enable Class D Speaker Outputs 00 = Off 01 = Left speaker only 10 = Right speaker only 11 = Left and right speakers enabled	Enabling the Outputs
	5:0		110111	Reserved	
R50 (32h)	8:0		001001101	Reserved	
R51 (33h) Class D Control (2)	8:6		010	Reserved	
	5:3	DCGAIN[2:0]	000	DC Speaker Boost (Boosts speaker DC output level by up to 1.8 x on left and right channels) 000 = 1.00x boost (+0dB) 001 = 1.27x boost (+2.1dB) 010 = 1.40x boost (+2.9dB) 011 = 1.52x boost (+3.6dB) 100 = 1.67x boost (+4.5dB) 101 = 1.8x boost (+5.1dB) 110 to 111 = Reserved	Analogue Outputs

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	REFER TO
	2:0	ACGAIN[2:0]	000	AC Speaker Boost (Boosts speaker AC output signal by up to 1.8 x on left and right channels) 000 = 1.00x boost (+0dB) 001 = 1.27x boost (+2.1dB) 010 = 1.40x boost (+2.9dB) 011 = 1.52x boost (+3.6dB) 100 = 1.67x boost (+4.5dB) 101 = 1.8x boost (+5.1dB) 110 to 111 = Reserved	Analogue Outputs
R52 (34h) PLL (1)	8:6	OPCLKDIV[2:0]	000	SYSCLK Output to GPIO Clock Division ratio 000 = SYSCLK 001 = SYSCLK / 2 010 = SYSCLK / 3 011 = SYSCLK / 4 100 = SYSCLK / 5.5 101 = SYSCLK / 6	General Purpose Input / Output
	5	SDM	0	Enable Integer Mode 0 = Integer mode 1 = Fractional mode	Clocking and Sample Rates
	4	PLLPRESCALE	0	Divide MCLK by 2 before input to PLL 0 = Divide by 1 1 = Divide by 2	Clocking and Sample Rates
	3:0	PLLN[3:0]	1000	Integer (N) part of PLL input/output frequency ratio. Use values greater than 5 and less than 13.	Clocking and Sample Rates
R53 (35h) PLL (2)	8		0	Reserved	
	7:0	PLLK[23:16]	00110001	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Clocking and Sample Rates
R54 (36h) PLL (3)	8		0	Reserved	
	7:0	PLLK[15:8]	00100110	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Clocking and Sample Rates
R55 (37h) PLL (4)	8		0	Reserved	
	7:0	PLLK[7:0]	11101001	Fractional (K) part of PLL1 input/output frequency ratio (treat as one 24-digit binary number).	Clocking and Sample Rates

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Normal Filter					
Passband	+/- 0.03dB	0		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.454 fs			+/- 0.03	dB
Stopband		0.546 fs			
Stopband Attenuation	f > 0.546 fs	-50			dB
DAC Sloping Stopband Filter					
Passband	+/- 0.03dB	0		0.25 fs	
	+/- 1dB	0.25 fs		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.25 fs			+/- 0.03	dB
Stopband 1		0.546 fs		0.7 fs	
Stopband 1 Attenuation	f > 0.546 fs	-60			dB
Stopband 2		0.7 fs		1.4 fs	
Stopband 2 Attenuation	f > 0.7 fs	-85			dB
Stopband 3		1.4 fs			
Stopband 3 Attenuation	f > 1.4 fs	-55			dB

DAC FILTERS	
Mode	**Group Delay**
Normal	18 / fs
Sloping Stopband	18 / fs

DAC FILTER RESPONSES

DAC STOPBAND ATTENUATION

The DAC digital filter type is selected by the DACSLOPE register bit as shown in Table 42.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 (06h) DAC Control (2)	1	DACSLOPE	0	Selects DAC filter characteristics 0 = Normal mode 1 = Sloping stopband mode

Table 42 DAC Filter Selection

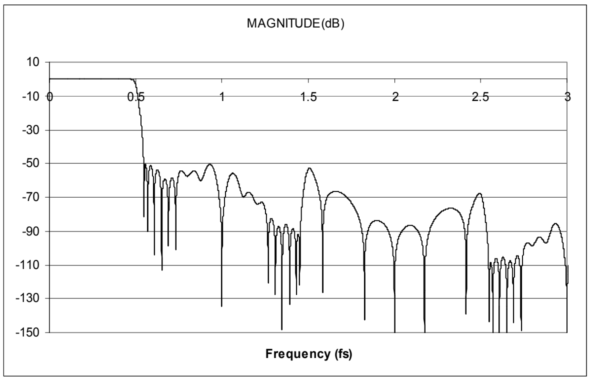


Figure 36 DAC Digital Filter Frequency Response (Normal Mode)

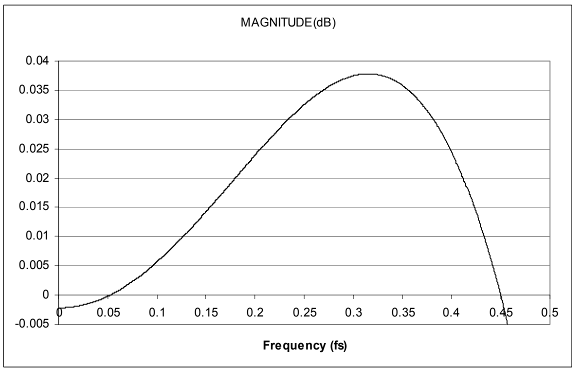


Figure 37 DAC Digital Filter Ripple (Normal Mode)

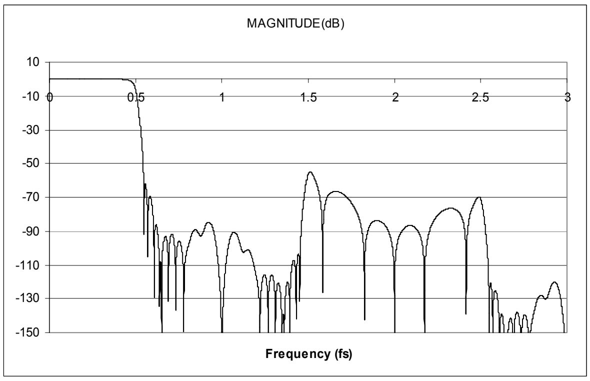


Figure 38 DAC Digital Filter Frequency Response (Sloping Stopband Mode)

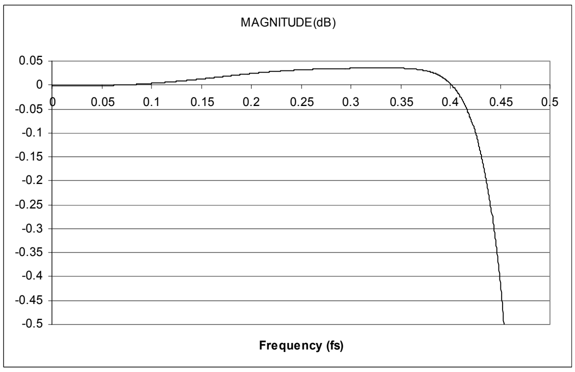


Figure 39 DAC Digital Filter Ripple (Sloping Stopband Mode)

DE-EMPHASIS FILTER RESPONSES

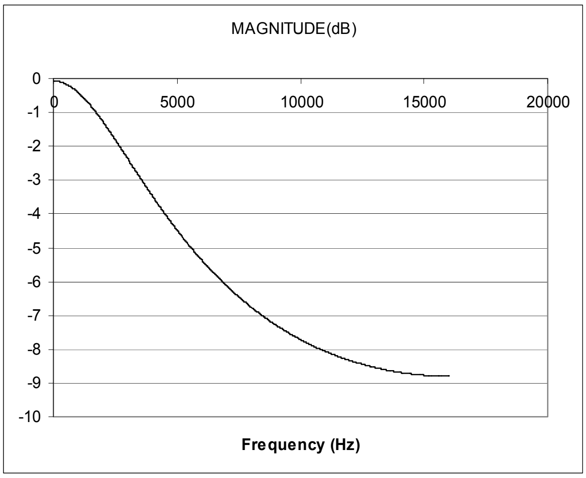


Figure 40 De-Emhpasis Digital Filter Response (32kHz)

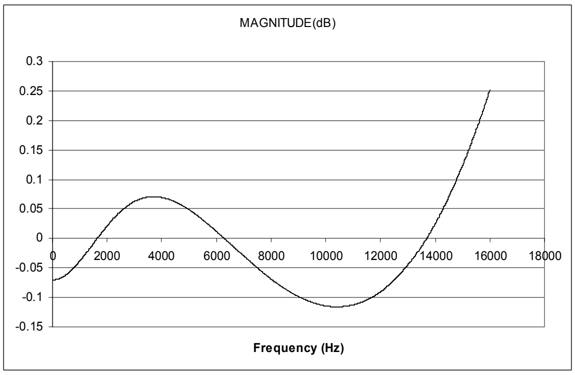


Figure 41 De-Emphasis Error (32kHz)

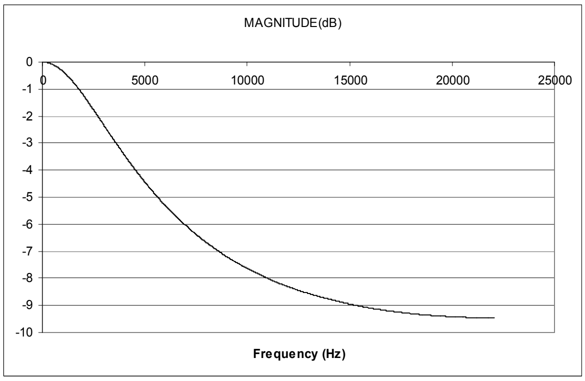


Figure 42 De-Emhpasis Digital Filter Response (44.1kHz)

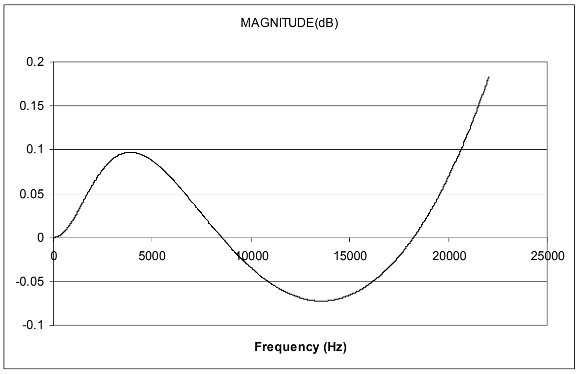


Figure 43 De-Emphasis Error (44.1kHz)

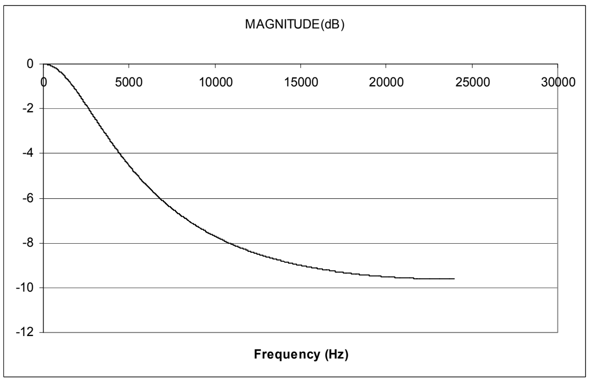


Figure 44 De-Emhpasis Digital Filter Response (48kHz)

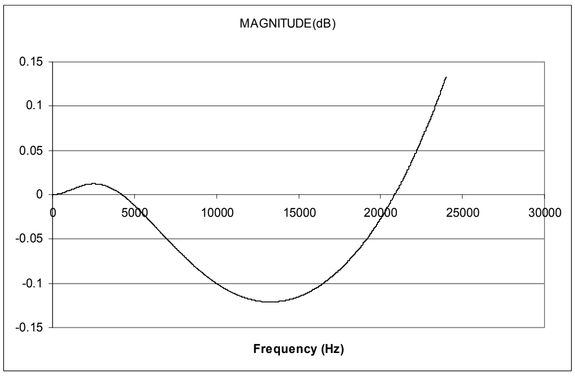
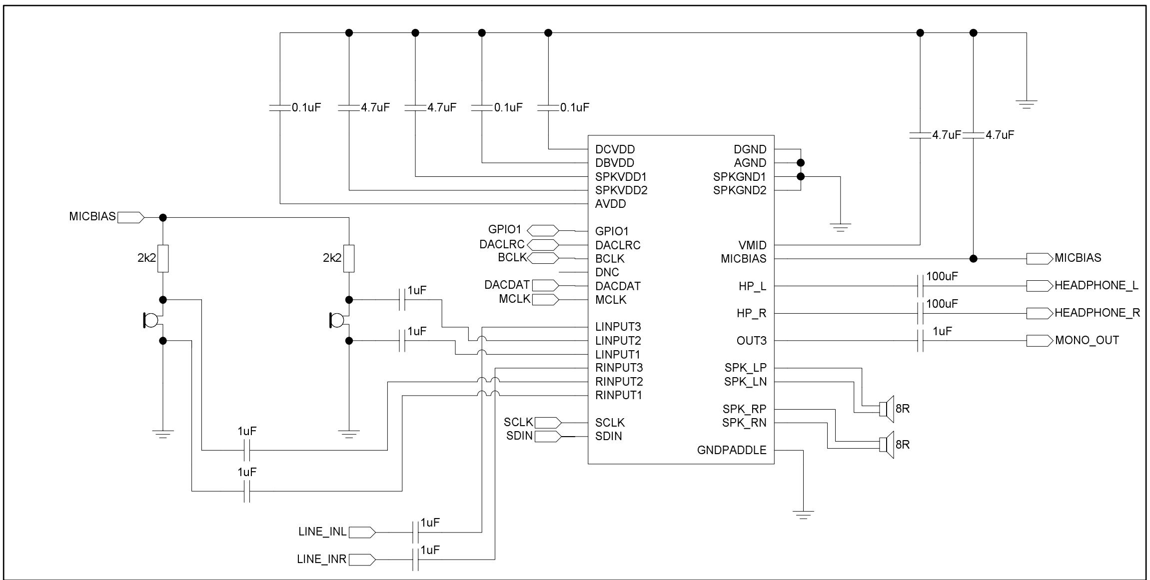


Figure 45 De-Emphasis Error (48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS



Notes:
1. AGND and DGND should be connected as close to the WM8956 as possible.
2. Supply decoupling capacitors on DCVDD, DBVDD, SPKVDD and AVDD should be positioned as close to the WM8956 as possible.
3. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for optimum performance.
4. Microphone common mode noise performance can be improved by adding resistors from the microphone negative terminal to ground.
5. The speakers should be connected as close as possible to the WM8956. When this is not possible, filtering should be placed on the speaker outputs close the the WM8956.

SPEAKER SELECTION

For filterless operation, it is important to select a speaker with appropriate internal inductance. The internal inductance and the speaker's load resistance create a low-pass filter with a cut-off frequency of:

$$f_c = R_L / 2\pi L$$

e.g. for an 8Ω speaker and required cut-off frequency of 20kHz, the speaker should be chosen to have an inductance of:

$$L = R_L / 2\pi f_c = 8\Omega / 2\pi * 20\text{kHz} = 64\mu\text{H}$$

8Ω speakers typically have an inductance in the range 20µH to 100µH. Care should be taken to ensure that the cut-off frequency of the speaker's internal filtering is low enough to prevent speaker damage. The class D outputs of the WM8956 operate at much higher frequencies than is recommended for most speakers, and the cut-off frequency of the filter should be low enough to protect the speaker.

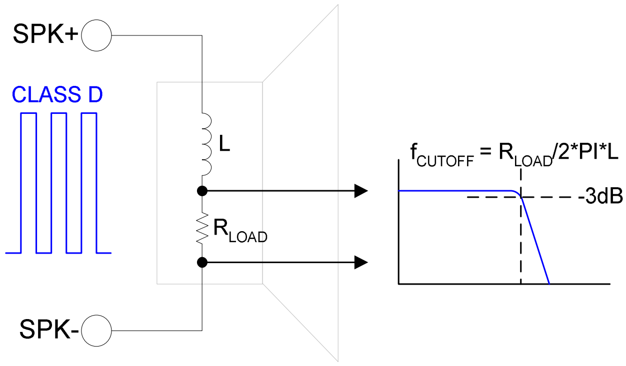


Figure 46 Speaker Equivalent Circuit

PCB LAYOUT CONSIDERATIONS

The efficiency of the speaker drivers is affected by the series resistance between the WM8956 and the speaker (e.g. inductor ESR) as shown in Figure 47. This resistance should be as low as possible to maximise efficiency.

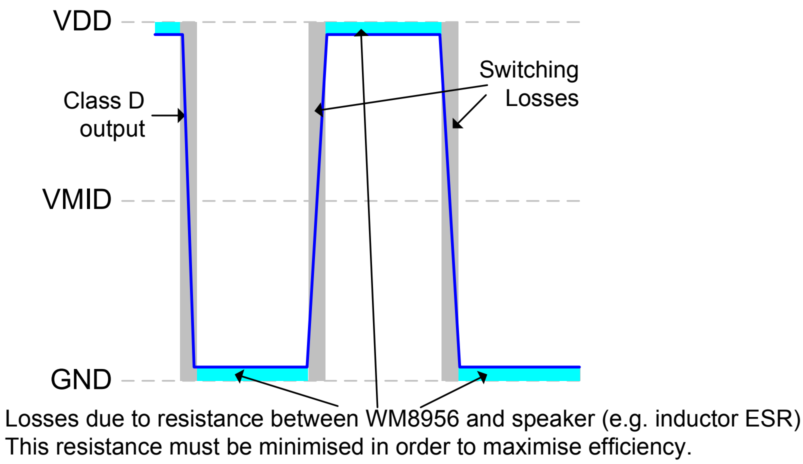


Figure 47 Speaker Connection Losses

The distance between the WM8956 and the speakers should be kept to a minimum to reduce series resistance, and also to reduce EMI. Further reductions in EMI can be achieved by additional passive filtering and/or shielding as shown in Figure 48. When additional passive filtering is used, low ESR components should be chosen to minimise series resistance between the WM8956 and the speaker, maximising efficiency.

LC passive filtering will usually be effective at reducing EMI at frequencies up to around 30MHz. To reduce emissions at higher frequencies, ferrite beads placed as close to the device as possible will be more effective.

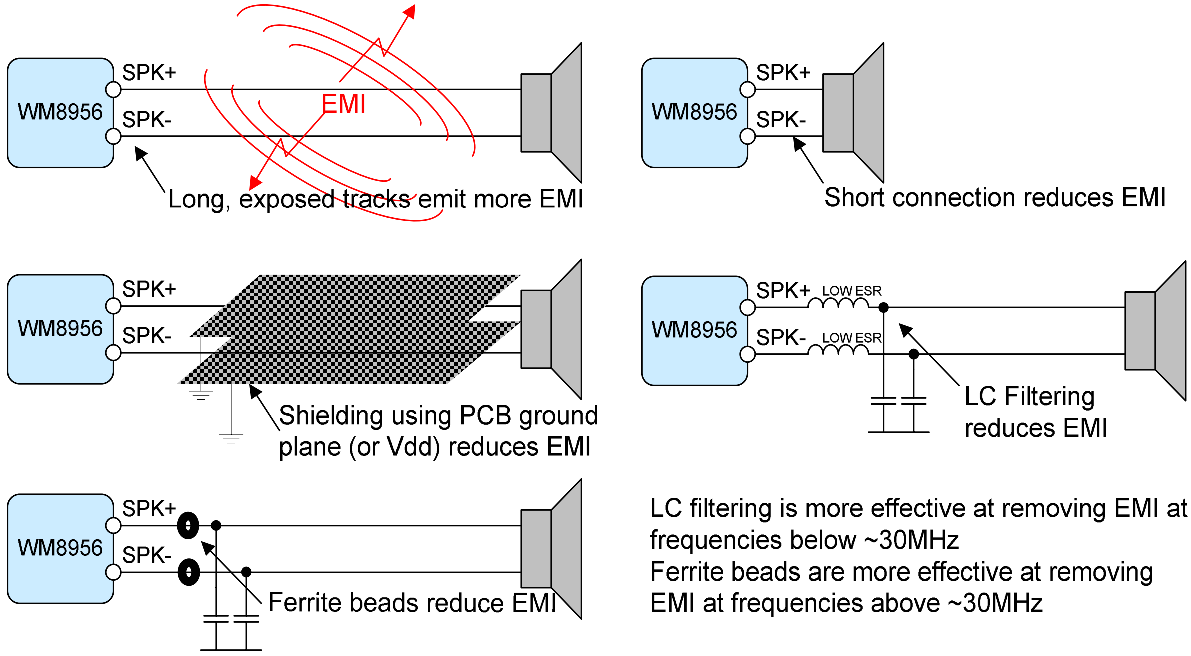
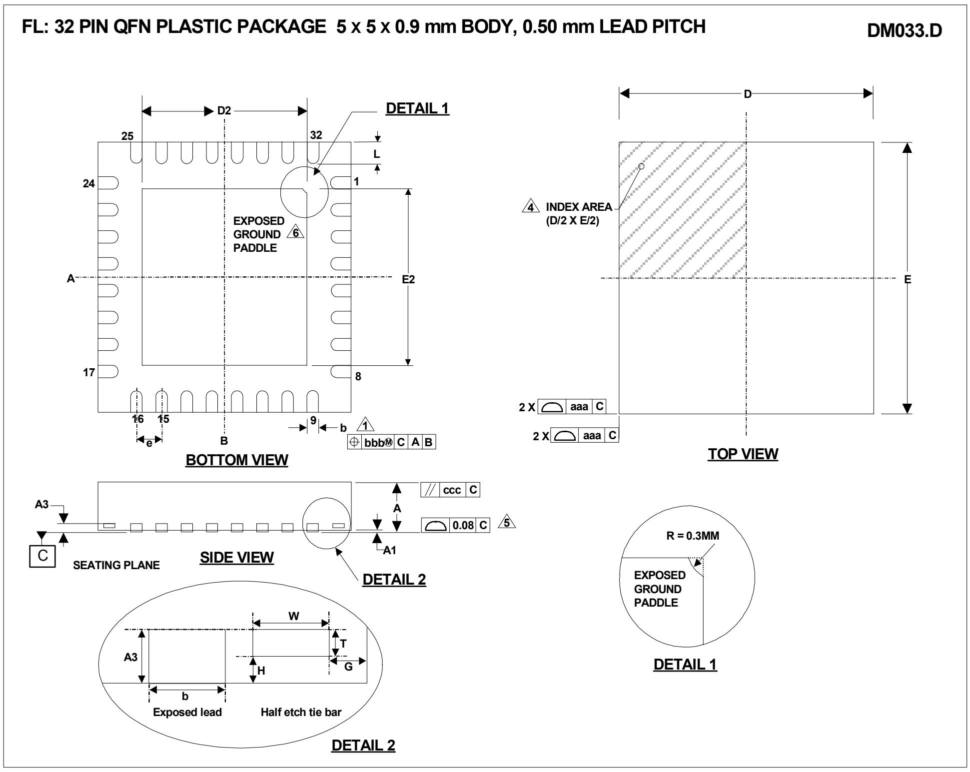


Figure 48 EMI Reduction Techniques

PACKAGE DRAWING



Symbols		Dimensions (mm)		
	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0	0.02	0.05	
A3		0.20 REF		
b	0.18	0.25	0.30	1
D		5.00		
D2	3.30	3.45	3.55	2
E		5.00		
E2	3.30	3.45	3.55	2
e		0.50 BSC		
G		0.213		
H		0.1		
L	0.30	0.40	0.50	
T		0.1		
W		0.2		
Tolerances of Form and Position				
aaa	0.15			
bbb	0.10			
ccc	0.10			
REF:	JEDEC, MO-220, VARIATION VHHD-5.			

NOTES:
1. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.
2. FALLS WITHIN JEDEC, MO-220, VARIATION VHHD-5.
3. ALL DIMENSIONS ARE IN MILLIMETRES.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-002.
5. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
6. REFER TO APPLICATION NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.
7. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.

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