

256K x 16 Static RAM

Features

- High Speed
 - 55 ns and 70 ns availability
- Low voltage range:
 - 1.65V–1.95V
- Pin Compatible with CY62146BV18
- Ultra-low active power
 - Typical Active Current: 0.5 mA @ f = 1 MHz
 - Typical Active Current: 2 mA @ f = f_{max} (70 ns speed)
- Low standby power
- Easy memory expansion with \overline{CE} and \overline{OE} features
- Automatic power-down when deselected
- CMOS for optimum speed/power

Functional Description

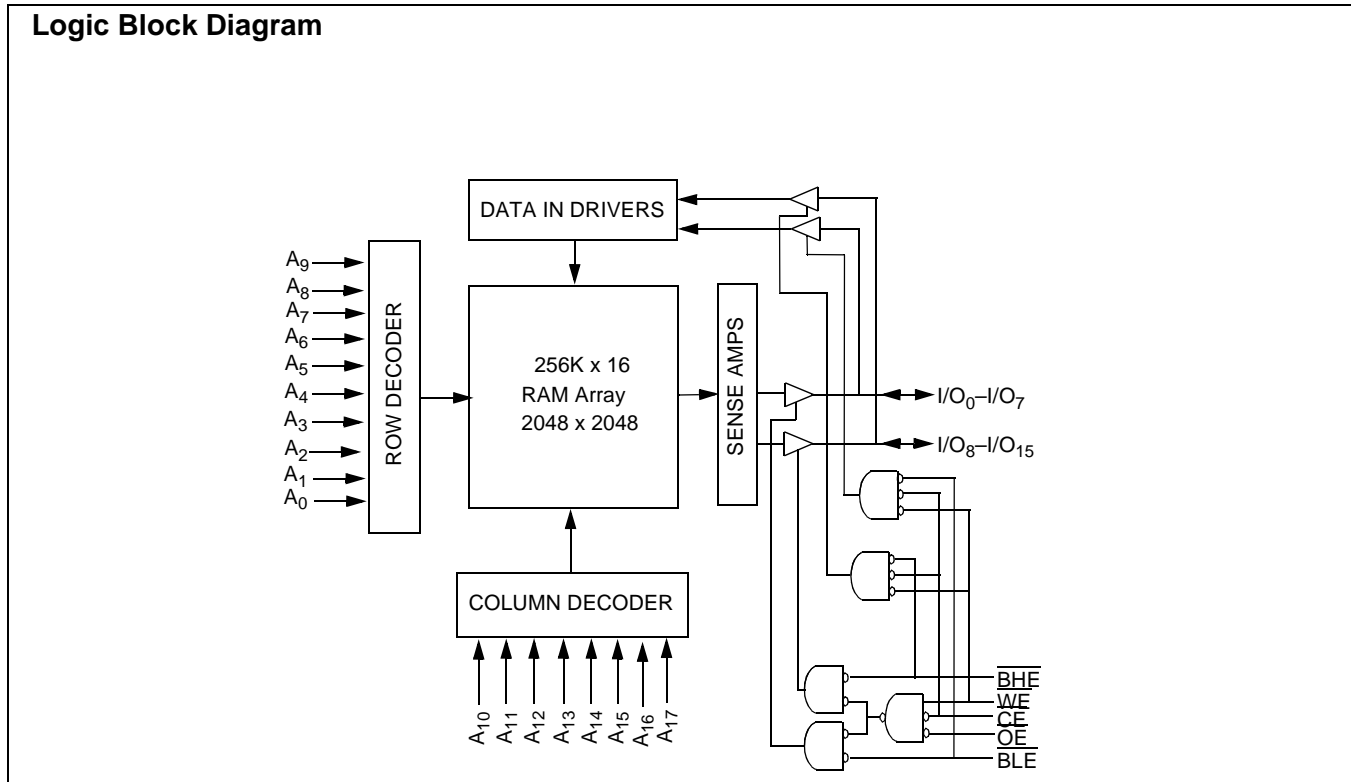
The CY62146CV18 is a high-performance CMOS static RAM organized as 256K words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly

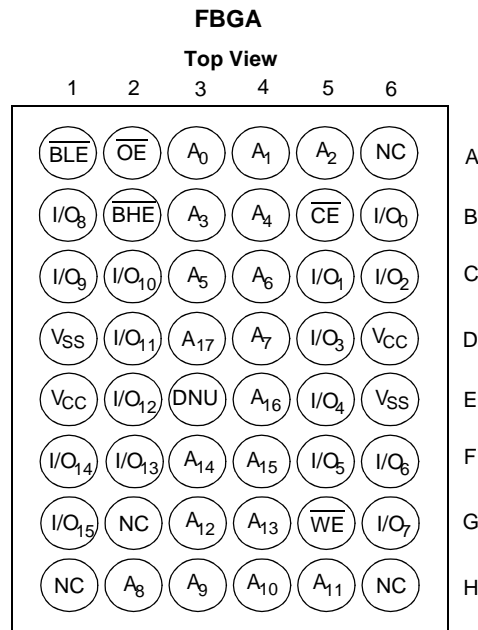
reduces power consumption by 99% when addresses are not toggling. The device can also be put into standby mode when deselected (\overline{CE} HIGH). The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when deselected (\overline{CE} HIGH), outputs are disabled (\overline{OE} HIGH), \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{16}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62146CV18 is available in a 48-Ball FBGA package.



Pin Configurations^[1, 2]

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +2.4V

DC Voltage Applied to Outputs in High-Z State^[2] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[2] -0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC}
CY62146CV18	Industrial	-40°C to +85°C	1.65V to 1.95V

Product Portfolio

Product	V _{CC} Range			Speed	Power Dissipation (Industrial)					
					Operating (I _{CC})				Standby (I _{SB2})	
	V _{CC} (min.)	V _{CC} (typ.) ^[4]	V _{CC} (max.)		f = 1 MHz		f = f _{max}			
					Typ. ^[4]	Max.	Typ. ^[4]	Max.	Typ. ^[4]	Max.
CY62146CV18	1.65V	1.80V	1.95V	55ns	0.5 mA	3 mA	2.5 mA	7 mA	1 μA	10 μA
				70ns	0.5 mA	3 mA	2 mA	6 mA		

Notes:

- NC pins are not connected to the die.
- E3 (DNU) can be left as NC or V_{SS} to ensure proper application.
- V_{IL(min.)} = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62146CV18 MoBL2™-55			CY62146CV18 MoBL2™-70			Unit
			Min.	Typ. ^[4]	Max	Min.	Typ. ^[4]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA V _{CC} = 1.65V	1.4			1.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA V _{CC} = 1.65V			0.2			0.2	V
V _{IH}	Input HIGH Voltage		1.4		V _{CC} + 0.2V	1.4		V _{CC} + 0.2V	V
V _{IL}	Input LOW Voltage		-0.2		0.4	-0.2		0.4	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1		+1	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-1		+1	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC} V _{CC} = 1.95V I _{OUT} = 0 mA CMOS levels		2.5	7		2	6	mA
		f = 1 MHz		0.5	3		0.5	3	mA
I _{SB1}	Automatic CE Power-down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$ f = f _{MAX} (Address and Data Only), f = 0 (OE, WE, BHE, and BLE)		1	10		1	10	μA
I _{SB2}	Automatic CE Power-down Current— CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, f = 0, V _{CC} = 1.95V							

Capacitance^[5]

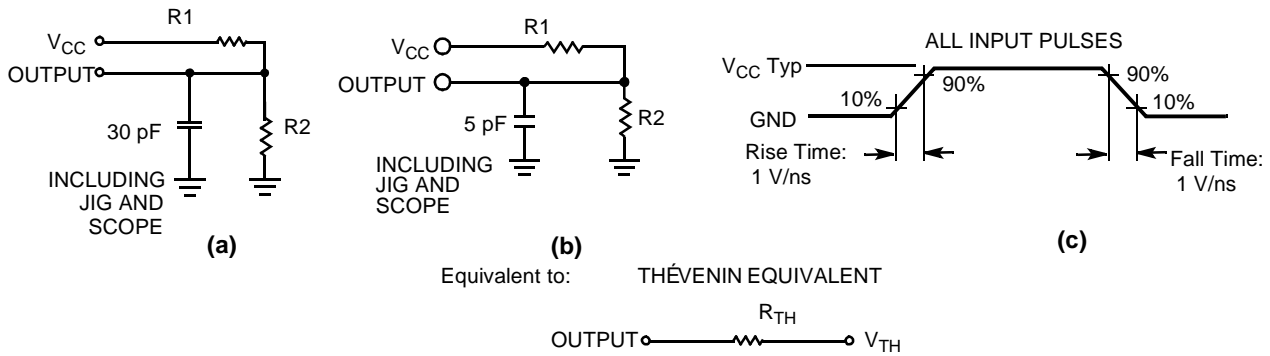
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC} (typ.)	8	pF
C _{OUT}	Output Capacitance		10	pF

Thermal Resistance

Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient) ^[5]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	θ _{JA}	55	°C/W
Thermal Resistance (Junction to Case) ^[5]		θ _{JC}	16	°C/W

Note:

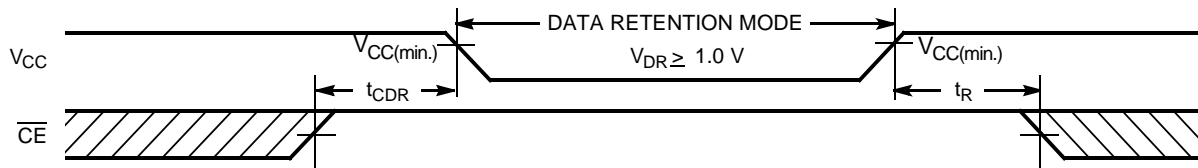
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


Parameters	1.8V	UNIT
R1	13500	Ohms
R2	10800	Ohms
R_{TH}	6000	Ohms
V_{TH}	0.80	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[4]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0		1.95	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.0V$ $CE \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		1	8	μA
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[6]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform

Note:

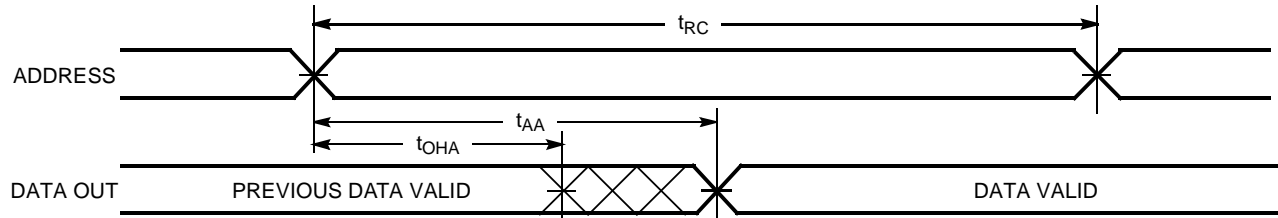
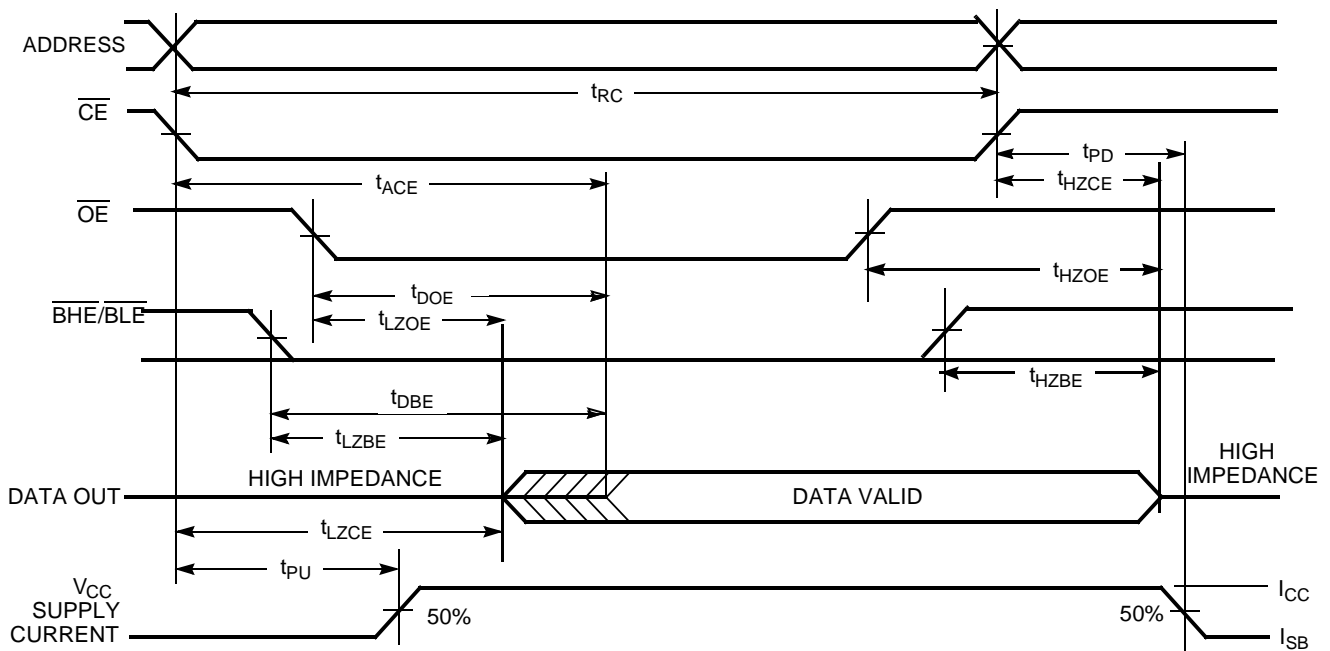
6. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ $\geq 100 \mu s$ or stable at $V_{CC(min)}$ $\geq 100 \mu s$.

Switching Characteristics Over the Operating Range ^[7]

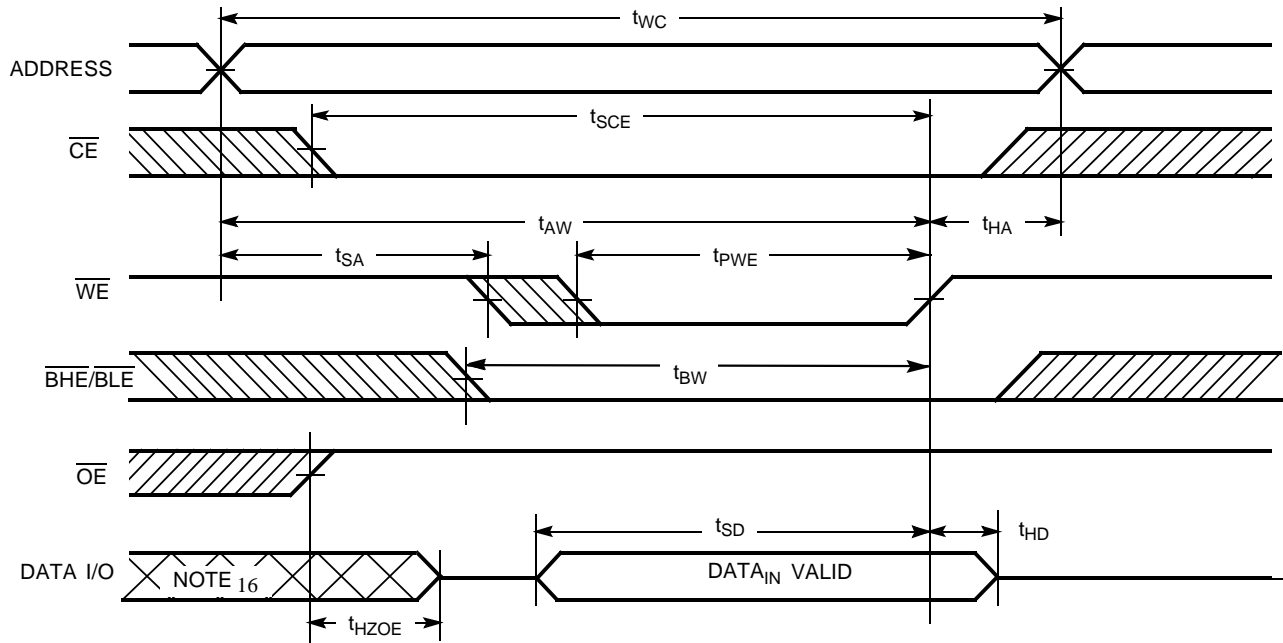
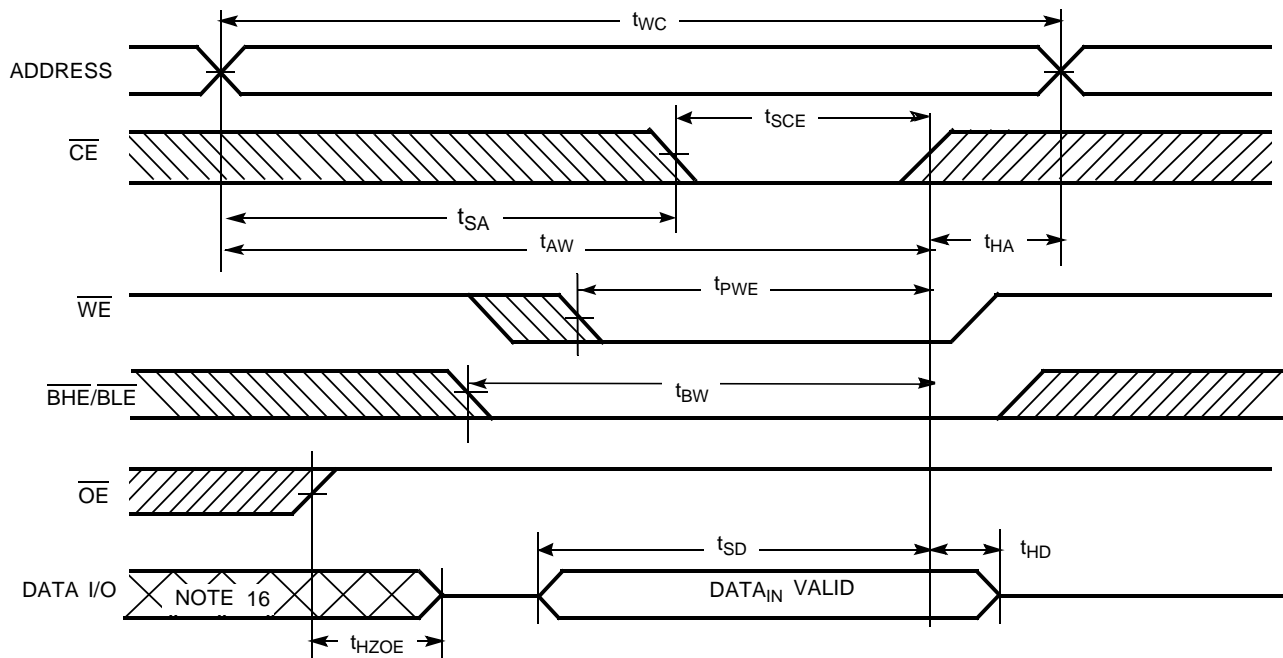
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	\overline{CE} LOW to Data Valid		55		70	ns
t _{DOE}	\overline{OE} LOW to Data Valid		25		35	ns
t _{LZOE}	\overline{OE} LOW to Low-Z ^[8]	5		5		ns
t _{HZOE}	\overline{OE} HIGH to High-Z ^[8, 9]		20		25	ns
t _{LZCE}	\overline{CE} LOW to Low-Z ^[8]	5		10		ns
t _{HZCE}	\overline{CE} HIGH to High-Z ^[8, 9]		20		25	ns
t _{PU}	\overline{CE} LOW to Power-up	0		0		ns
t _{PD}	\overline{CE} HIGH to Power-down		55		70	ns
t _{DBE}	\overline{BHE} / \overline{BLE} LOW to Data Valid		30		45	ns
t _{LZBE}	\overline{BHE} / \overline{BLE} LOW to Low-Z ^[8]	5		5		ns
t _{HZBE}	\overline{BHE} / \overline{BLE} HIGH to High-Z ^[8, 9]		20		25	ns
Write Cycle^[10]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	\overline{CE} LOW to Write End	40		60		ns
t _{AW}	Address Set-up to Write End	40		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		ns
t _{PWE}	\overline{WE} Pulse Width	40		50		ns
t _{BW}	\overline{BHE} / \overline{BLE} Pulse Width	40		60		ns
t _{SD}	Data Set-up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	\overline{WE} LOW to High-Z ^[8, 9]		15		25	ns
t _{LZWE}	\overline{WE} HIGH to Low-Z ^[9]	5		10		ns

Notes:

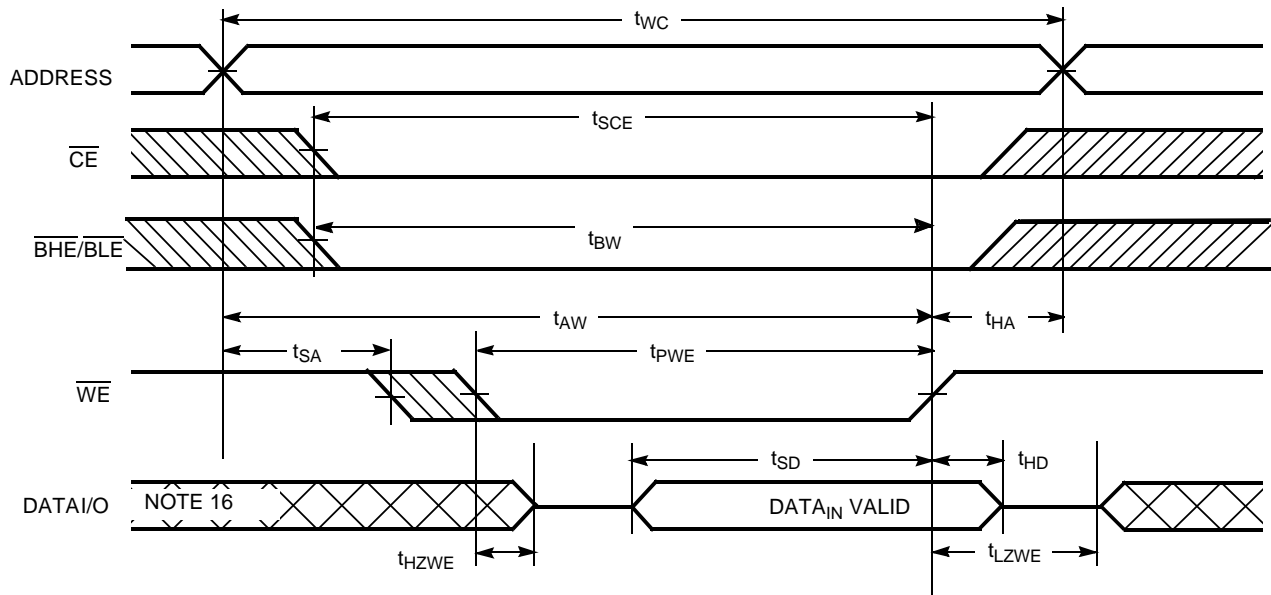
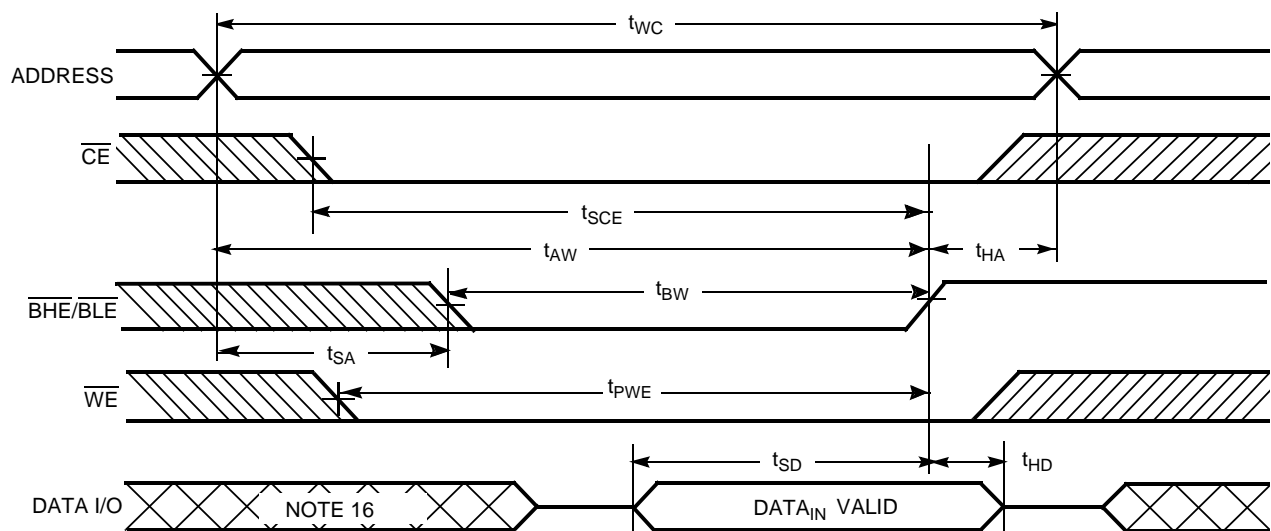
- Test conditions assume signal transition time of 3ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
- The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE} = V_{IL}$, \overline{BHE} and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write

Switching Waveforms
Read Cycle No. 1 (Address Transition Controlled)^[11, 12]

Read Cycle No. 2 ($\overline{\text{OE}}$ Controlled)^[12, 13]

Notes:

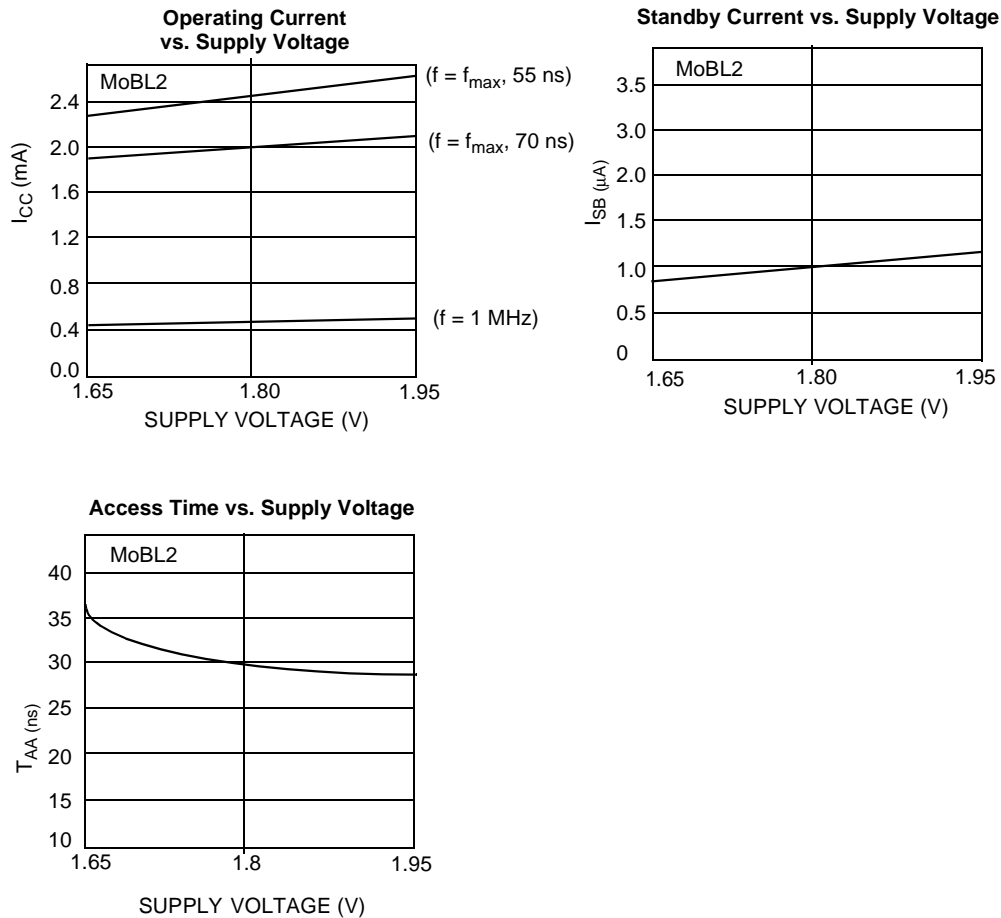
11. Device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}} = V_{\text{IL}}$, $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IL}}$.
12. $\overline{\text{WE}}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{\text{CE}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{WE} Controlled) ^[10, 14, 15]

Write Cycle No. 2 (\overline{CE} Controlled) ^[10, 14, 15]

Notes:

14. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
15. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
16. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[15]

Write Cycle No. 4 ($\overline{\text{BHE/BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[15]


Typical DC and AC Characteristics (Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC\ Typ}$, $T_A = 25^\circ\text{C}$.)

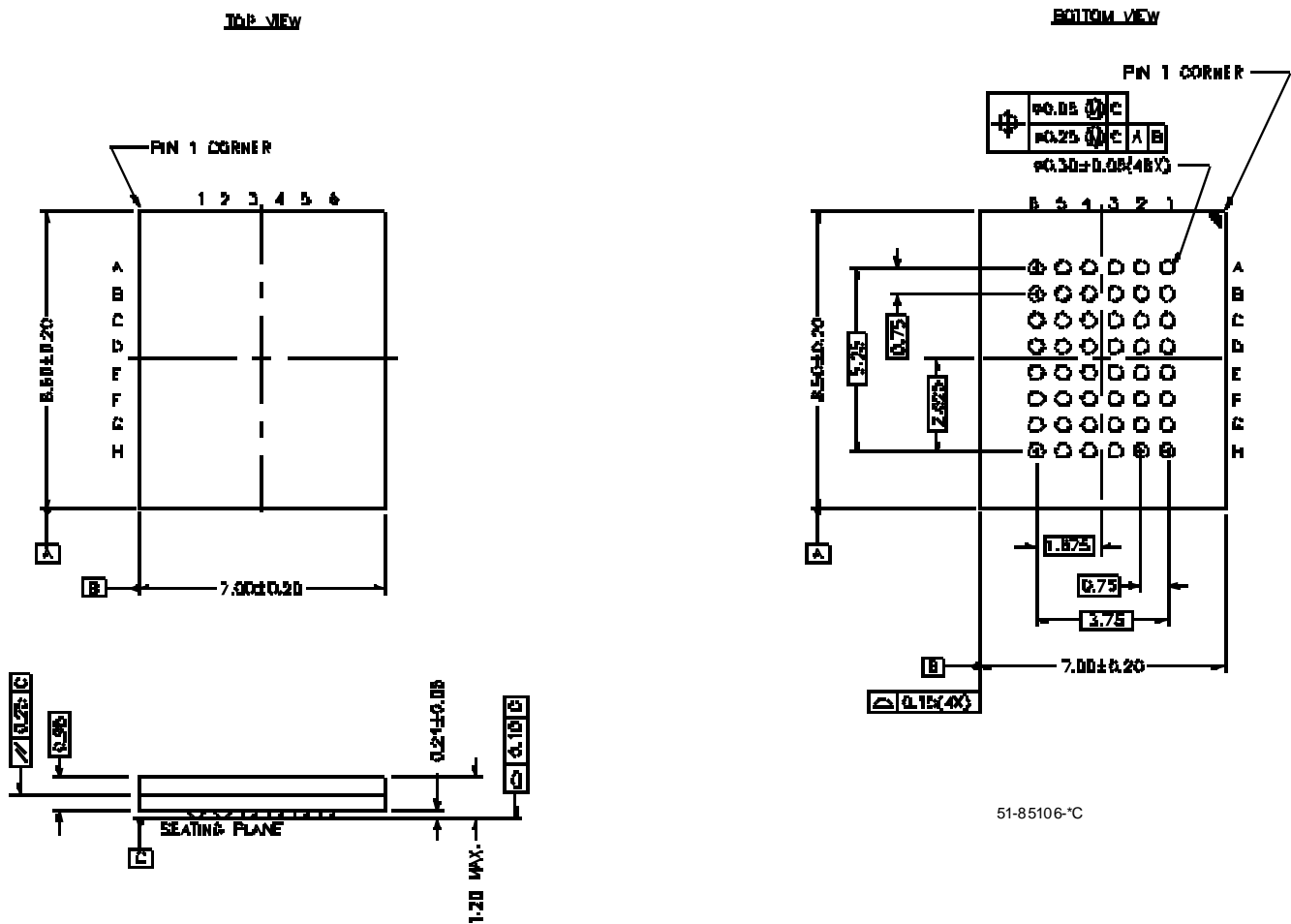


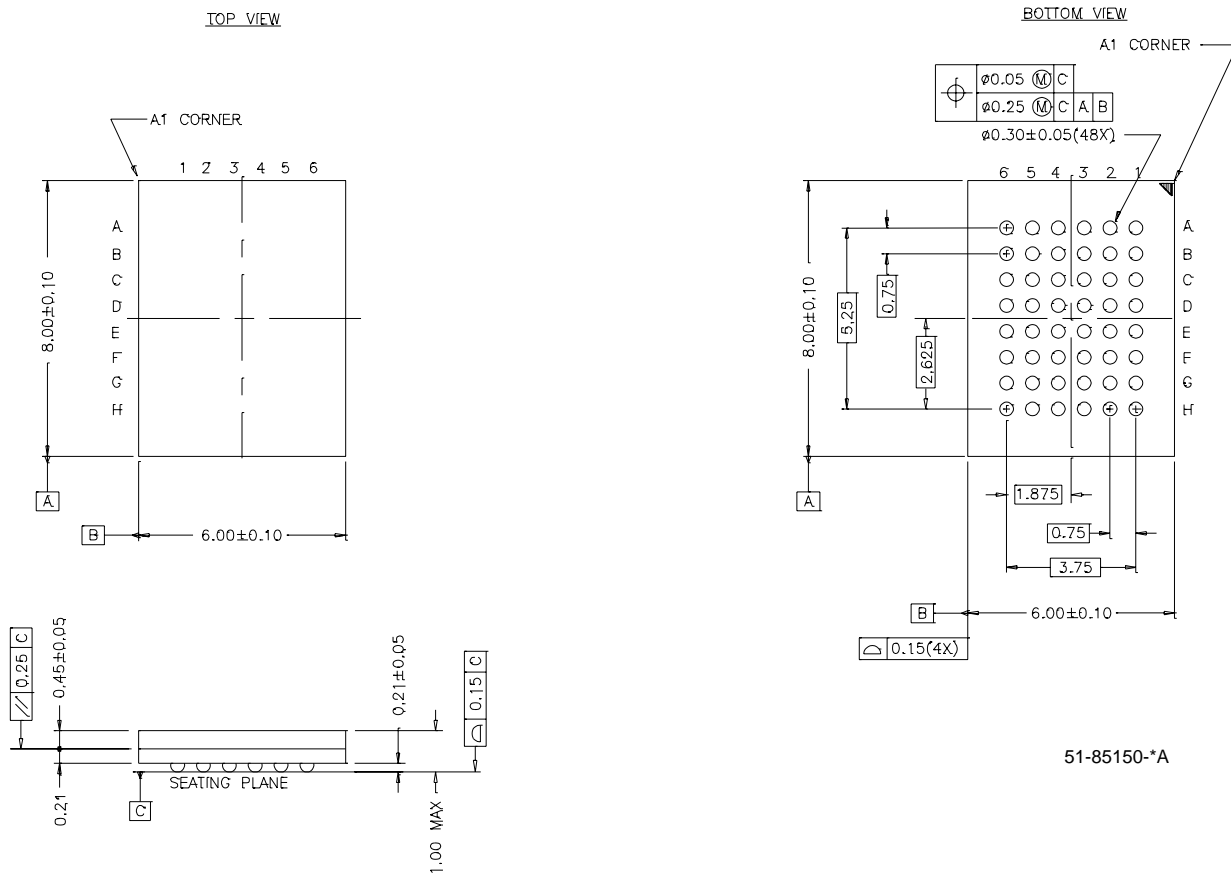
Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O ₀ –I/O ₁₅)	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High-Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High-Z	Read	Active (I_{CC})
L	H	L	H	H	High-Z	Output Disabled	Active (I_{CC})
L	H	H	X	X	High-Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O ₀ –I/O ₁₅)	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High-Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High-Z	Write	Active (I_{CC})
L	L	X	H	H	High-Z	Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62146CV18LL-70BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	Industrial
	CY62146CV18LL-70BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	
55	CY62146CV18LL-55BAI	BA48B	48-Ball Fine Pitch BGA (7 mm x 8.5 mm x 1.2 mm)	
	CY62146CV18LL-55BVI	BV48A	48-Ball Fine Pitch BGA (6 mm x 8 mm x 1 mm)	

Package Diagrams
48-Ball (7.00 mm x 8.5 mm x 1.2 mm) Thin BGA BA48B


Package Diagrams (continued)
48-Lead VFBGA (6 x 8 x 1 mm) BV48A


51-85150-*A

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Document Title: CY62146CV18 MoBL2™ MoBL2 256K x 16 SRAM
Document Number: 38-05010

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106039	05/08/01	HRT/MGN	Created Preliminary Data Sheet
*A	107702	06/15/01	MGN	Delete Datasheet. Not offering this device.
*B	111468	11/02/01	MGN	Reactivating datasheet. Die Rev. from R5 to R7.
*C	115863	09/03/02	DPM	From Preliminary to Final. Added BV package