300mA, Low Noise, Ultra-Fast CMOS Triple LDOs Regulator

General Description

The RT9004 is designed for portable RF and wireless applications with demanding performance and space requirements. The RT9004 performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The RT9004 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The RT9004 consumes less than 0.01uA in shutdown mode and has fast turn-on time less than 50us. RT9004 is short circuit thermal folded back protected. RT9004 lowers its OTP trip point from 165°C to 110°C when output short circuit occurs (V_{OUT} < 0.4V) providing maximum safety to end users. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. Available in the VDFN-10L 3x3 and WDFN-10L 3x3 packages, the RT9004 also offers custom voltage, range of 1.5V to 3.5V with 0.1V per step.

Ordering Information

RT9004□□□

- Package Type
  - QV : VDFN-10L 3x3 (V-Type)
  - QW : WDFN-10L 3x3 (W-Type)
- Operating Temperature Range
  - P : Pb Free with Commercial Standard
  - G : Green (Halogen Free with Commercial Standard)
- Voltage Version : VOUT1/VOUT2/VOUT3
  - A : 2.8V/2.5V/1.8V
  - B : 3.0V/2.5V/1.8V
  - C : 2.8V/2.8V/1.8V
  - D : 2.8V/1.8V/1.8V
  - E : 3.3V/2.8V/1.8V
  - F : 3.3V/2.8V/2.8V
  - G : 2.5V/2.8V/2.5V
  - H : 2.8V/2.8V/1.5V
  - J : 1.5V/3.3V/3.3V
  - K : 3.0V/3.0V/1.8V

Note :

Richtek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Features

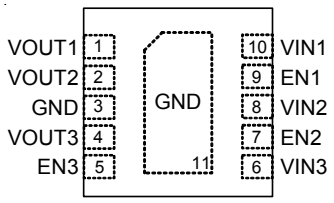
- **Short Circuit Thermal Folded Back Protection**
- **Low-Noise for RF Application**
- **Fast Response in Line/Load Transient**
- **Quick Start-Up (Typically 50us)**
- **Low Dropout : 220mV @ 300mA**
- **Wide Operating Voltage Ranges : 2.5V to 5.5V**
- **TTL-Logic-Controlled Shutdown Input**
- **Low Temperature Coefficient**
- **Thermal Shutdown Protection**
- **Only 1uF Output Capacitor Required for Stability**
- **High Power Supply Rejection Ratio**
- **Custom Voltage Available**
- **Small 10-Lead VDFN and WDFN Packages**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- CDMA/GSM Cellular Handsets
- Battery-Powered Equipment
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- PCMCIA Cards
- Portable Information Appliances

Pin Configurations

(TOP VIEW)

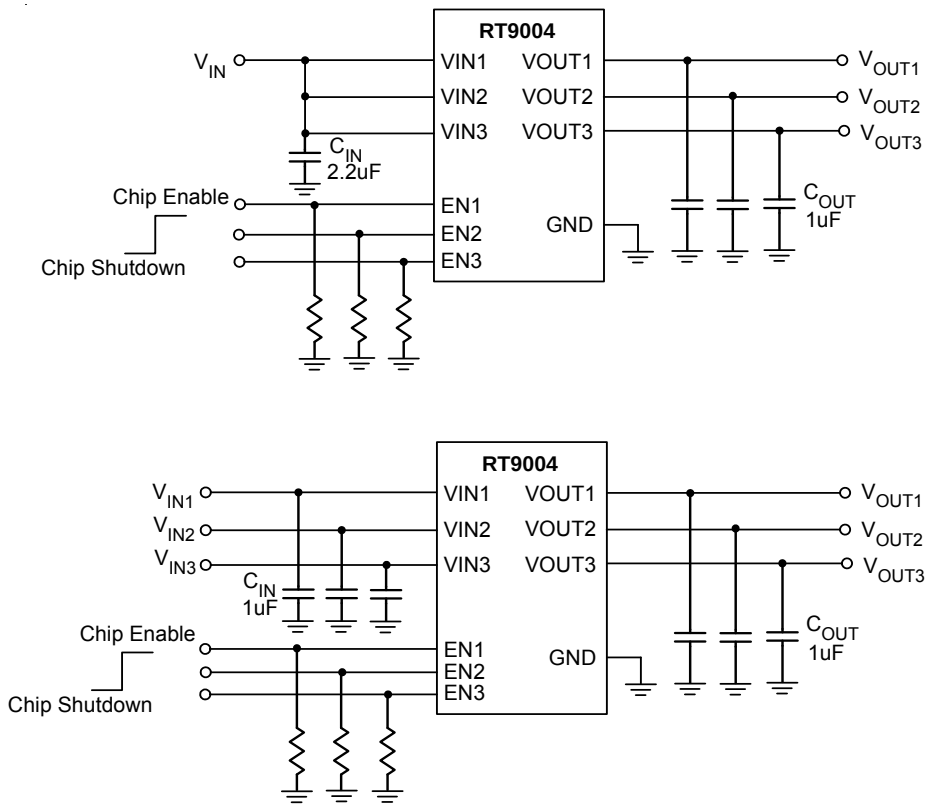


V/WDFN-10L 3x3

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area, otherwise visit our website for detail.

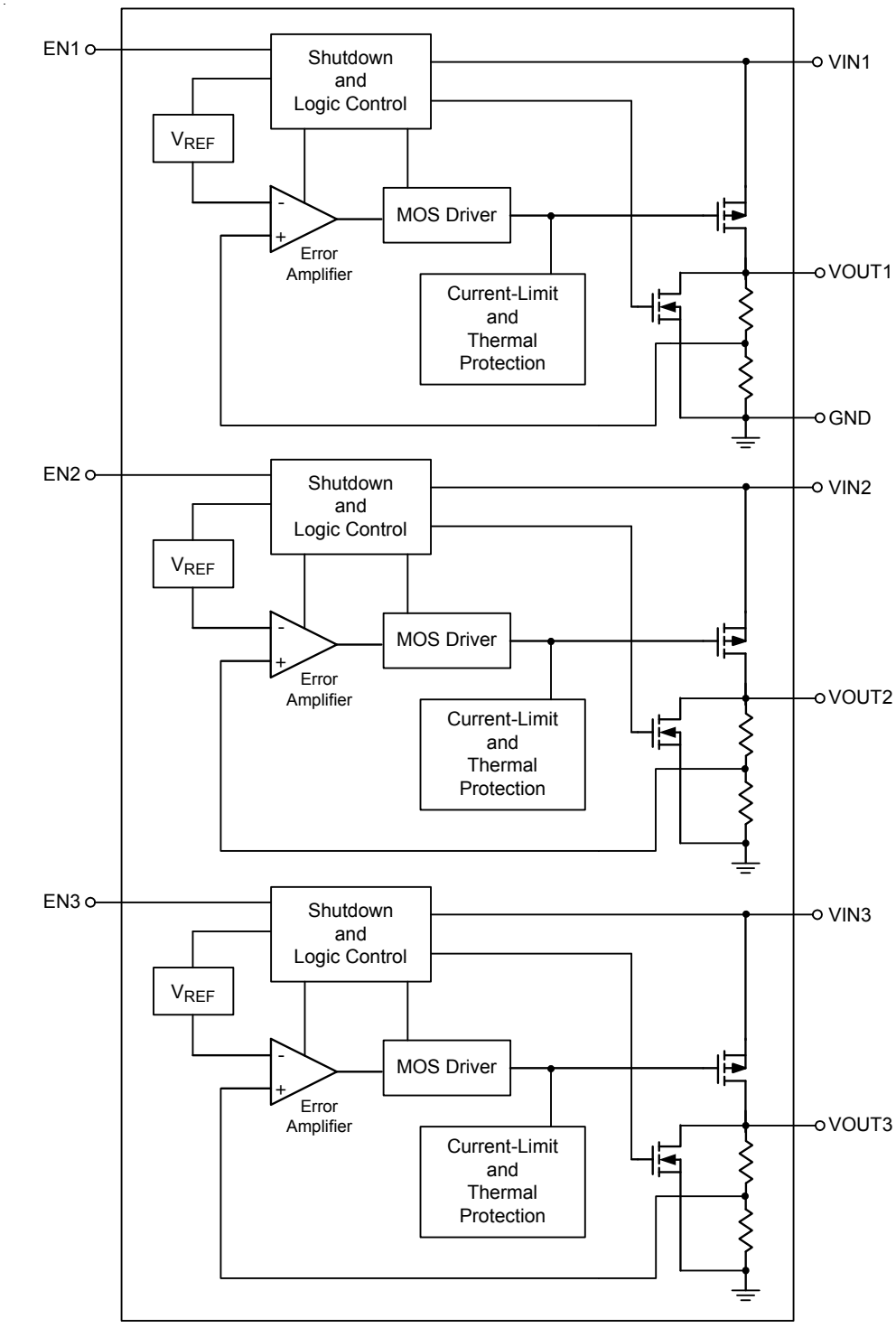
Typical Application Circuit



Functional Pin Description

Pin Number	Pin Name	Pin Function
1	VOUT1	Output Voltage 1.
2	VOUT2	Output Voltage 2.
3 Exposed Pad (11)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
4	VOUT3	Output Voltage 3.
5	EN3	Chip Enable 3 (Active High). Note that this pin is high impedance. There should be a pull low 100kΩ resistor connected to GND when the control signal is floating.
6	VIN3	Input Voltage 3.
7	EN2	Chip Enable 2 (Active High). Note that this pin is high impedance. There should be a pull low 100kΩ resistor connected to GND when the control signal is floating.
8	VIN2	Input Voltage 2.
9	EN1	Chip Enable 1 (Active High). Note that this pin is high impedance. There should be a pull low 100kΩ resistor connected to GND when the control signal is floating.
10	VIN1	Input Voltage 1.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- 6.0V
- Power Dissipation, P_D @ T_A = 25°C
  V/WDFN-10L 3x3 ---------- 0.952 W
- Package Thermal Resistance (Note 4)
  V/WDFN-10L 3x3, θ_{JA} ---------- 105°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 125°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Input Voltage ---------- 2.5V to 5.5V
- Operation Ambient Temperature Range ---------- –40°C to 85°C
- Operation Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = V_{OUT} + 1V, C_{IN} = C_{OUT} = 1µF, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage Accuracy		ΔV_{OUT}	I_{OUT} = 1mA	–2	--	+2	%
Current Limit		I_{LIM}	R_{LOAD} = 1Ω	360	400	--	mA
Quiescent Current		I_Q	V_{EN} >= 1.2V, I_{OUT} = 0mA	--	90	--	µA
Dropout Voltage (Note 4)		V_{DROP}	I_{OUT} = 200mA	--	170	--	mV
			I_{OUT} = 300mA	--	220	--	
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT} + 1V) to 5.5V, I_{OUT} = 1mA	--	--	0.3	%
Load Regulation		ΔV_{LOAD}	1mA < I_{OUT} < 300mA	--	--	0.6	%
Standby Current		I_{STBY}	V_{EN} = GND, Shutdown	--	0.01	1	µA
EN Input Bias Current		I_{IBSD}	V_{EN} = GND or VIN	--	0	100	nA
EN Threshold	Logic-Low Voltage	V_{IL}	V_{IN} = 3V to 5.5V, Shutdown	--	--	0.4	V
	Logic-High Voltage	V_{IH}	V_{IN} = 3V to 5.5V, Start-Up	1.2	--	--	
Power Supply Rejection Rate	f = 100Hz	PSRR	C_{OUT} = 1µF, I_{OUT} = 100mA	--	–60	--	dB
	f = 10kHz			--	–30	--	
Thermal Shutdown Temperature		T_{SD}		--	165	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	30	--	°C
Thermal Folded Back Temperature		ΔT_{TFB}		--	110	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

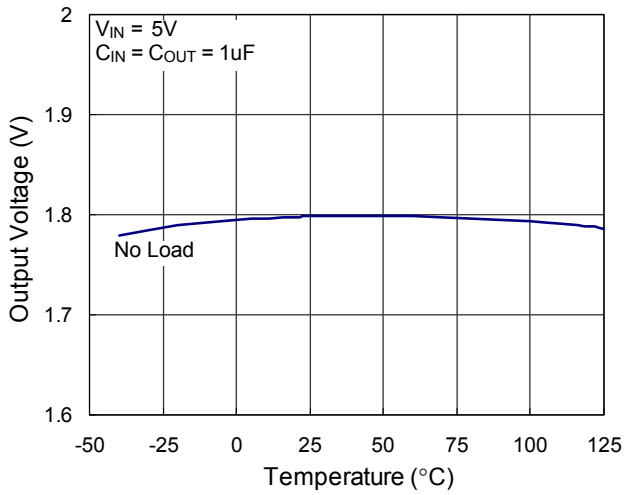
Note 2. Devices are ESD sensitive. Handling precaution is recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

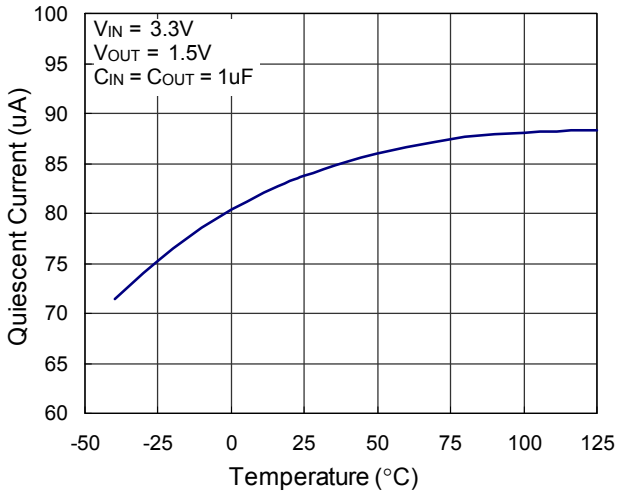
Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board (single-later, 1s) of JEDEC 51-3 thermal measurement standard.

Typical Operating Characteristics

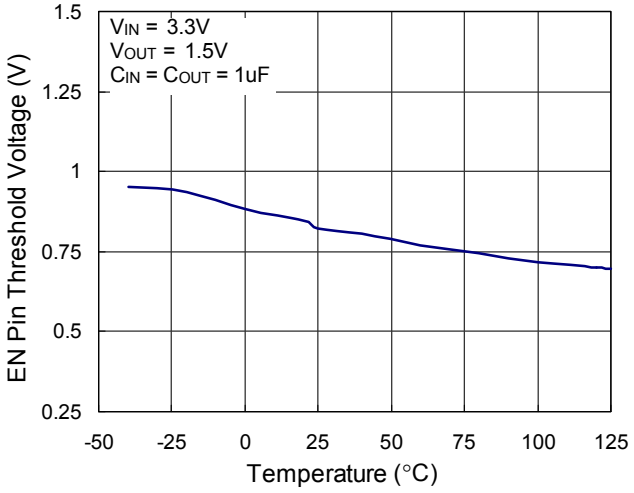
Output Voltage vs. Temperature



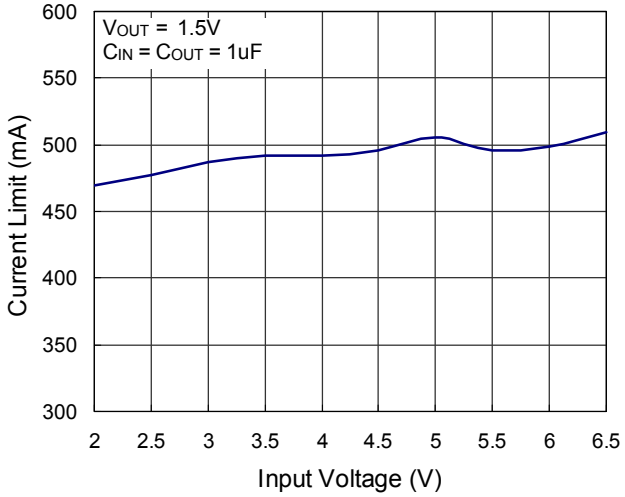
Quiesent Current vs. Temperature



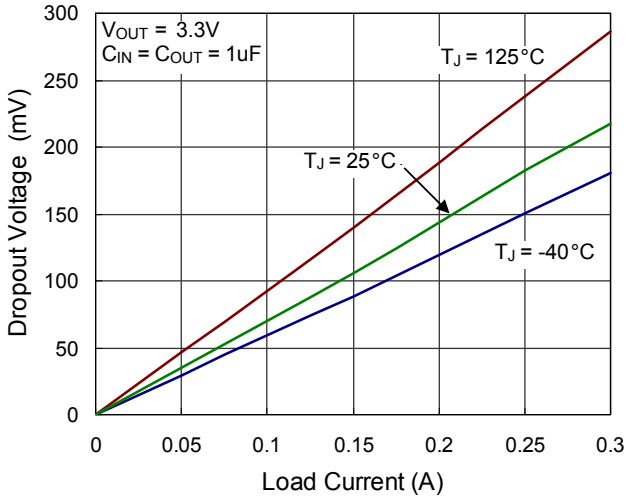
EN Pin Shutdown Threshold vs. Temperature



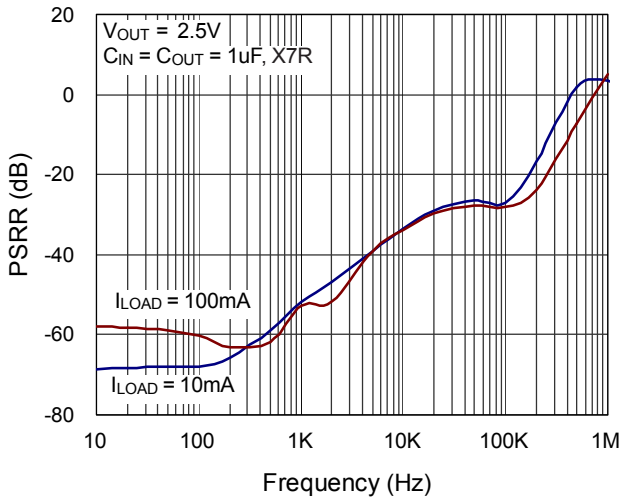
Current Limit vs. Input Voltage



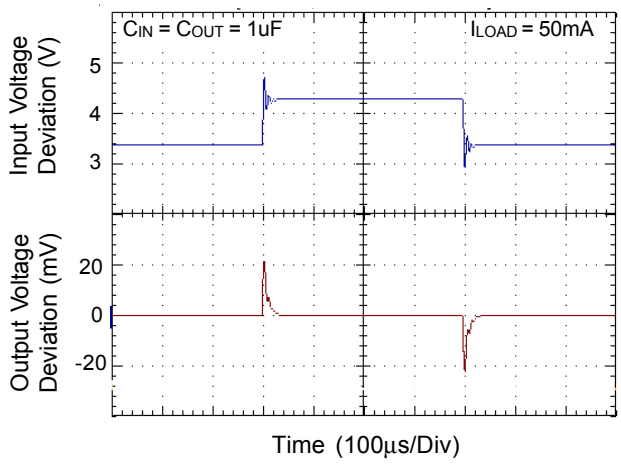
Dropout Voltage vs. Load Current



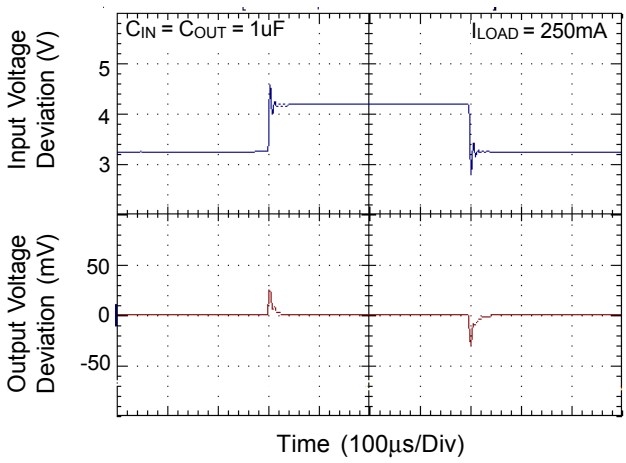
PSRR



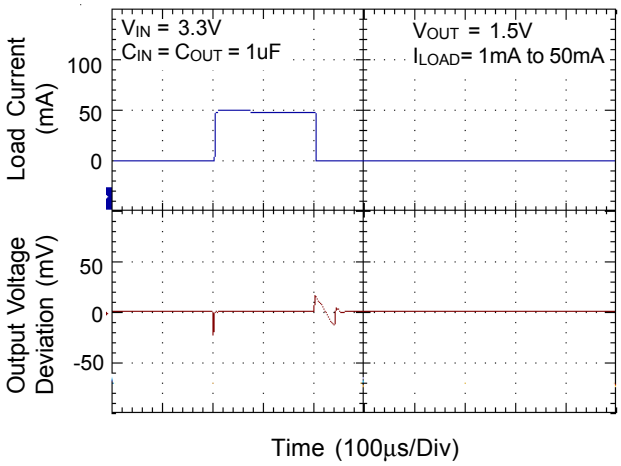
Line Transient Response



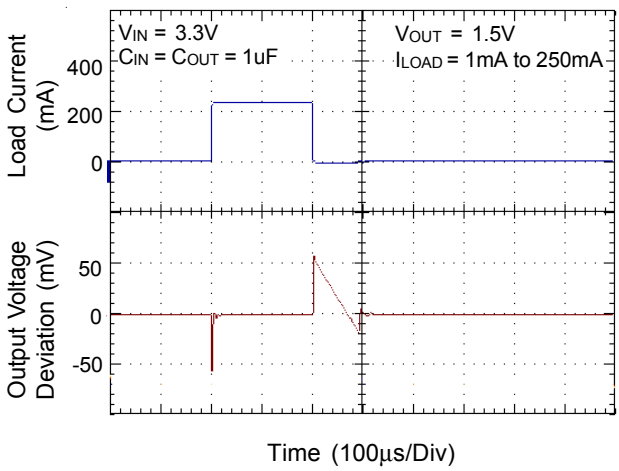
Line Transient Response



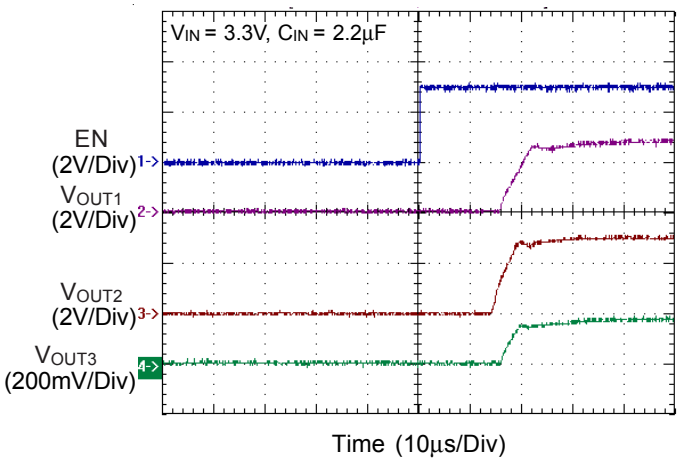
Load Transient Response



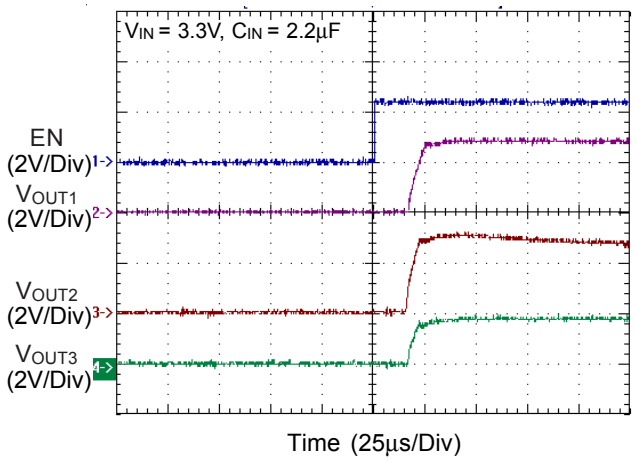
Load Transient Response



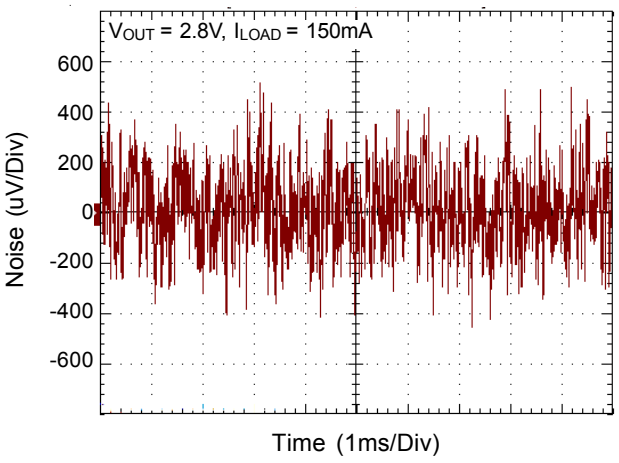
Start Up



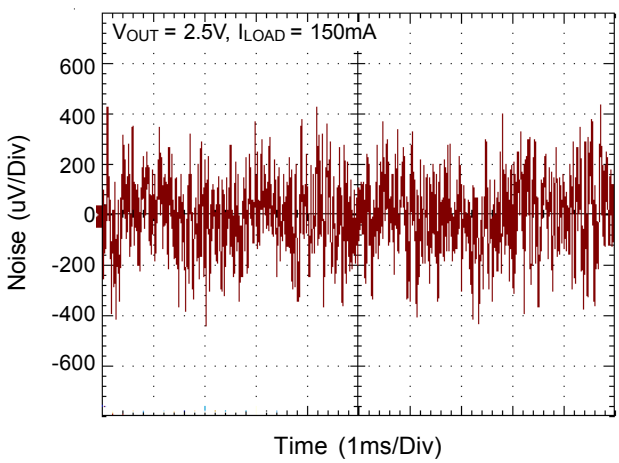
Start Up



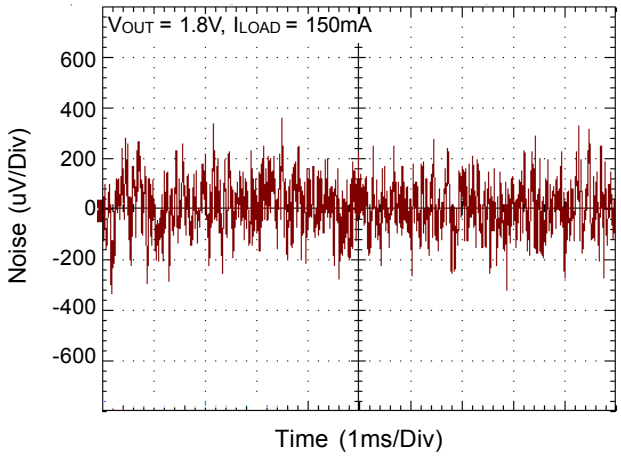
Noise



Noise



Noise



Applications Information

Like any low-dropout regulator, the external capacitors used with the RT9004 must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 2.2μF on the RT9004 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9004 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 20mΩ on the RT9004 output ensures stability. The RT9004 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1 shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the RT9004 and returned to a clean analog ground.

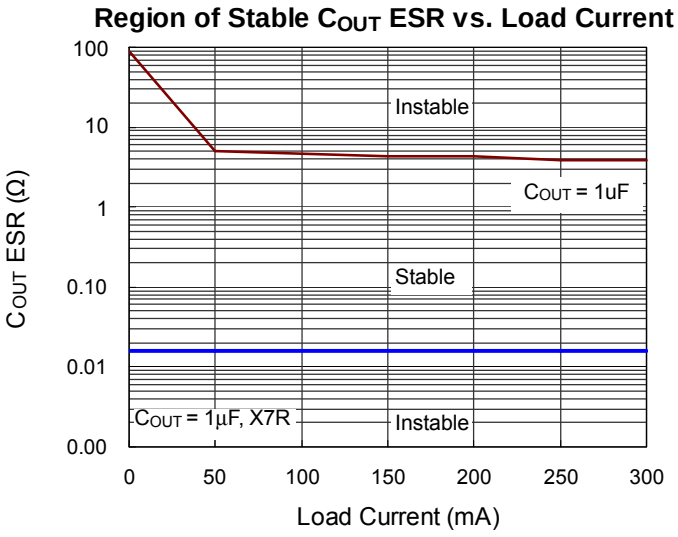


Figure 1

Enable Function

The RT9004 features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.2 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For to protecting the system, the RT9004 have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to VIN to keep the LDO regulator in a continuously on state.

Thermal Considerations

Thermal protection limits power dissipation in RT9004. When the operation junction temperature exceeds 165°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 30°C.

RT9004 lowers its OTP trip level from 165°C to 110°C when output short circuit occurs (V_{OUT} < 0.4V) as shown in Figure 2. This limits IC case temperature under 100°C and provides maximum safety to end users when output short circuit occurs.

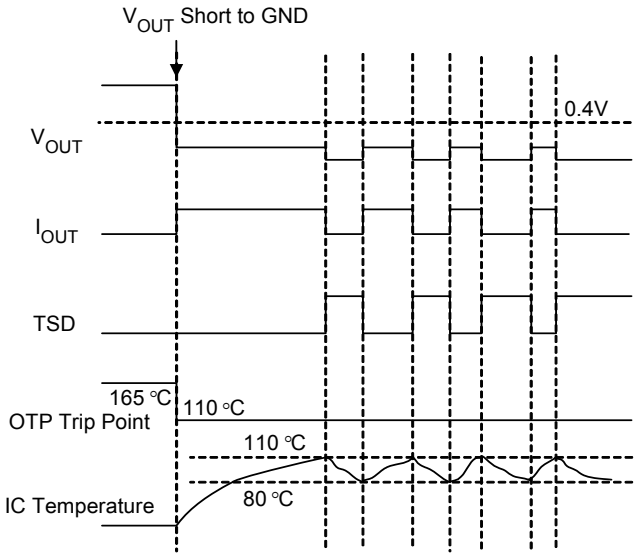


Figure 2. Short Circuit Thermal Folded Back Protection when Output Short Circuit Occurs

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$P_D = (V_{IN}-V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9004, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For VDFN-10L 3x3 and WDFN-10L 3x3 packages, the thermal resistance θ_{JA} is 105°C/W on the standard JEDEC 51-3 single-layer 1s thermal test board and 70°C/W on the standard JEDEC 51-7 4-layers 2S2P thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C - 25°C) / 105 = 0.952 W for single-layer 1s board

$P_{D(MAX)}$ = (125°C - 25°C) / 70 = 1.428 W for 4-layers 2S2P board

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9004 packages, the Figure 3 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

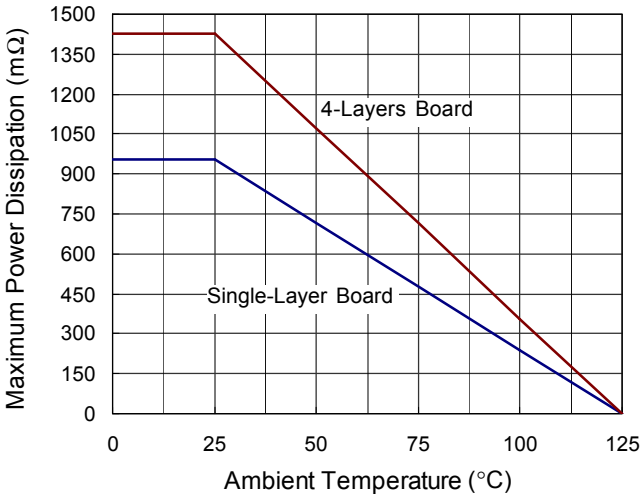
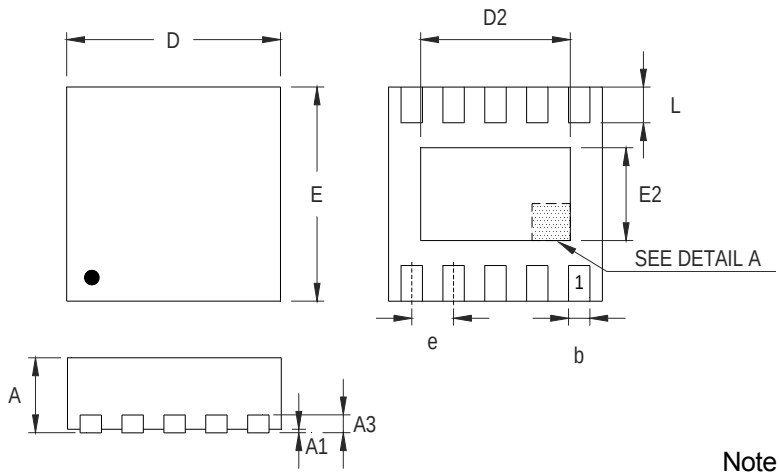
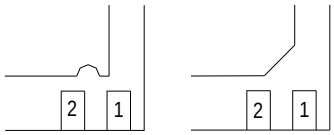


Figure 3. Derating Curves for RT9004 Package

Outline Dimension





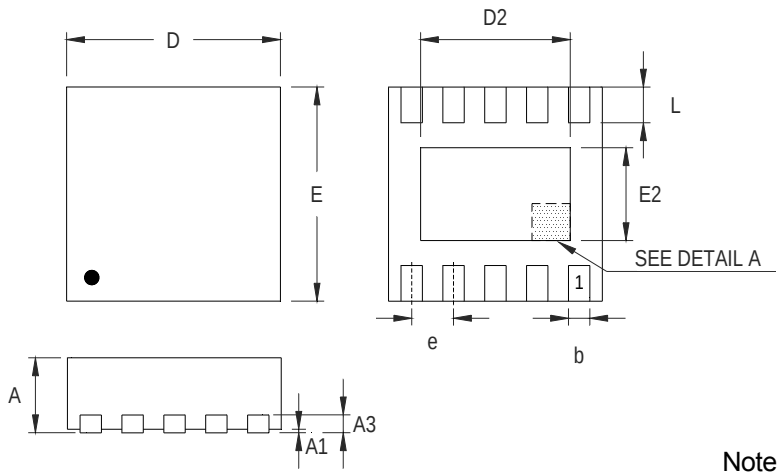
DETAIL A

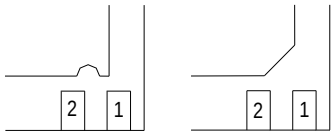
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 10L DFN 3x3 Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

Richtek Technology Corporation
Headquarter
5F, No. 20, Taiyuen Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789 Fax: (8863)5526611

Richtek Technology Corporation
Taipei Office (Marketing)
8F, No. 137, Lane 235, Paochiao Road, Hsintien City
Taipei County, Taiwan, R.O.C.
Tel: (8862)89191466 Fax: (8862)89191465
Email: marketing@richtek.com