## Features

- **8032 Pin and Instruction Compatible**
- **Four 8-bit I/O Ports**
- **Three 16-bit Timer/Counters**
- **256 bytes RAM**
- **Full-duplex UART**
- **Asynchronous Port Reset**
- **6 Sources, 2 Level Interrupt Structure**
- **64 Kbytes Program Memory Space**
- **64 Kbytes Data Memory Space**
- **Power Control Modes**
- **Idle Mode**
- **Power-down Mode**
- **On-chip Oscillator**
- **Operating Frequency: 30 MHz**
- **Power Supply: 4.5V to 5.5V**
- **Temperature Range: Military (-55°C to 125°C)**
- **Packages: Side Brazed 40-pin, MQFPJ 44-pin**
- **QML Q and V with SMD 5962-00518**
- **SCC C an B with Specification SCC9521002**

## Description

The 80C32E is a radiation tolerant ROMless version of the 80C52 single chip 8-bit microcontroller.

The 80C32E retains all the features of the 80C32 with 256 bytes of internal RAM, a 6-source, 2-level interrupt system, an on-chip oscillator and three 16-bit timer/counters.

The fully static design of the 80C32E reduces system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

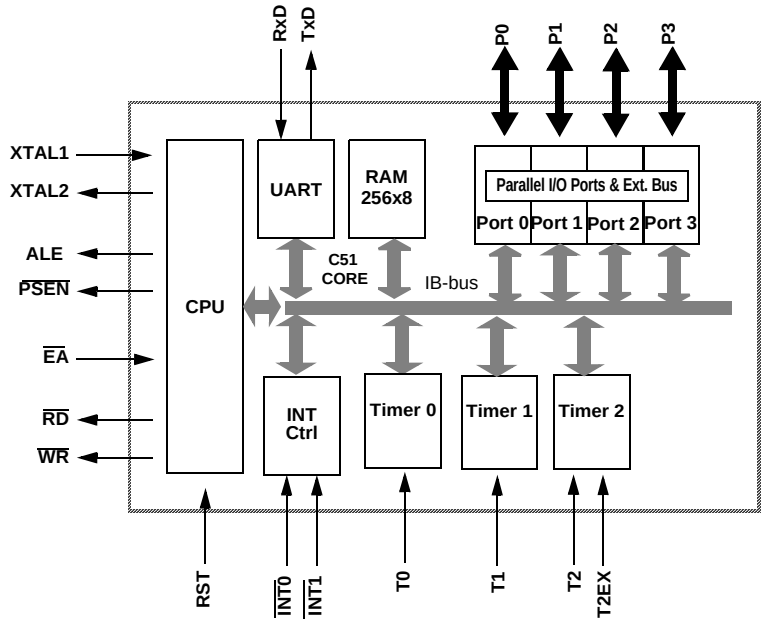
The 80C32E has 2 software-selectable modes of reduced activity for further reduction in power consumption. In the idle mode the CPU is frozen while the timers, the serial port and the interrupt system are still operating. In the power-down mode the RAM is saved and all other functions are inoperative.

# Rad. Tolerant 8-bit ROMless Microcontroller

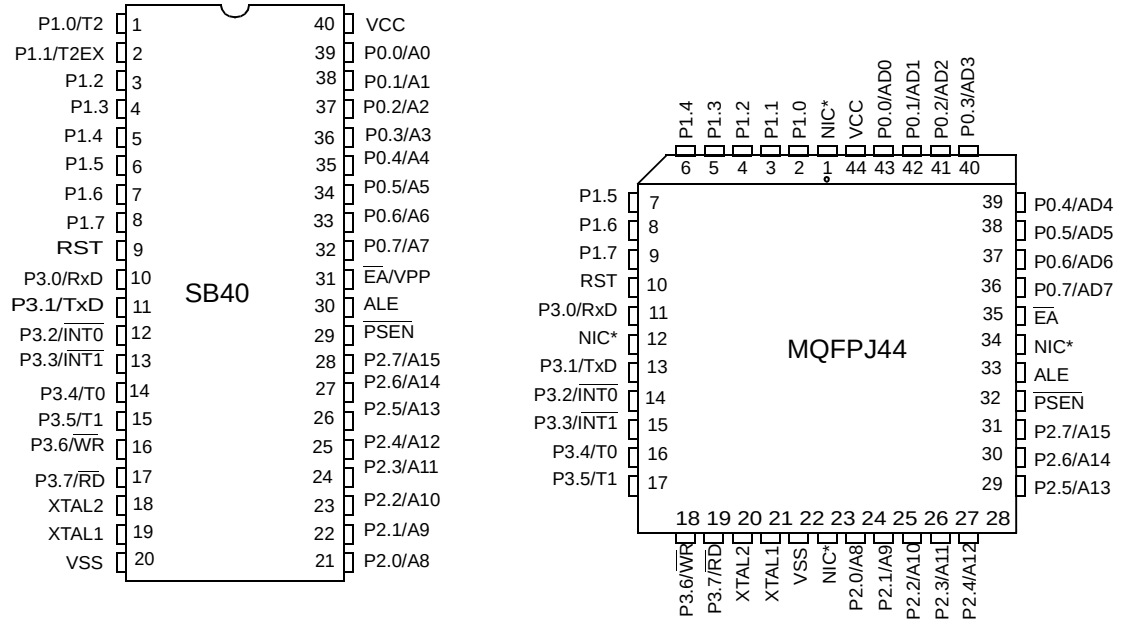
# 80C32E

Rev. 4149M–AERO–06/03

## Block Diagram




## Pin Configuration




Note: NIC: No Internal Connection

## Pin Description

| Mnemonic | Type | Name and Function |
|---|---|---|
| $V_{SS}$ | I | **Ground:** 0V reference |
| $V_{CC}$ | I | **Power Supply:** This is the power supply voltage for normal, idle and power-down operation |
| P0.0-P0.7 | I/O | **Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. |
| P1.0-P1.7 | I/O | **Port 1**: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. |
| P2.0-P2.7 | I/O | **Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 SFR. |
| P3.0-P3.7 | I/O | **Port 3**: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below. |
| | I | **RXD (P3.0):** Serial input port |
| | O | **TXD (P3.1):** Serial output port |
| | I | **$\overline{\text{INT0}}$ (P3.2):** External interrupt 0 |
| | I | **$\overline{\text{INT1}}$ (P3.3):** External interrupt 1 |
| | I | **T0 (P3.4):** Timer 0 external input |
| | I | **T1 (P3.5):** Timer 1 external input |
| | O | **$\overline{\text{WR}}$ (P3.6):** External data memory write strobe |
| | O | **$\overline{\text{RD}}$ (P3.7):** External data memory read strobe |
| RST | I | **Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on reset using only an external capacitor to $V_{CC.}$ |

| Mnemonic | Type | Name and Function |
|---|---|---|
| ALE | O (I) | **Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. |
| PSEN | O | **Program Store ENable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory. |
| EA | I | **External Access Enable:** $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations. |
| XTAL1 | I | **Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. |
| XTAL2 | O | **Crystal 2:** Output from the inverting oscillator amplifier |

## Idle and Power-down Operation

Idle mode allows the interrupt, serial port and timer blocks to continue to operate while the clock of the CPU is gated off.

Power-down mode stops the oscillator.

**Table 1.** PCON Register
PCON – Power Control Register

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **SMOD** | **-** | **-** | **-** | **GF1** | **GF0** | **PD** | **IDL** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | SMOD | **Double Baud Rate bit**<br>Set to select double baud rate in mode 1, 2 or 3. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 3 | GF1 | **General-purpose Flag**<br>Cleared by user for General-purpose usage.<br>Set by user for General-purpose usage. |
| 2 | GF0 | **General-purpose Flag**<br>Cleared by user for General-purpose usage.<br>Set by user for General-purpose usage. |
| 1 | PD | **Power-down mode bit**<br>Cleared by hardware when reset occurs.<br>Set to enter power-down mode. |
| 0 | IDL | **Idle mode bit**<br>Clear by hardware when interrupt or reset occurs.<br>Set to enter idle mode. |

Reset Value = 000X 0000
Not bit addressable

## Idle Mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into Idle mode. In Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

## Power-down Mode

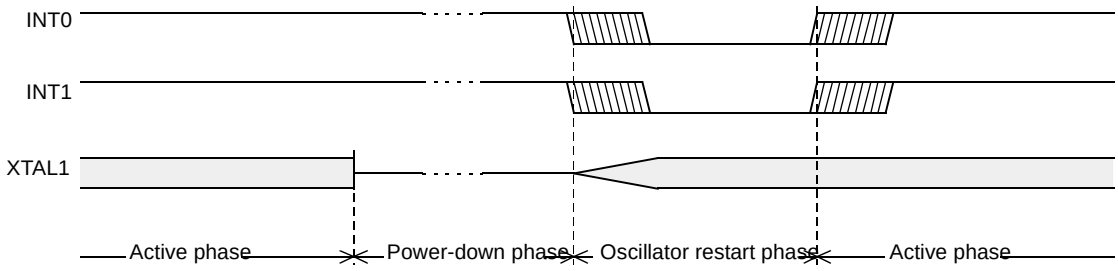
To save maximum power, a power-down mode can be invoked by software.

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. $V_{CC}$ can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before $V_{CC}$ is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.
Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 1. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and Power-down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put 80C32E into power-down mode.

**Figure 1.** Power-down Exit Waveform




Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

**Table 2.** State of Ports During Idle and Power-down Modes

| Mode | Program Memory | ALE | $\overline{\text{PSEN}}$ | PORT0 | PORT1 | PORT2 | PORT3 |
|---|---|---|---|---|---|---|---|
| Idle | External | 1 | 1 | Floating | Port Data | Address | Port Data |
| Power-down | External | 0 | 0 | Floating | Port Data | Port Data | Port Data |

## Hardware Description

Refer to the C51 8-bit Microcontroller Hardware description manual for details on 80C32E functionality.

## Electrical Characteristics

### Absolute Maximum Ratings[2]

| | |
|---|---|
| Ambient Temperature Under Bias. M = Military-55°C to 125°C<br>Storage Temperature ..... -65°C to + 150°C<br>Voltage on $V_{CC}$ to $V_{SS}$ .....-0.5V to + 7V<br>Voltage on Any Pin to $V_{SS}$.....-0.5V to $V_{CC}$ + 0.5V<br>Power Dissipation ..... 1 W[2] | Notes: 1. Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.<br>2. This value is based on the maximum allowable die temperature and the thermal resistance of the package. |

## DC Parameters

**Table 3.** DC Parameters in Standard Voltage$T_A$ = -55°C to +125°C; $V_{SS}$ = 0V; $V_{CC}$ = 5V ± 10%; F = 0 to 30 MHz.

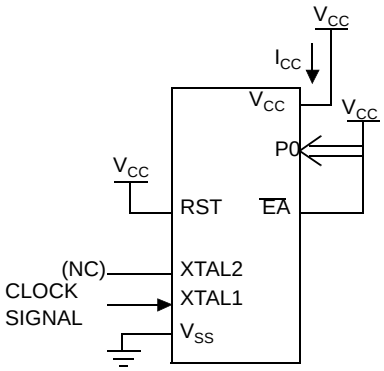
| Symbol | Parameter | Min. | Max | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.5 | 0.2 $V_{CC}$ - 0.1 | V | |
| $V_{IH}$ | Input High Voltage except XTAL1, RST | 0.2 $V_{CC}$ + 1.4 | $V_{CC}$ + 0.5 | V | |
| $V_{IH1}$ | Input High Voltage, XTAL1, RST | 0.7 $V_{CC}$ | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage, ports 1, 2, 3(5) | | 0.45 | V | $I_{OL}$ = 1.6 mA(4) |
| $V_{OL1}$ | Output Low Voltage, port 0, ALE, $\overline{PSEN}$(5) | | 0.45 | V | $I_{OL}$ = 3.2 mA(4) |
| $V_{OH}$ | Output High Voltage, ports 1, 2, 3 | 2.4<br>0.75 $V_{CC}$<br>0.9 $V_{CC}$ | | V<br>V<br>V | $I_{OH}$ = -60 µA<br>$I_{OH}$ = -25 µA<br>$I_{OH}$ = -10 µA |
| $V_{OH1}$ | Output High Voltage, port 0, ALE, $\overline{PSEN}$ | 2.4<br>0.75 $V_{CC}$<br>0.9 $V_{CC}$ | | V<br>V<br>V | $I_{OH}$ = -400 µA<br>$I_{OH}$ = -150 µA<br>$I_{OH}$ = -40 µA |
| $R_{RST}$ | RST Pull-down Resistor | 50 | 200 | kΩ | |
| $I_{IL}$ | Logical 0 Input Current ports 1, 2 and 3 | | -75 | µA | Vin = 0.45V |
| $I_{LI}$ | Input Leakage Current | | ±10 | µA | 0.45 V < Vin < $V_{CC}$ |
| $I_{TL}$ | Logical 1 to 0 Transition Current, ports 1, 2, 3 | | -750 | µA | Vin = 2.0V |
| $C_{IO}$ | Capacitance of I/O Buffer | | 10 | pF | Fc = 1 MHz<br>$T_A$ = 25°C |
| $I_{PD}$ | Power-down Current (3) | | 75 | µA | 2.0V < $V_{CC}$ < 5.5V |
| $I_{CC}$ | Power Supply Current (1)(2)(6)<br>Freq = 1 MHz Icc Op<br>Freq = 1 MHz Icc Idle<br>Freq = 6 MHz Icc Op<br>Freq = 6 MHz Icc Idle<br>Freq >12 MHz Icc Op<br>Freq >12 MHz Icc Idle | | <br>1.8<br>1<br>10<br>4<br>1.25F + 5<br>0.36F + 2.7 | <br>mA<br>mA<br>mA<br>mA<br>mA<br>mA | $V_{CC}$ = 5.5V<br><br><br><br><br><br>F in MHz |

Notes:
1. $I_{CC}$ under reset is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns (see Figure 6), $V_{IL}$ = $V_{SS}$ + 0.5V,
   $V_{IH}$ = $V_{CC}$ - 0.5V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = $V_{CC}$. $I_{CC}$ would be slightly higher if a crystal oscillator is used.
2. Idle $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns, $V_{IL}$ = $V_{SS}$ + 0.5V, $V_{IH}$ = $V_{CC}$ - 0.5V; XTAL2 N.C; Port 0 = $V_{CC}$; $\overline{EA}$ = RST = $V_{SS}$ (see Figure 4).
3. Power-down $I_{CC}$ is measured with all output pins disconnected; $\overline{EA}$ = $V_{SS}$, PORT 0 = $V_{CC}$; XTAL2 NC.; RST = $V_{SS}$ (see Figure 5).
4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the $V_{OL}$s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45V with maxi $V_{OL}$ peak 0.6V. The use of a Schmitt Trigger is not necessary.
5. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 10 mA
   Maximum $I_{OL}$ per 8-bit port:
   Port 0: 26 mA
   Ports 1, 2 and 3: 15 mA
   Maximum total $I_{OL}$ for all output pins: 71 mA

If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

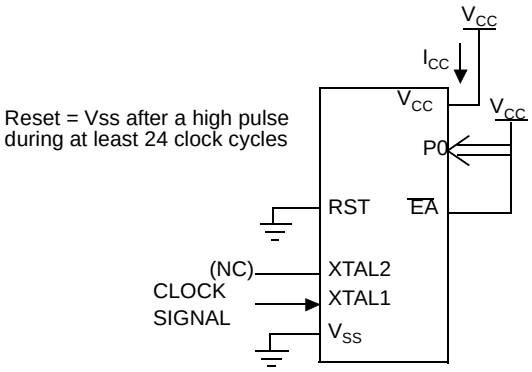
6. Operating $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns, $V_{IL}$ = $V_{SS}$ + 0.5V, $V_{IH}$ = $V_{CC}$ - 0.5V; XTAL2 N.C.; $\overline{EA}$ = Port 0 = $V_{CC}$; RST = $V_{SS}$. The internal ROM runs the code 80 FE (label: SJMP label). $I_{CC}$ would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

**Figure 2.** $I_{CC}$ Test Condition, Under Reset



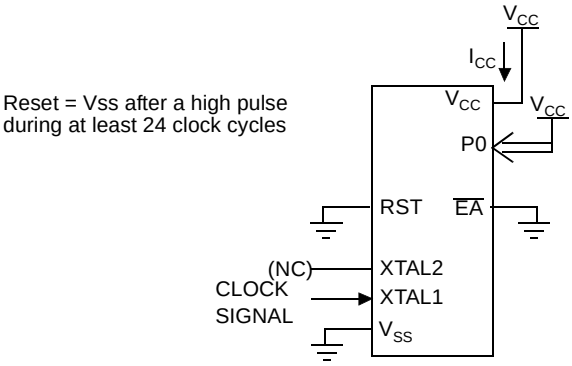

All other pins are disconnected.

**Figure 3.** Operating $I_{CC}$ Test Condition




All other pins are disconnected.

**Figure 4.** $I_{CC}$ Test Condition, Idle Mode




All other pins are disconnected.

**Figure 5.** $I_{CC}$ Test Condition, Power-down Mode

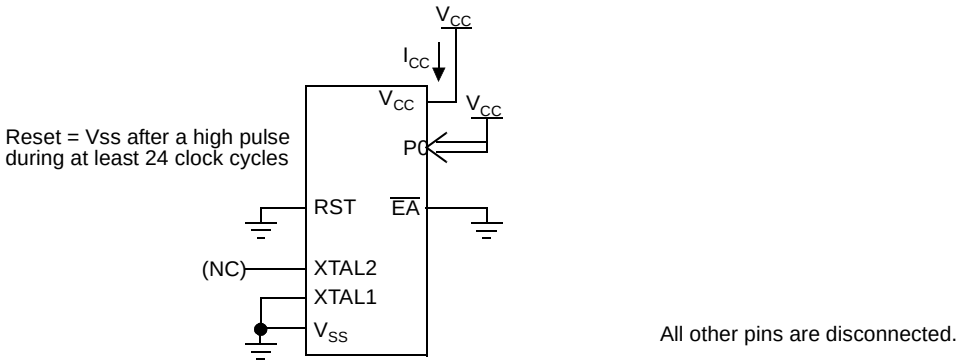
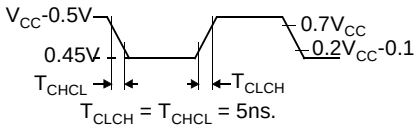



**Figure 6.** Clock Signal Waveform for $I_{CC}$ Tests in Active and Idle Modes



## AC Parameters

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:

$T_{AVLL}$ = Time for Address Valid to ALE Low.
$T_{LLPL}$ = Time for ALE Low to $\overline{PSEN}$ Low.

$T_A$ = -55°C to +125°C (Military temperature range); $V_{SS}$ = 0V; $V_{CC}$ = 5V ± 10%;

Load capacitance for Port 0, ALE and $\overline{PSEN}$ = 100 pF; Load capacitance for all other outputs = 80 pF.

**Table 4.** External Program Memory Characteristics (ns)

| Symbol | Parameter | 30 MHz | |
|---|---|---|---|
| | | Min | Max |
| $T_{LHLL}$ | ALE Pulse Width | 60 | |
| $T_{AVLL}$ | Address Valid to ALE | 15 | |
| $T_{LLAX}$ | Address Hold After ALE | 35 | |
| $T_{LLIV}$ | ALE to Valid Instruction In | | 100 |
| $T_{LLPL}$ | ALE to PSEN | 25 | |
| $T_{PLPH}$ | PSEN Pulse Width | 80 | |
| $T_{PLIV}$ | PSEN to Valid Instruction In | | 65 |
| $T_{PXIX}$ | Input Instruction Hold After PSEN | 0 | |
| $T_{PXIZ}$ | Input Instruction Float After PSEN | | 30 |
| $T_{PXAV}$ | PSEN to Address Valid | 35 | |
| $T_{AVIV}$ | Address to Valid Instruction In | | 130 |
| $T_{PLAZ}$ | PSEN Low to Address Float | | 6 |

**Figure 7.** External Program Memory Read Cycle

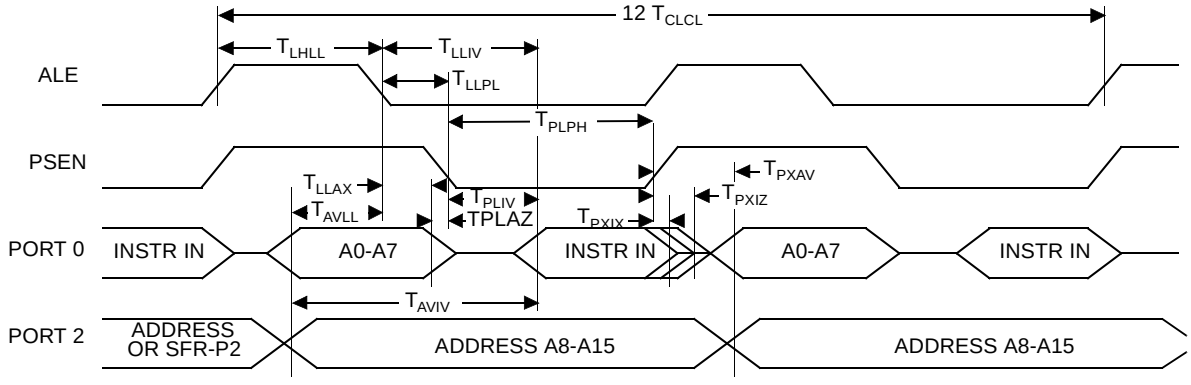


**Table 5.** External Data Memory Characteristics (ns)

| Symbol | Parameter | 30 MHz | |
|---|---|---|---|
| | | min | max |
| $T_{RLRH}$ | $\overline{RD}$ Pulse Width | 180 | |
| $T_{WLWH}$ | $\overline{WR}$ Pulse Width | 180 | |
| $T_{RLDV}$ | $\overline{RD}$ to Valid Data In | | 135 |
| $T_{RHDX}$ | Data Hold After $\overline{RD}$ | 0 | |
| $T_{RHDZ}$ | Data Float After $\overline{RD}$ | | 70 |
| $T_{LLDV}$ | ALE to Valid Data In | | 235 |
| $T_{AVDV}$ | Address to Valid Data In | | 260 |
| $T_{LLWL}$ | ALE to $\overline{WR}$ or $\overline{RD}$ | 90 | 115 |
| $T_{AVWL}$ | Address to $\overline{WR}$ or $\overline{RD}$ | 115 | |
| $T_{QVWX}$ | Data Valid to $\overline{WR}$ Transition | 20 | |
| $T_{QVWH}$ | Data set-up to $\overline{WR}$ High | 215 | |
| $T_{WHQX}$ | Data Hold After $\overline{WR}$ | 20 | |
| $T_{RLAZ}$ | $\overline{RD}$ Low to Address Float | | 0 |
| $T_{WHLH}$ | $\overline{RD}$ or $\overline{WR}$ High to ALE high | 20 | 40 |

**Figure 8.** External Data Memory Write Cycle

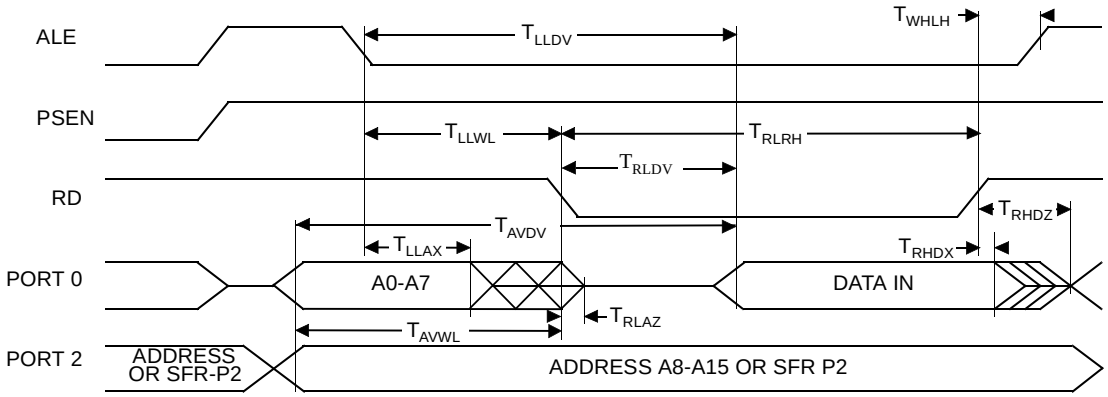


**Figure 9.** External Data Memory Read Cycle

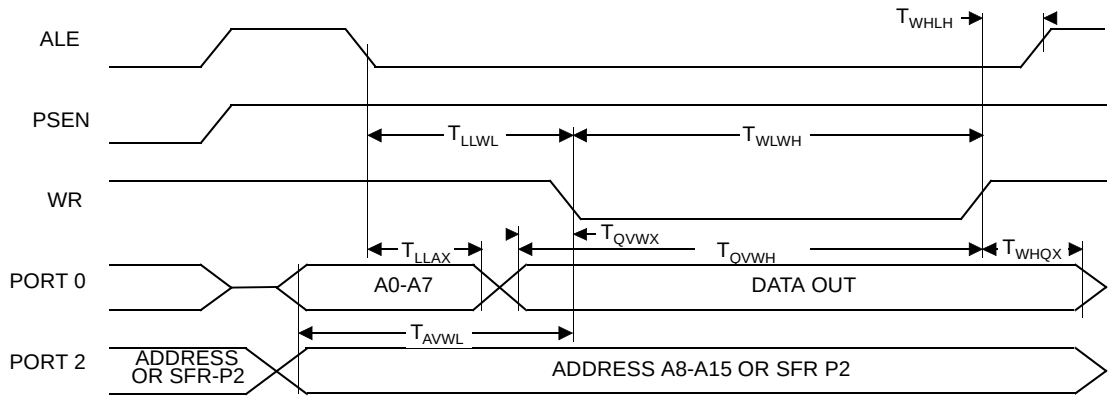



**Table 6.** Serial Port Timing – Shift Register Mode (ns)

| Symbol | Parameter | 30 MHz | |
|---|---|---|---|
| | | Min | Max |
| $T_{XLXL}$ | Serial port clock cycle time | 400 | |
| $T_{QVHX}$ | Output data set-up to clock rising edge | 300 | |
| $T_{XHQX}$ | Output data hold after clock rising edge | 50 | |
| $T_{XHDX}$ | Input data hold after clock rising edge | 0 | |
| $T_{XHDV}$ | Clock rising edge to input data valid | | 300 |

**Figure 10.** Shift Register Timing Waveforms

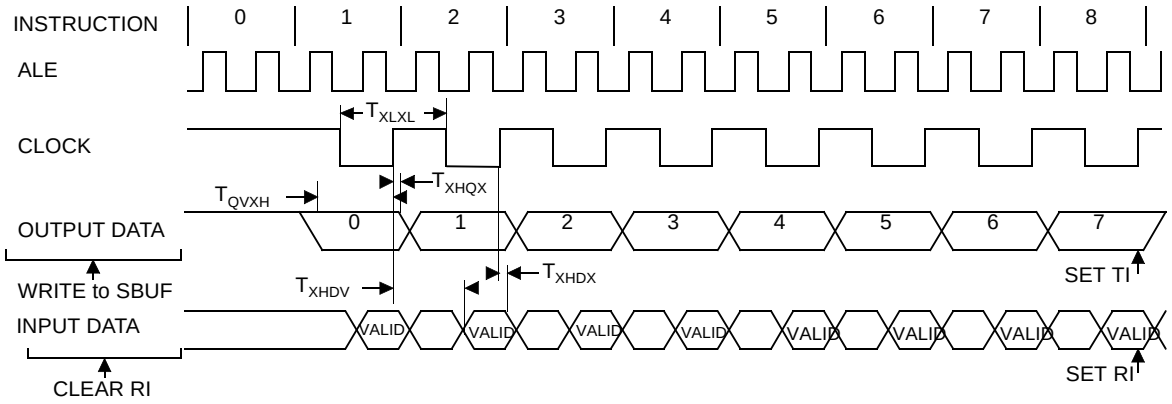


**Table 7.** External Clock Drive Characteristics (XTAL1)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_{CLCL}$ | Oscillator Period | 33.33 | | ns |
| $T_{CHCX}$ | High Time | 5 | | ns |
| $T_{CLCX}$ | Low Time | 5 | | ns |
| $T_{CLCH}$ | Rise Time | | 5 | ns |
| $T_{CHCL}$ | Fall Time | | 5 | ns |

**Figure 11.** External Clock Drive Waveforms

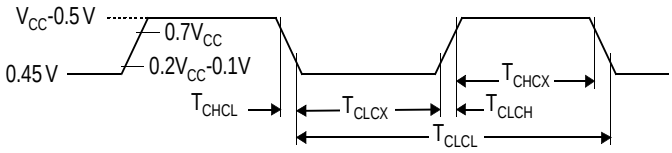
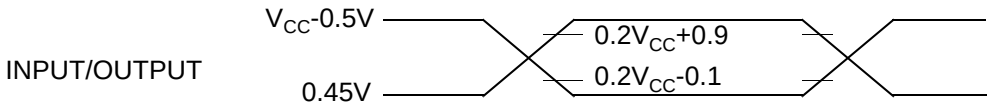
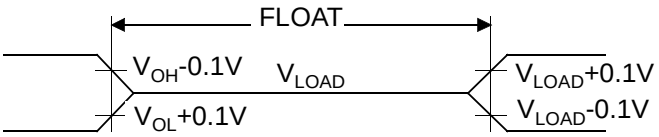



**Figure 12.** AC Testing Input/Output Waveforms



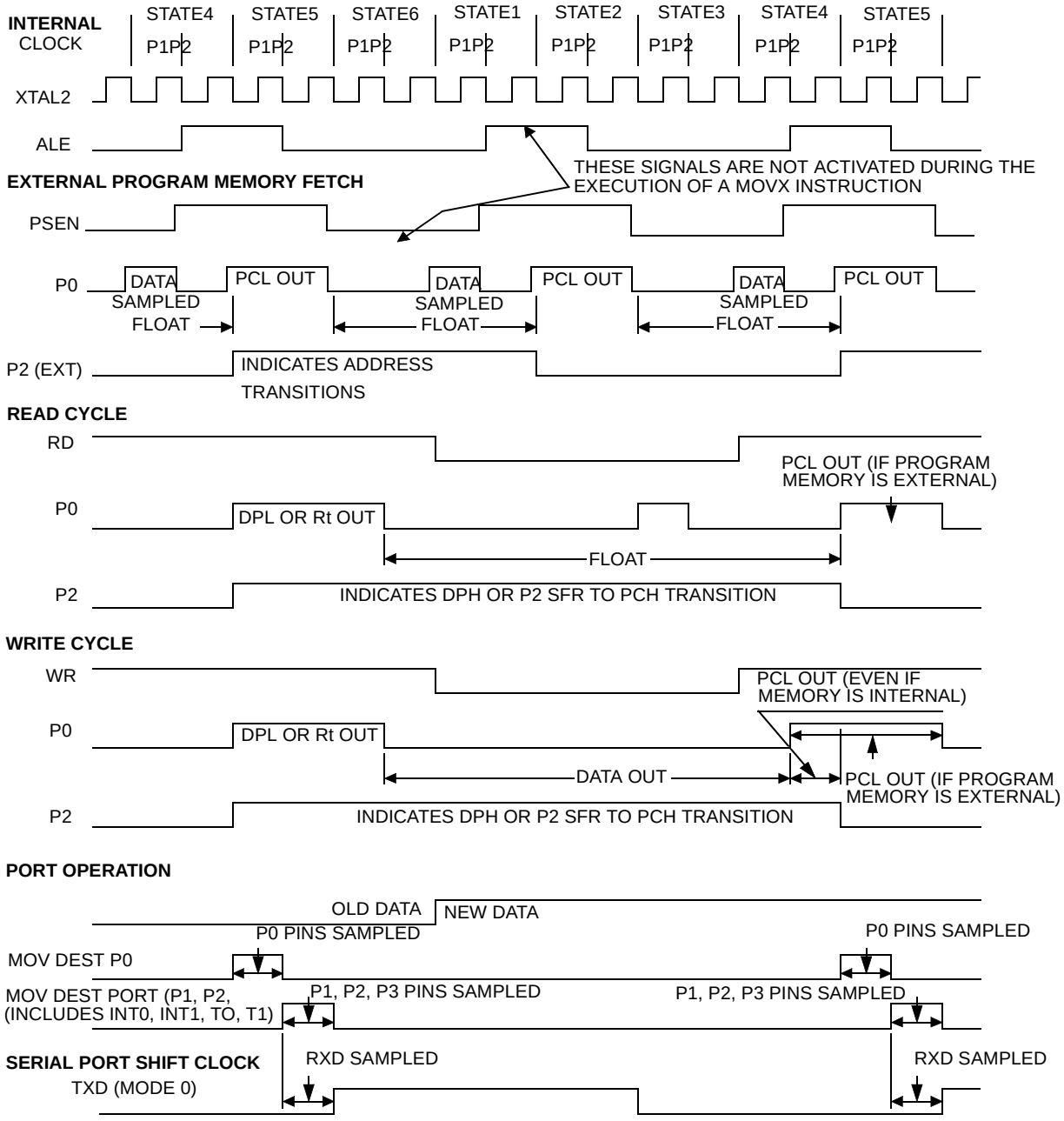

AC inputs during testing are driven at $V_{CC}$ - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at $V_{IH}$ min for a logic “1” and $V_{IL}$ max for a logic “0”.

**Figure 13.** Float Waveforms




For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded $V_{OH}/V_{OL}$ level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA.

**Figure 14.** Clock Waveforms




This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ($T_A$=25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

## Ordering Information

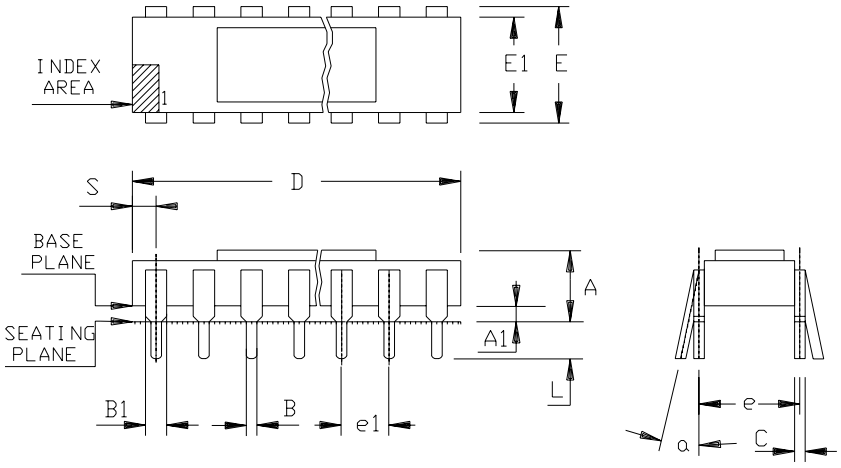
**Table 8.** Possible Order Entries

| Part Number | Speed (MHz) | Temperature Range | Package | Quality Flow |
|---|---|---|---|---|
| MC-80C32E-30-E | 30 | 25°C | Side Brazed 40-pin (.6) | Engineering samples |
| MJ-80C32E-30-E | 30 | 25°C | MQFPJ 44-pin | Engineering samples |
| MC-80C32E-30 | 30 | -55°C to +125°C | Side Brazed 40 pin (.6) | Standard Mil. |
| MJ-80C32E-30 | 30 | -55°C to +125°C | MQFPJ 44-pin | Standard Mil. |
| 5962-0051801QQC | 30 | -55°C to +125°C | Side Brazed 40 pin (.6) | QML-Q |
| 5962-0051801QXC | 30 | -55°C to +125°C | MQFPJ 44-pin | QML-Q |
| 5962-0051801VQC | 30 | -55°C to +125°C | Side Brazed 40 pin (.6) | QML-V |
| 5962-0051801VXC | 30 | -55°C to +125°C | MQFPJ 44-pin | QML-V |
| SCC9521002-01B | 30 | -55°C to +125°C | Side Brazed 40 pin (.6) | SCC B |
| SCC9521002-02B | 30 | -55°C to +125°C | MQFPJ 44-pin | SCC B |
| MM0-80C32E-30-E(1) | 30 | -55°C to +125°C | Die | Engineering samples |
| 5962-0051801Q9A(1) | 30 | -55°C to +125°C | Die | QML-Q |
| 5962-0051801V9A(1) | 30 | -55°C to +125°C | Die | QML-V |

Note: 1. Please contact Atmel for availability.

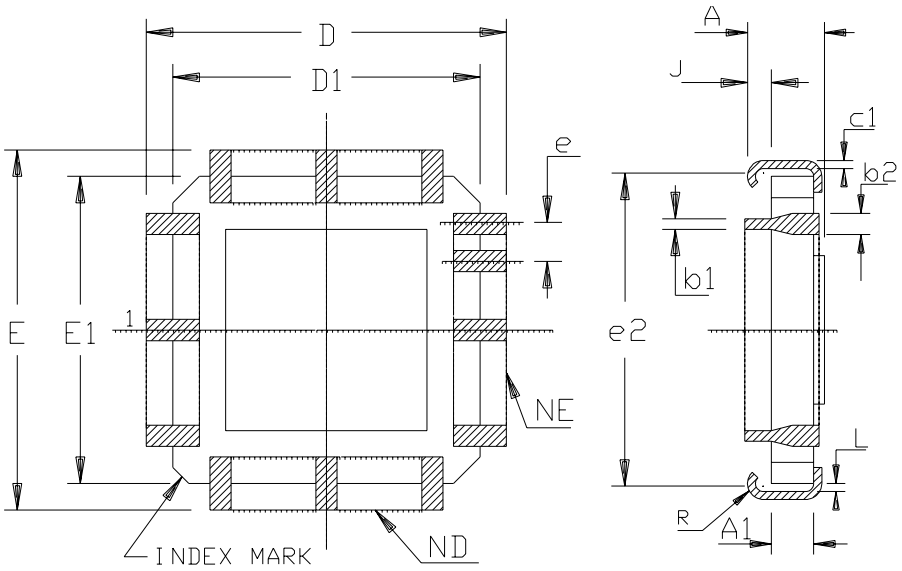
## Package Drawings

### 40-pin Side Braze (600 mils)




| | MM | | INCH | |
|---|---|---|---|---|
| A | 2.16 | 4.83 | .085 | .190 |
| A1 | 0.51 | 1.77 | .020 | .070 |
| B | 0.38 | 0.58 | .015 | .023 |
| B1 | 0.97 | 1.52 | .038 | .060 |
| C | 0.20 | 0.30 | .008 | .012 |
| D | 50.30 | 51.56 | 1.980 | 2.030 |
| E | 15.12 | 15.87 | .595 | .625 |
| E1 | 14.74 | 15.49 | .580 | .610 |
| L | 3.18 | 4.44 | .125 | .175 |
| S | 0.77 | 1.65 | .030 | .065 |
| e | 15.24 | TYP | .600 | TYP |
| e1 | 2.54 | TYP | .100 | TYP |
| a | 0° | | 15° | |
| PKG STD | 01 | | | |

## 44-pin Multilayer Quad Flat Pack




| | MM | | INCH | |
|---|---|---|---|---|
| A | 2.67 | 4.95 | .105 | .195 |
| A1 | 1.65 NOM | | .065 NOM | |
| b1 | 0.33 | 0.56 | .013 | .022 |
| b2 | 0.55 | 0.88 | .022 | .035 |
| c1 | 0.17 | 0.25 | .007 | .010 |
| D/E | 17.14 | 17.78 | .675 | .700 |
| D1/E1 | 15.74 | 16.76 | .620 | .660 |
| e | 1.27 BSC | | .050 BSC | |
| e2 | 16.00 BSC | | .630 BSC | |
| L | 0.12 | - | .005 | - |
| ND/NE | 11 | | 11 | |
| R | 0.50 | 1.01 | .020 | .040 |
| J | 0.58 | ---- | .023 | ---- |

## Atmel Headquarters


***Corporate Headquarters***
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

***Europe***
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

***Asia***
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

***Japan***
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581


## Atmel Operations


***Memory***
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

***Microcontrollers***
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

***ASIC/ASSP/Smart Cards***
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

***RF/Automotive***
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

***Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom***
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

***e-mail***
literature@atmel.com

***Web Site***
http://www.atmel.com





4149M–AERO–06/03 /xM